0.9 V, 5 nW, 9 ppm/^{o}C Resistorless Sub-Bandgap Voltage Reference in 0.18μm CMOS

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***Abstract*—In this work a novel resistorless sub-bandgap voltage reference (BGR) is introduced. It is a self-biased and small area topology that works in the nano-ampere current consumption range, and under 1 V of power supply. The analytical behavior of the circuit is described, and simulation results for a standard 0.18 μm CMOS process are analysed. A reference voltage of 479 mV is demonstrated, with a temperature coefficient of 8.79 ppm/^{o}C for the 0 to 125 $^\circ$C range, while the power consumption of the whole circuit is 4.86 nW under a 0.9 V power supply at 27 $^\circ$C. The estimated silicon area is 0.0012 mm^2.**

I. Introduction

Voltage references are fundamental circuit blocks, ubiquitously used in analog, mixed-signal, RF and digital systems, including memories. The importance of low power design is self-evident in mobile and energy harvesting applications, while resistorless approaches enable the implementation of the circuit in standard digital processes.

Basically, the bandgap voltage reference introduced by Widlar in 1971 [1] can be divided into three fundamental functions: the generation of two voltages or currents, one proportional and the other complementary to absolute temperature (PTAT and CTAT, respectively), and biasing. The biasing function sometimes is implemented inside the PTAT generator, reducing area and complexity, as is done in the traditional BGR approach [1].

The first efforts in designing low power analog circuits, including voltage references, used MOSFETs operating in the subthreshold region [2], [3]. In more recent advances, resistorless references have continued to explore this region of operation, but these circuits generally present a dedicated current biasing block, increasing complexity, area and power consumption. They explore the threshold voltage negative dependence with temperature to generate the CTAT voltage [4], [5], [6] and [7], while the conventional BJT was used in [8] (where MOSFETs are not operating in subthreshold) and [9]. Another approach is to use switched-capacitors [10], [11].

In this paper we propose a new self-biased BGR circuit, where the bias function is implemented through a counterbalance of the BJT junction voltage and MOSFETs gate-source voltages, without the need for resistors. The PTAT voltage is generated through the well known self-cascode structure [12]. This approach results in a very simple and small area topology, that works in the nano-ampere current consumption range and under 1 V of power supply.

II. Circuit Description

The proposed topology is shown in Fig.1. In this circuit, the BJT junction voltage is counterbalanced by the gate-source voltage of two stacked nMOS transistors M1 and M2. The resulting gate-source voltage defines the BJT emitter current, through a feedback path that uses a current mirror with gain K_1. By defining K_1 and the aspect ratio of M1 and M2, a non-zero equilibrium DC operating point can be reached, that reflects the current-voltage behaviour of both the BJT and the MOSFETs. Since M1 and M2 have the same drain current and the same aspect ratios, the voltage V_E appears divided by two at the gate of M1. This voltage is then added to a PTAT voltage generated by three self-cascode structures M2-M3, M4-M5 and M6-M7 to provide a temperature independent output V_{REF}. The following section explains and equates each of these contributions.

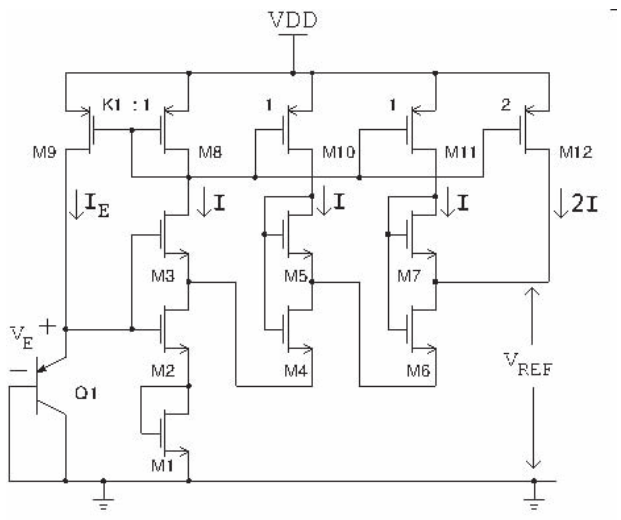

Fig. 1. Schematic of the implemented BGR circuit.

A. BJT Bias Circuit and V_E Divider

The emitter current I_E of the bipolar transistor is given by (1).

$$I_E = I_{SE} exp\left(\frac{V_E}{m\phi_t}\right) \quad (1)$$

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Where V_E is the emitter-base voltage, ϕ_T is the thermal voltage, m represents the slope factor and I_{SE} is the reverse saturation current for the p-n junction. Assuming that all MOSFETs are operating in subthreshold regime and saturated, the drain current I_D, according to the ACM MOSFET model [13], is given by (2).

$$I_D = 2eI_{SQ}\frac{W}{L}exp\left(\frac{V_G - V_{T0}}{n\phi_t} - \frac{V_S}{\phi_t}\right) \quad (2)$$

Where e is the Napier constant, I_{SQ} is the specific current per square, which is a process dependent parameter defined by carrier mobility, oxide capacitance and temperature, V_{T0} is the threshold voltage for zero bulk-source voltage, and V_G and V_S are the gate and source voltages referred to the substrate, respectively. Assuming that M1 and M2 have the same width W_1 and length L_1, and present the same slope factor n (since the bulk-source voltage is zero), their gate-source voltages will be equal, and one half of the emitter voltage, as in (3).

$$V_{GS1} = \frac{V_E}{2} \quad (3)$$

Substituting (1), (2) and (3) into the equality $K_1 I_D = I_E$, also noting that $I_{D(M1)} = 5I_{D(M8)}$ and solving for the junction voltage V_E, leads to (4).

$$V_E = \frac{\phi_t}{\left(\frac{1}{m} - \frac{1}{2n}\right)}\left[ln\left(2e\frac{K_1}{5}\frac{W_1}{L_1}\frac{I_{SQ}}{I_{SE}}\right) - \frac{V_{T0}}{n\phi_t}\right] \quad (4)$$

This expression is a simplified one, valid for the case where the source-bulk voltage is zero, which would require a triple-well nMOSFET process. Due considerations will be made on the design section regarding the implementation in standard CMOS processes.

B. PTAT Circuit

The PTAT voltage can be generated by the traditional self-cascode structure [12]. In this circuit, both MOSFETs are operating saturated and in the subthreshold region. The difference of their gate-source voltages appear across the drain-source terminals of the lower transistor, and this voltage is proportional to the thermal potential. The proportionality constant can be scaled by adjusting the current across each device and their aspect ratios S, as given by (5).

$$V_{DS(LOW)} = n\phi_T ln\left(\frac{I_{LOW}}{I_{HIGH}}\frac{S_{HIGH}}{S_{LOW}}\right) \quad (5)$$

Since $V_{DS(LOW)}$ is tipically less than 100 mV at room temperature, the lower transistor is in the limit of saturation, which introduces non-linearities in the PTAT derivative specially at high temperatures. The proposed topology uses three of these structures in series (transistors M2 to M7), which leads to a PTAT voltage given by (6).

$$V_{PTAT} = V_{DS(M2)} + V_{DS(M4)} + V_{DS(M6)} \quad (6)$$

Knowing that $I_{D(M2)} = 5I$, $I_{D(M4)} = 4I$, $I_{D(M6)} = 3I$, and substituting (5) into (6) leads to (7).

$$V_{PTAT} = n\phi_T ln\left(60\frac{S_3}{S_2}\frac{S_5}{S_4}\frac{S_7}{S_6}\right) \quad (7)$$

C. Reference Voltage

The reference voltage output is thus the sum of the divided junction voltage at the gate of M1 (3), plus the PTAT voltage (7), and it is given by (8).

$$V_{REF} = V_{GS1} + V_{PTAT} = \frac{V_E}{2} + n\phi_T ln\left(60\frac{S_3}{S_2}\frac{S_5}{S_4}\frac{S_7}{S_6}\right) \quad (8)$$

Here, the first term of the equation represents the CTAT voltage, while the second term is a constant that multiplies ϕ_T. $\partial V_{GS1}/\partial T$ is half of the junction V_E derivative, around -1 mV/^{o}C. The aspect ratios of the MOSFETs can be sized to provide a positive $\partial V_{PTAT}/\partial T$ = 1 mV/^{o}C, making the output temperature independent, or $\partial V_{REF}/\partial T \approx 0$. Non-linearities, mainly from the junction voltage [14], will degrade the performance of the circuit, resulting in the curvature usually seen in BGR circuits.

III. Design Methodology

For the BJT bias in the nano-ampere current range a junction voltage of 550 mV at 27 °C is established, leading to an emitter current of 3.5 nA. The current mirror gain is rounded to an integer value that makes common-centroid structures easier, providing good layout regularity, while current I is determined by the aspect ratio of M1 and M2. This current has to be much larger than the leakage current for the PTAT cells to work [12]. We decided to use MOSFETs biased with currents larger than 500 pA, to prevent significant errors from the drain and source leakage currents. It is also well known that the PTAT self-cascode generator works well if the upper transistor does not leave subthreshold and the lower transistor does not leave saturation. For this technology, the PTAT voltage that can be generated ranges from 50 mV to 100 mV, approximately, so each cell was designed to provide around 80 mV at 27 ^{o}C.

The proposed topology can also be implemented without floating-well nMOSFETs, which means that simpler and cheaper processes can be used. In this case, the V_E voltage is not equally divided between the stacked nMOSFETs M1-M2, because of the body effect that increases the threshold voltage of the devices with $V_S > 0$ V. If one considers $n = 1.3$, then $V_{GS2} = 0.57V_E$ and $V_{GS1} = 0.43V_E$. Practically, it reduces the drain current of the MOS branches and can be compensated by increasing the current gain K_1. The PTAT voltage generated will be approximately the same, but, because the transistors now have theirs bulks tied together at ground, the minimum voltage supply of the circuit will increase. The final sizing of the design is presented in table I.

IV. Simulation Results

The results presented here are for schematic simulations only, using grounded-well nMOSFETs. Since simulation differences between schematic and post-layout extraction affect

TABLE I. MOSFET AND BJT SIZING FOR THE PROPOSED BGR

	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	Q1
W (μm)	8	8	80	2	16	2	16	2	12	2	2	4	2
L (μm)	2	2	2	2	2	2	2	2	2	2	2	2	2

mainly the dynamic behavior of the circuit, it should only impact the power supply rejection ratio (PSRR) curve at high frequencies, not changing the circuit's DC operating point. A preliminar placement was done to estimate the silicon area, already considering common-centroid structures and dummies. It is a very small topology, occupying only 0.0012 mm^2, as shown in Fig.2.

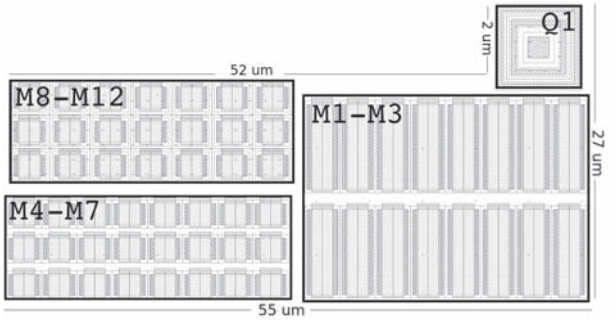

Fig. 2. Layout floorplanning of the proposed reference.

The voltage reference obtained is around 479 mV, with a slight curvature due to the non-linearity of the BJT's emitter voltage, as shown in Fig.3*a*. The effective temperature coefficient, as given by (9), is 8.79 ppm/^{o}C for the 0 to 125 ^{o}C temperature range, with V_{DD} = 0.9 V.

$$TC_{EFF} = \frac{V_{REF_{max}} - V_{REF_{min}}}{(T_{max} - T_{min})V_{REF(27^oC)}} \quad (9)$$

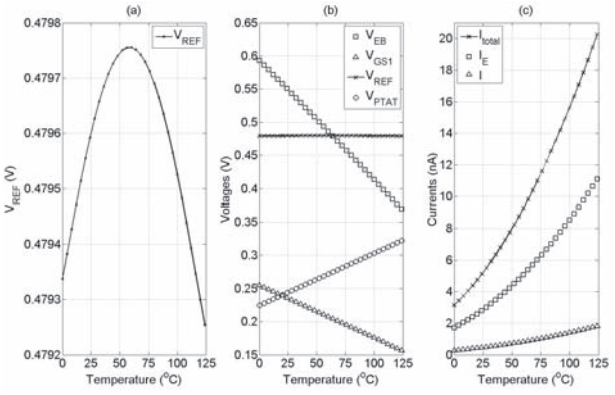

Fig. 3. (a) V_{REF}; (b) V_E, V_{GS1} and V_{PTAT} voltages; (c) I_{TOTAL}, I_E and I currents over temperature.

In Fig.3*b* we show the V_E voltage, that is divided by approximately two, then added to V_{PTAT} to form the temperature independent V_{REF}. Fig.3*c* presents the currents in each branch, which is 5.4 nA for the whole circuit at 27 ^{o}C, reaching a maximum of 20.5 nA at 125 ^{o}C. Startup behavior of the circuit was simulated, having a settling time of less than 200 μs, which is acceptable for our proof of concept. We expect that leakage currents are enough to start the circuit, but in real applications a startup circuit could be necessary for faster settling.

Even though the nominal supply voltage of the process used is 1.8 V, this implementation starts operating around 0.85 V, as shown in Fig.4*a*. The line sensitivity of V_{REF} is 2.112 mV/V from 0.85 V to 1.8 V, while the current consumption sensitivity is 69 pA/V - Fig.4*b*. Below 0.85 V, the PTAT cells are not working yet, and have zero drain current, which makes the feedback loop increase the current in the M1-M3 branch to achieve equilibrium with the junction voltage V_E. PSRR measured at 100 Hz and V_{DD} = 0.9 V, is -48 dB - Fig.4*c*. Both line sensitivity and PSRR could be increased by adding cascode current sources, for example, at the penalty of increasing the minimum supply voltage.

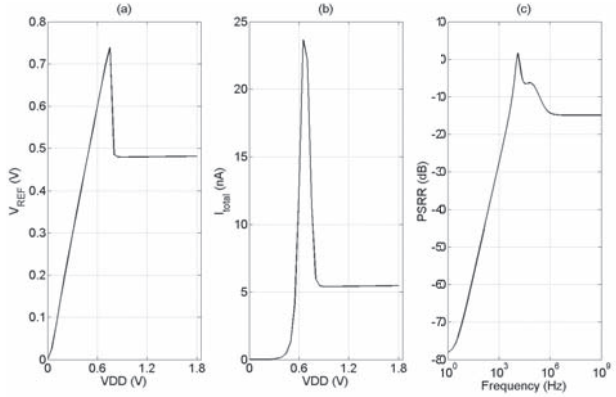

Fig. 4. (a) V_{REF}; and (b) I_{TOTAL} versus power supply; (b) PSRR versus frequency.

In Table II, a comparison of recently published low-power, resistorless voltage references in CMOS technology is presented. It is clear that one of the greatest advantages of our topology is the very small area, low temperature coefficient and power consumption, while providing comparable line sensitivities and PSRR. The temperature range could be increased to -40 ^{o}C if a higher TC is tolerated (but still much below 100 ppm/^{o}C). Similar results were obtained on a different 0.13μm CMOS digital process using low-power transistors, and we soon expect to tape out the proposed circuit.

To analyze the fabrication variability of the circuit, Monte Carlo (MC) simulation was done separately for local mismatch effects and average process variations, with 100 runs each. For average process MC, all the transistors have their parameters changed equally in each run. For local mismatch MC, the parameters of each transistor are varied individually in each run. Fig.5*(a)* shows the spread of the reference voltage, with a $\sigma/\mu = 2\%$ for mean process variation, while local mismatch, shown in Fig.5*(c)*, yields $\sigma/\mu = 0.8\%$. Fig.5*(b)* presents the spread of the temperature coefficient, where 96 % of the parts

TABLE II. COMPARISON OF RECENT RESISTORLESS CMOS VOLTAGE REFERENCES

Specification	[4]$^{+}$	[5]$^{+}$	[8]*	[6]$^{+}$	[7]$^{+}$	[9]*	**This Work***	Unit
Technology	0.35	0.35	0.5	0.18	0.18	0.18	**0.18**	μm
Temperature	0-80	-20-80	-40-120	0-125	-20-80	-40-120	**0-125**	^{o}C
Power Supply	0.9-4	1.4-3	3.6	0.45-2	0.5-3.6	0.7-1.8	**0.85-1.8**	V
Line Sensitivity	2700	20	-	4400	440	-	**2112**	ppm/V
V_{REF}	670	745	1.23	263.5	328	548	**479**	mV
Temperature Coefficient	10	7	11.8	142	176.4	114	**8.79**	ppm/^{o}C
Power @ V_{DDmin}	36	300	$6.48{\cdot}10^{5}$	3.15	0.011	52.5	**4.86**	nW
PSRR @ 100 Hz	-47	-45	-31.8	-45	-49	-56	**-48**	dB
Area	0.045	0.055	0.1	0.043	0.0014	0.0246	**0.0012**	mm^2

CTAT voltage generator: ($^{+}$) MOSFET threshold voltage V_{T0}; (*) BJT junction voltage V_E.

yield a TC below 50 ppm/^{o}C for mean process variations, while for local mismatch only the spread is much smaller and all parts have TC $<$ 12.5 ppm/^{o}C. Despite the very small area, it is clear that the major problem in the proposed reference is the average process variation, which has much larger impact in MOSFETs operating in the subthreshold condition.

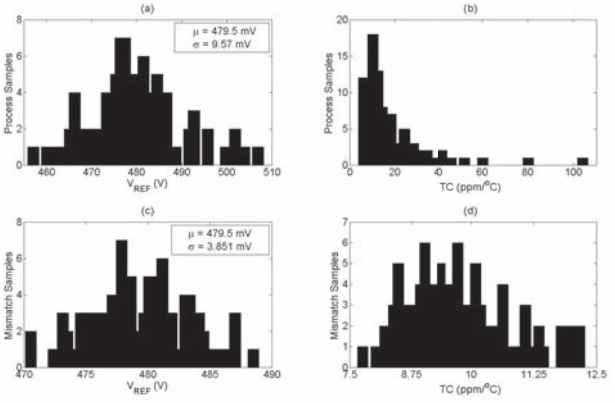

Fig. 5. V_{REF} and TC_{EFF} Monte Carlo results. Average process variation on (a) and (b); Local mismatch on (c) and (d);

As noted before by other authors [9], reports of variability results in such voltage references is still somewhat poor, specially regarding experimental results with a significant number of samples. For that reason, no comparison table of variability results is presented.

V. CONCLUSION

A novel resistorless low-power bandgap voltage reference topology was presented. It is composed by MOSFETs in the subthreshold region and a vertical parasitic PNP BJT only. The topology was designed and simulated in a 0.18μm CMOS technology, demonstrating a reference voltage of 479 mV with a power consumption of 4.86 nW, under a 0.9 V power supply. The main advantages are the low temperature coefficient of 8.79 ppm/^{o}C from 0 to 125 ^{o}C, with an estimated silicon area of 0.0012 mm^2. Monte Carlo simulations show that the spread of the reference voltage is $\sigma/\mu = 2\%$ for average process variation and $\sigma/\mu = 0.8\%$ for local mismatch. The design presented is a proof of concept that can be optimized for a given thermal stability, area and power consumption specification according to the application requirements.

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