MOSIS Lab Evaluation Report - 1.2 Volt Supply Band Gap Reference

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MOSIS Information

- Design Number = 91836
- Fab ID = V4CCAP
- Number of Parts Received = 40
- Number of Parts Tested = 2

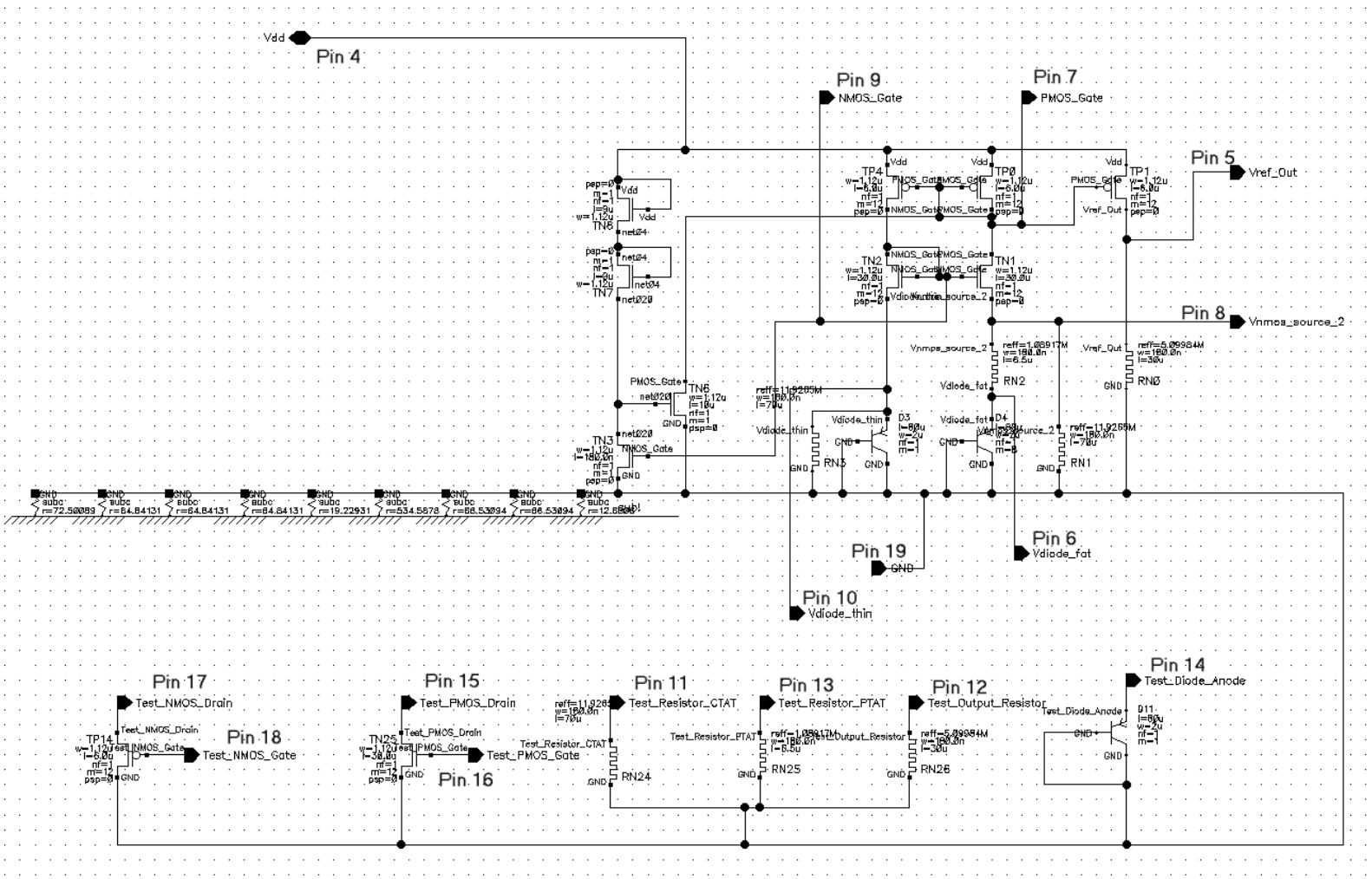
Preface

Early measurements were hard to interpret because:

- Measurement sweep time was fast enough that start up time of the band gap reference was significant.
- Band gap reference was oscillating. This was suppressed by placing a large ceramic capacitor between NM1 gate and source nodes.
- In the following discussions U1 and U2 refer to the 2 sample chips tested.

I have included all my measurement steps because they reinforce my argument as to what is causing problems with this design. If you are interested only in the conclusions then skip to that page. The original design document is included for those who might be interested.

Circuit Diagram Test Node Reference Diagram



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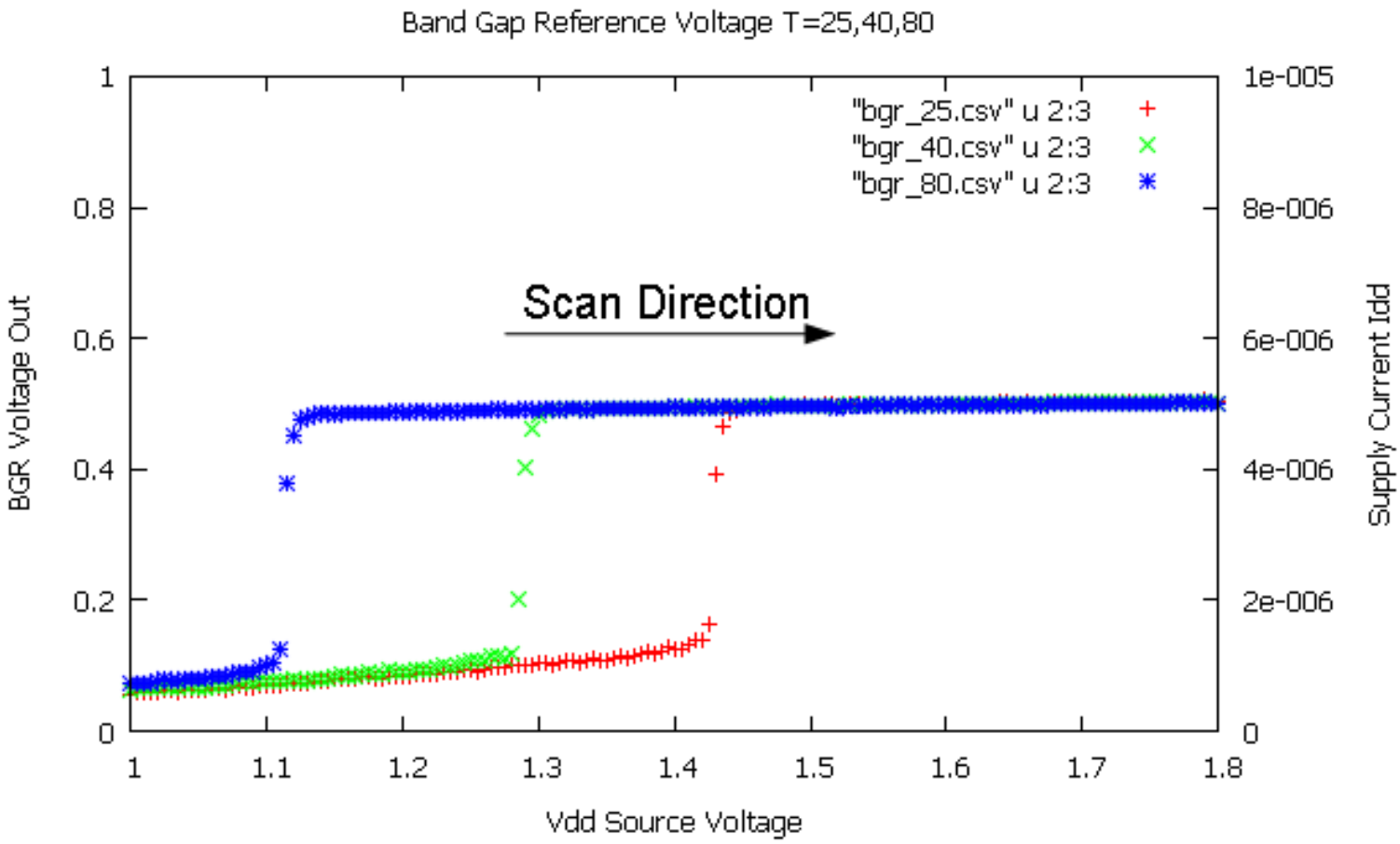
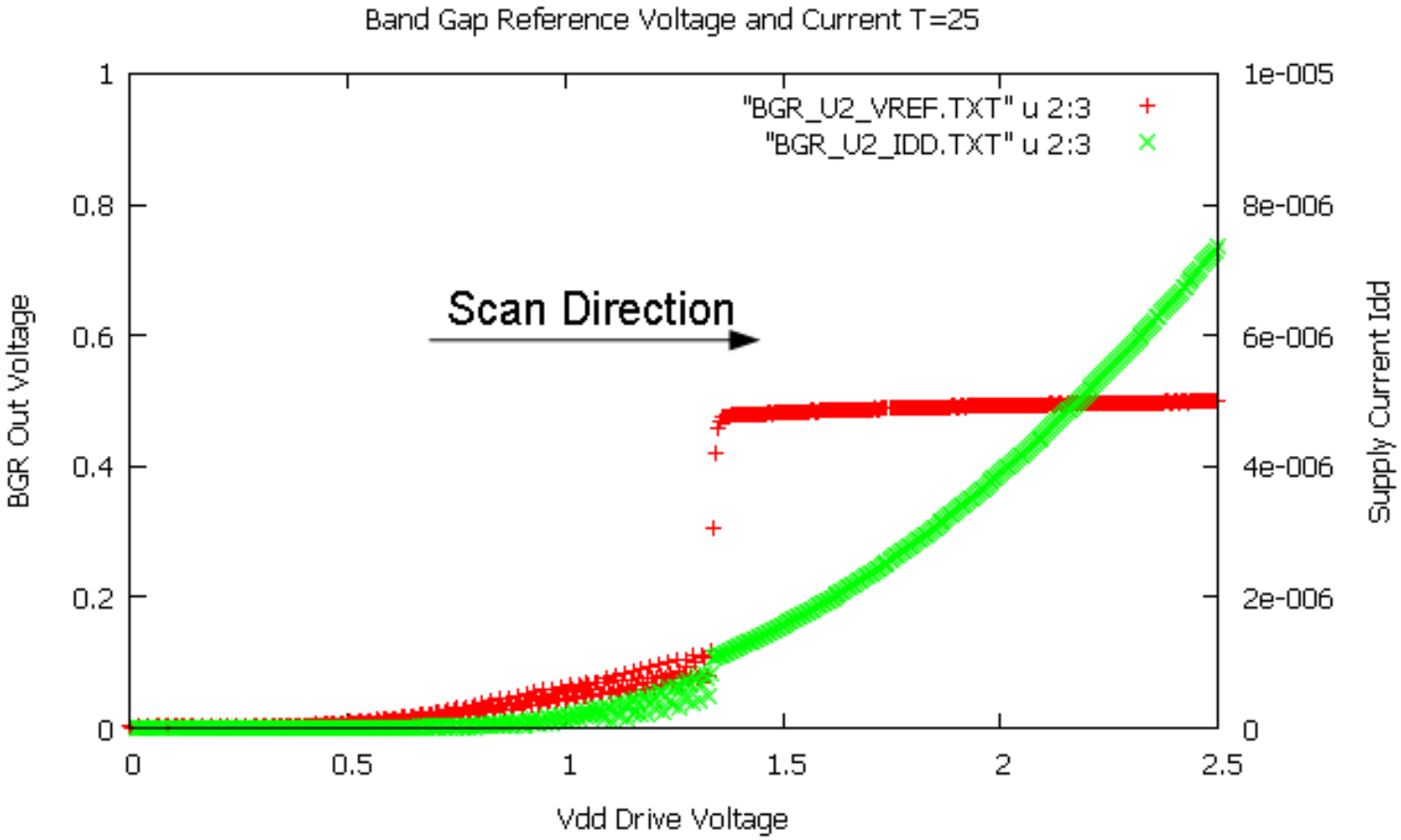
Phase 1: Attempts at direct measurement.



U1: Band gap reference V_{Ref} versus V_{dd} at Temperatures of 25, 40, 80 degrees

Notes

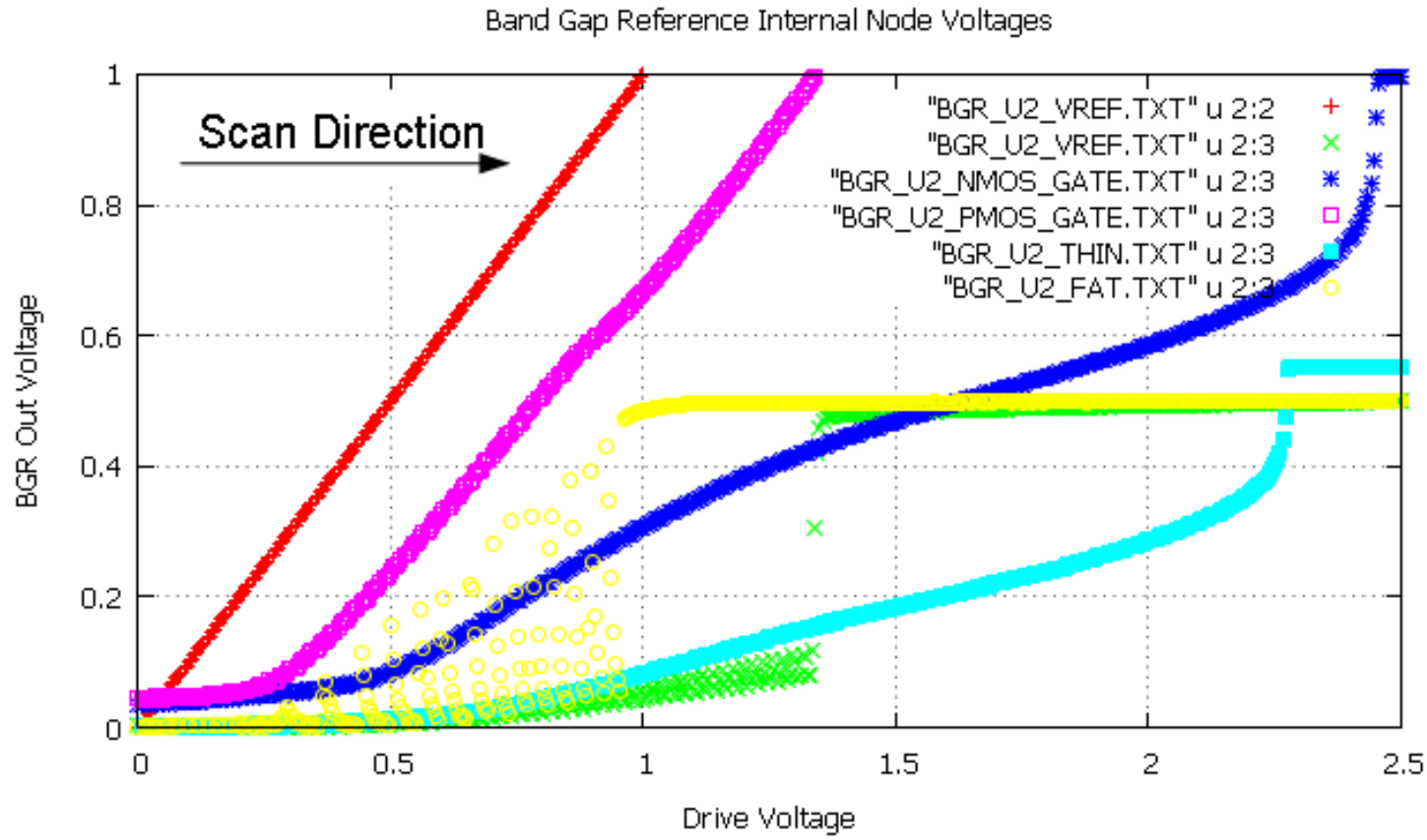
- The circuit did not function at 0 degrees Celcius.
- Turn on voltage follows trend of decreasing threshold voltages see in simulations. Is this correct?

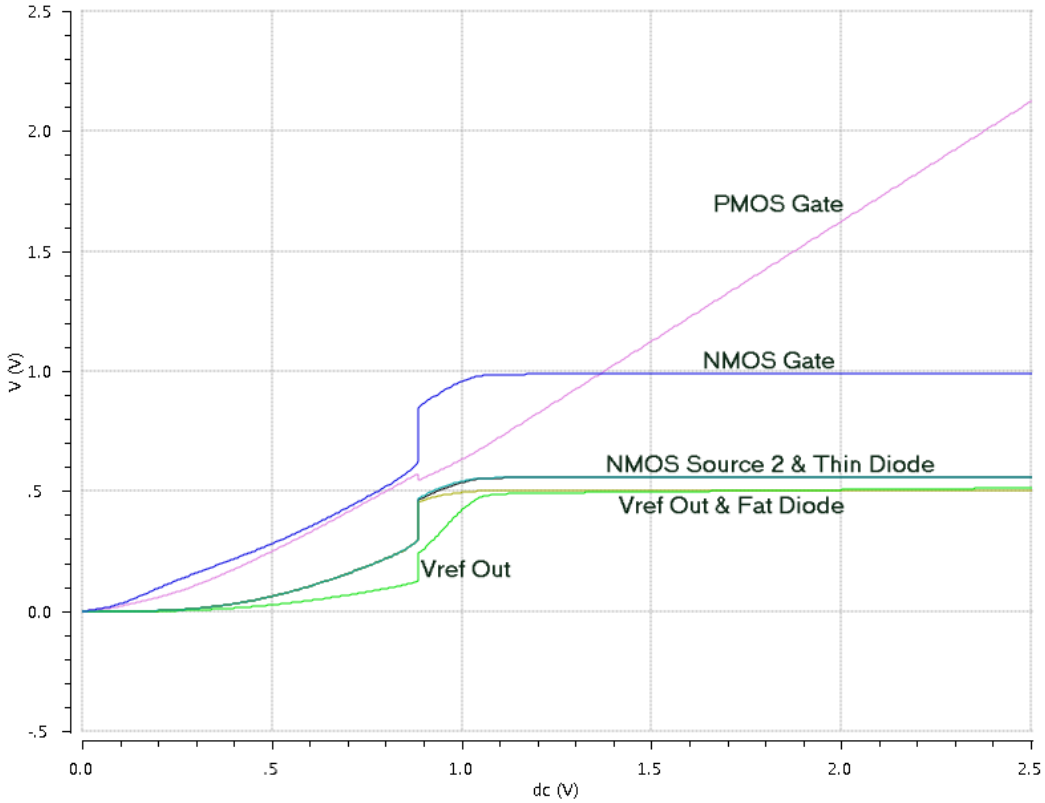


I_{DD} versus V_{DD} of BGR Circuit

Notes

- U1: Note how I_{dd} is noisy and after the turn on point no longer is noisy. This is suspicious. Oscillation of turn on circuit? The discontinuity of noise behavior at turn on makes it hard to blame this on measurement apparatus.
- Maybe something else is oscillating and able to affect the currents in the weaker lower value states of current.

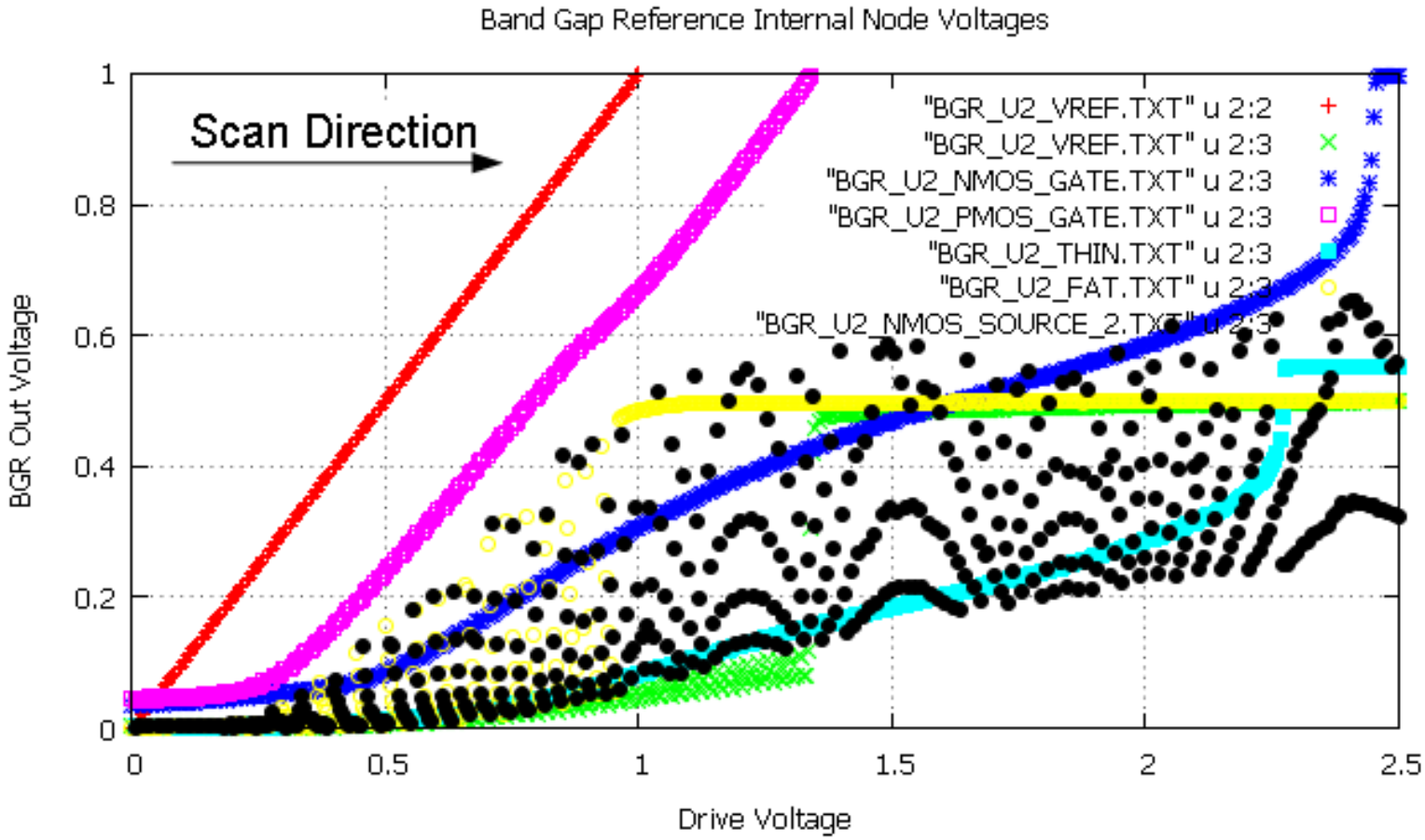




U2: BGR internal node voltages. Top: measured. Bottom: Simulated.

Notes

- Note how the "fat diode" node voltage appears to be oscillating.
- In the measured node values the "fat diode" node voltage appears inexplicable. It should be less than the "thin diode" voltage at all times. Also NM1 MOSFET would have a negative gate - source bias. NM1 should have no current at all! Simulated node voltages make more sense. In the simulated node voltages all the abrupt transitions occur at the same time. Why not in the measured dataset ?
- The oscillating node "Vnmos_source_2" was left off the previous plot due to its distracting nature. See the next plot.

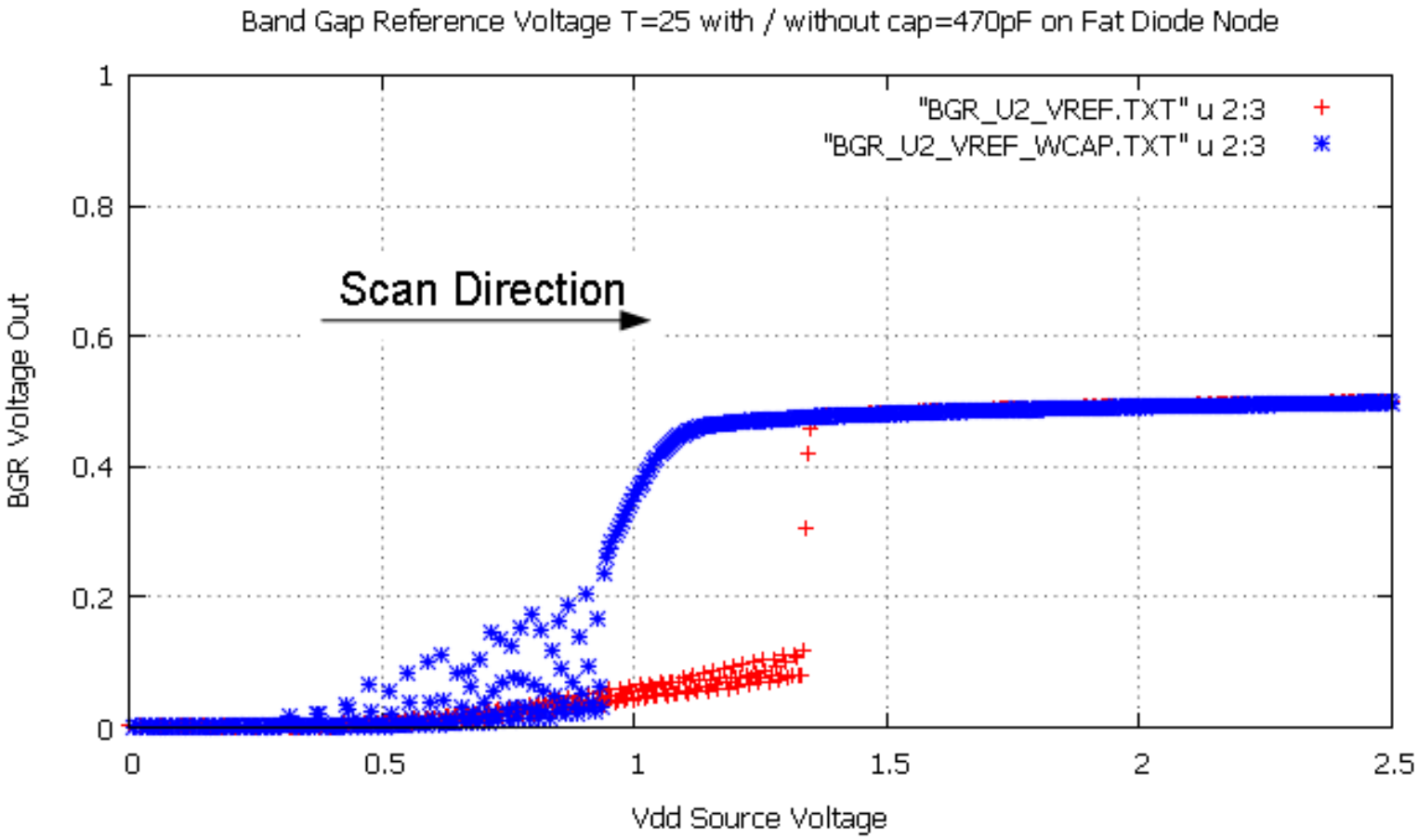


U2: BGR internal node voltages with "Vnmos_source_2" included. Something is obviously oscillating!

Notes

- "Vnmos_source_2" appears to bounce off of the nominal voltage level it is supposed to be which is equal to "BGR_U2_THIN" less the voltage across the series resistor which is about 50mVolt.
- Only this node shows the oscillation through out the measured V_{dd} range. It appears NM1 or the start up circuit or both are oscillating. Most likely it is NM1. It is set up with classic negative resistance oscillator configuration. High source / emitter impedance is always a risk.
- NMOS _Gate and Vdiode_Thin limit out on the right hand side in agreement with simulation. (flat tops at the right of the plot)

At this point an external capacitor was placed that connected NM1's gate and source to suppress any possible oscillations that it might be causing.



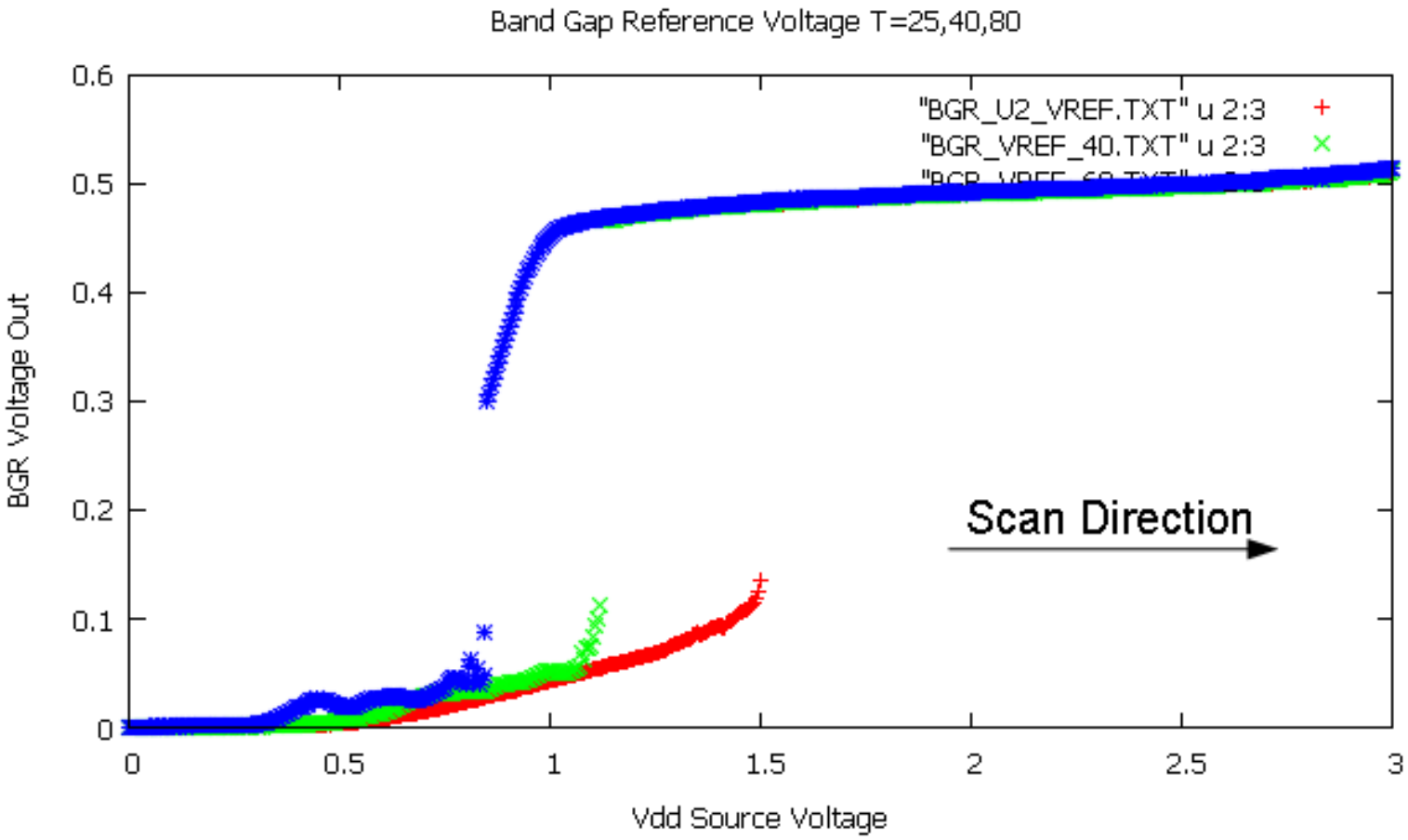
BGR supply voltage turn on threshold with and without oscillation suppression capacitor on node NMOS_SOURCE_2 node.

Notes

- U2: The above plot shows how the V_{dd} circuit turn on threshold changes after placing a capacitor on the "fat diode" node. It is almost certain there is an oscillation occurring in the circuit. The most likely candidate is NMOS FET TN1 as was suggested by the previous plot showing the measured voltage waveform on this device's source node.
- Why should the turn on threshold change with suppression of oscillation? It should not. I did not realize it yet but at this point it is becoming obvious that turn on speed is an issue.

Phase 2: Direct measurement Data / Plots After the suppression of oscillation

Band Gap Reference Pin Out - The oscillation suppression capacitor is connected between pin #8 and #9 (NM1's gate and source)

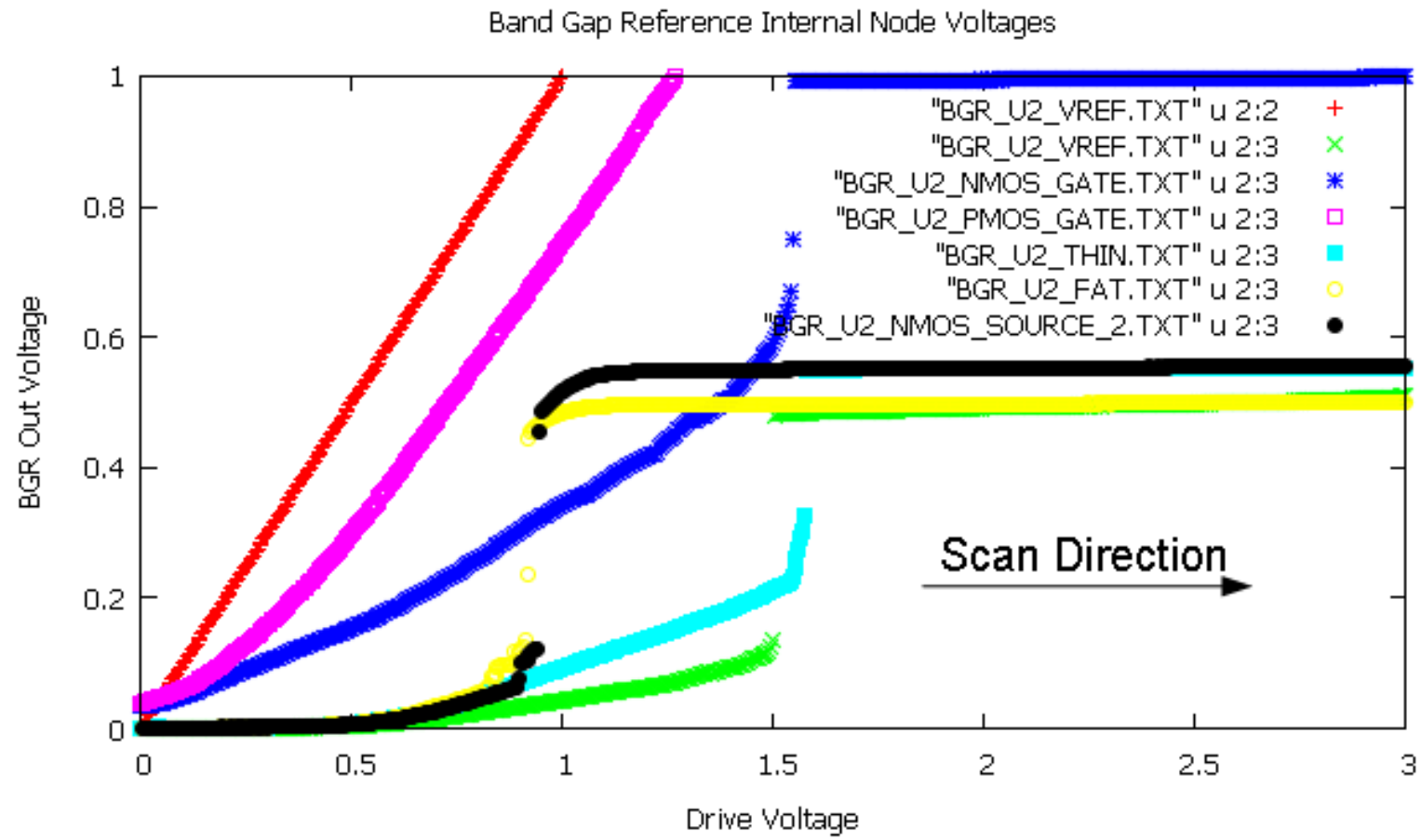


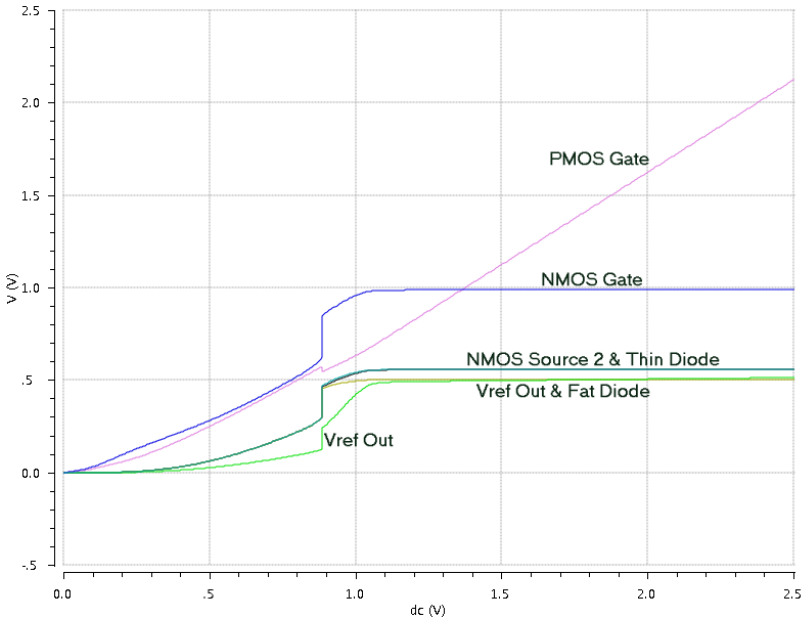
U2: Band gap reference V_{Ref} versus V_{dd} with Temperature as a parameter

Notes

- The circuit did not function at 0 degrees Celcius. (again)
- Turn on voltages are different from phase 1 measurements but still not materially different in nature.

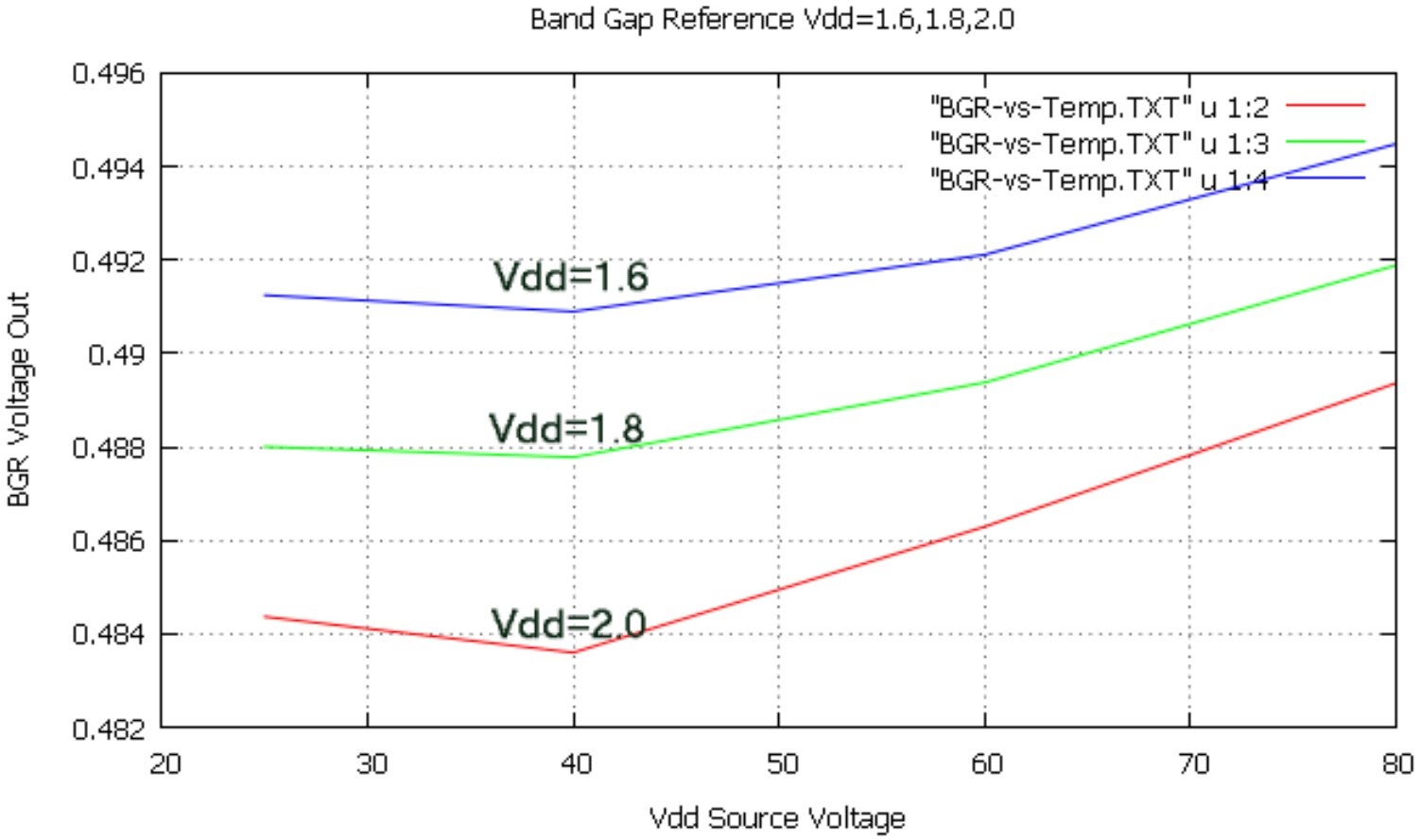
Measurement of internal voltages - After oscillation suppression





U2: BGR internal node voltages. Top: measured. Bottom: Simulated.

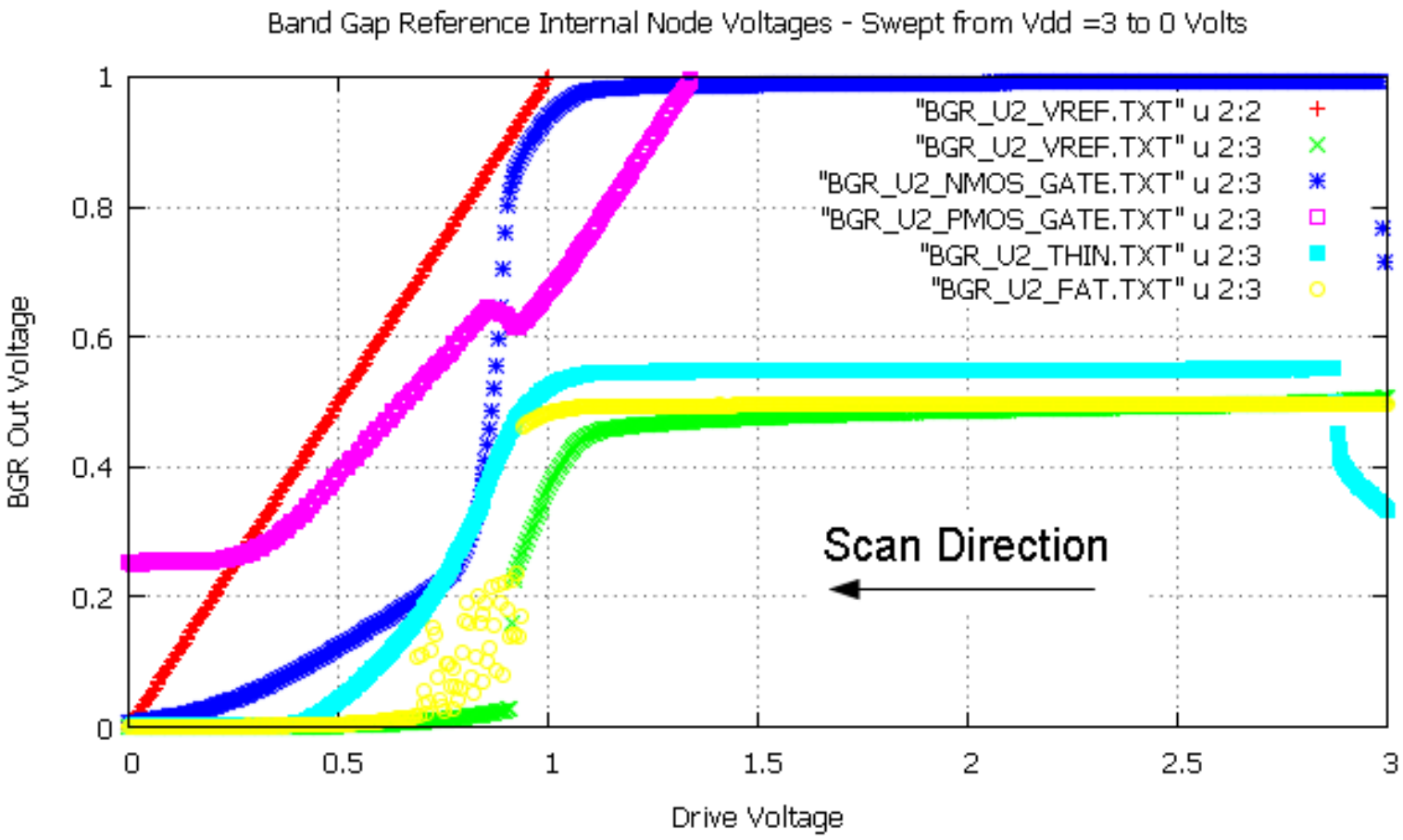
- How can the NMOS_SOURCE_2 node have vastly more current than the "thin diode" leg? Impossible! Something else is wrong.
- Why are the abrupt voltages not occuring at the same time?



U2: BGR output reference voltage versus temperature with parameter V_{dd}

Phase 3: Measurement of BGR running a reversed scan

In the following Vdd is swept from high to low voltage to alleviate the turn on threshold measurements dependence on BGR turn on time.



Temperature = 25C Degrees. Scanning from $V_{dd} = 3$ to 0 Volts insures the band gap reference is fully on as it approaches its lower Vdd operational limit.

Notes

- The BGR now functions almost down to $V_{dd} = 1$ Volt at room temperature in contrast to sweeps that went from $V_{dd} = 0$ to 3 volts where the BGR appeared to turn on at nominally 1.4 Volts.
- The abrupt voltage transitions are now aligned properly. Now I am convinced I have the correct data.

Conclusions

- Start up circuit is weak and only starts the circuit slowly - Needs a better startup circuit
- Start up circuit oscillates in the transition region - This probably will always happen to some degree in any design.
- NMOS NM1 oscillates all the time - was able to suppress with oscillation with the Vdd= 0 to 3 Volts sweep. When I went back with the same part and swept 3 to 0 Volts the bandgap refused to start up with the suppression capacitor in place. Should have done a stability analysis
- Small amount of moisture may be a problem with this circuit. Residual effects after being cooled were observed which subsided after adequate time for drying. (speculation!)
- The core of the BGR circuit appears to work as designed from Temperature =25 to 80C.
- There is ambiguity remaining as to why the BGR does not function properly at 0 degrees C. It could be:
  - the start up circuit is too weak to start it there. This is the most likely due to the fact that even when supplied with voltage well above where all threshold and saturation voltages should be satisfied the BGR did not start.
  - condensation has a noticable effect on the parts operation - could that be preventing operation?
  - It is unlikely the NM1 oscillation is the culprit.

———————————————-*End of Laboratory Evalution*———————————————-
———————————————-*Original Design Document Begins Next Page*———————————————-
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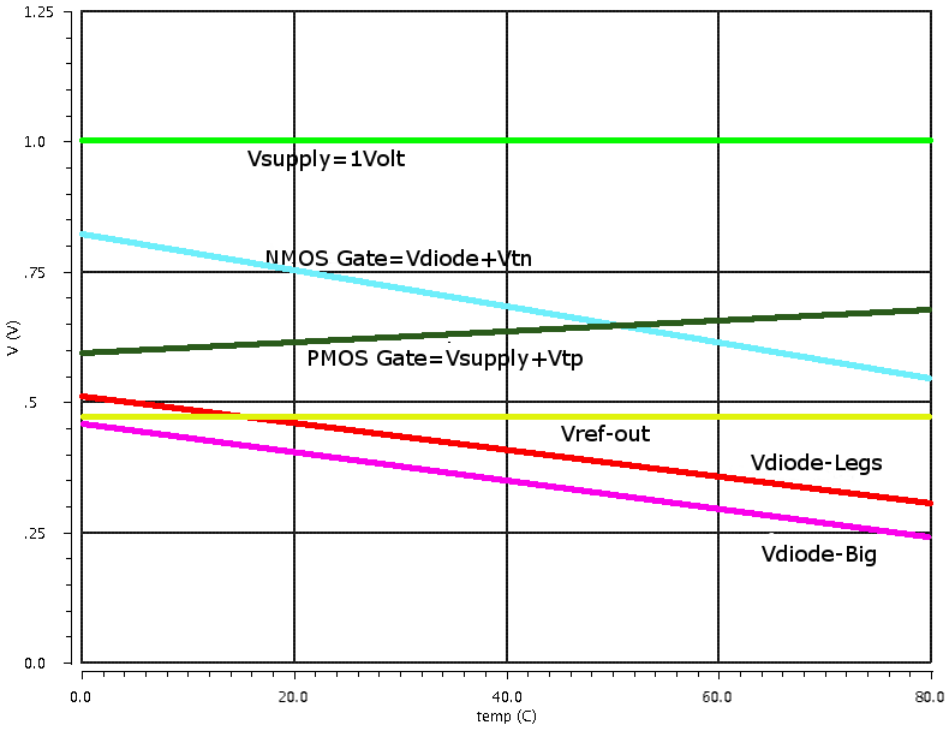
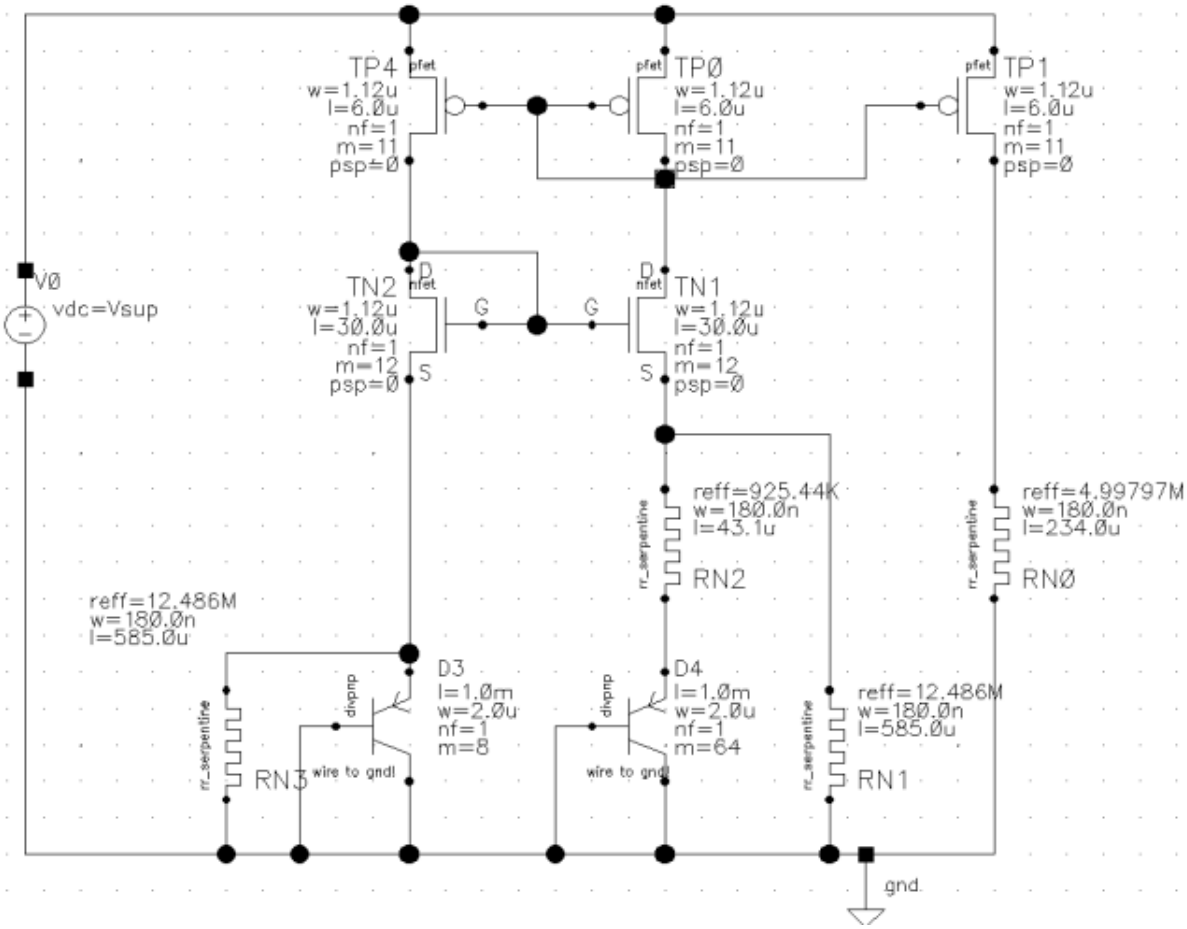
Project Specifications

- bandgap reference
- maximum power consumption = 10 microwatt,
- supply voltage = 1.8 V (better if the bandgap operates from supply voltage = 1.2 V)
  - For Vsupply=1.2V this implies Itotal = 10uW/1.2V = 8.7uAmpere supply current.
- Temperature range from 0 to 80 celsius
- Topology Used: Voltage Following Current Source

1. The limiting factor of this topology over temperature is the MOSFET threshold voltage variation with temperature. The following graph illustrates the variation of PMOS gate node, NMOS gate node and the diode reference leg voltage.





$V_{SUPPLY_{Minimum}} = V_{DIODE} + V_{TN1} - V_{TP0} =\sim 0.5 + 0.110 + 0.450 = 1.06 Volts$

Minimum usable supply voltage occurs where the threshold voltages are maximum at low temperatures. FET TN1 reaches its minimum V_{DS} under this condition. This estimate depends on FET TN1 on the edge of weak inversion at $i_f = 1$ in to allow operation down to $Vds = 110mV$.

2. Resistor hand calculation

Choosing:

- $I_{reference} = 100nAmp$
- $\frac{A_{Diode-Big}}{A_{Diode-Small}} = 8$

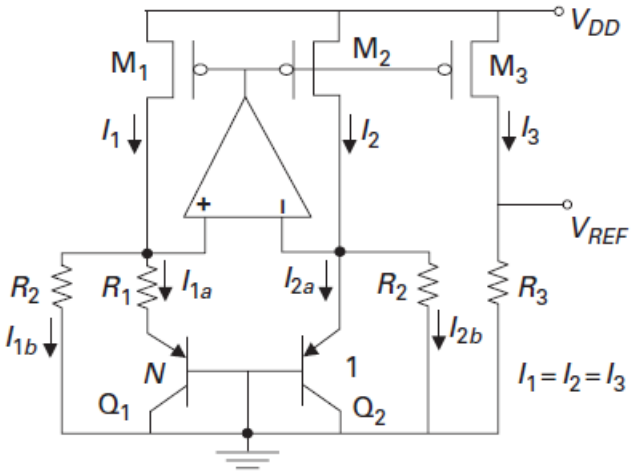


Fig. 6.13 A circuit for generating a sub-1-V bandgap reference.

In the same manner as figure 13 of our text:

$V_{Reference} = \frac{R_3}{R_2} V_{Diode-Small} + \frac{R_3}{R_1} \frac{KT}{q} ln(A_{Ratio})$

$\frac{dV_{Reference}}{dT} = 0 = \frac{R_3}{R_2} \frac{dV_{Diode-Small}}{dT} + \frac{R_3}{R_1} \frac{K}{q} ln(A_{Ratio})$

$\frac{dV_{Diode-Small}}{dT} = -2mV/C$

with $A_{ratio} = 8$

$0 = \frac{R_3}{R_2}(-2mV/C) + \frac{R_3}{R_1}(179 * 10^{-4})$

$\frac{R_2}{R_1} = \frac{2mV}{0.179mV} = 11.17$

Choosing: $I_{reference} = 100nAmp$

$\frac{\phi_T ln(8)}{R_1} + \frac{V_{Diode-Small}}{R_2} = 100nA$

$\frac{\phi_T ln(8)}{R_1} + \frac{V_{Diode-Small}}{11.17R_1} = 100nA$

$R_1 = 967kOhm$

$R_2 = 10.81MOhm$

Picking $V_{Reference} = 0.5Volts$ with $I_{Mirror} = 100nA$ sets $R_3 = 5MOhm$

These resistor values have to be fine tuned in simulation to get more precise values that set the nominal room temperature slope to 0. In the first step the hand design was simulated using ideal resistors to isolate design issues. After arriving at the simulation adjusted values the ideal resistors were replaced with serpentine resistors from the IBM 7RF library. Serpentine resistors appear to be poorly behaved over temperature however since all resistors in this circuit work off the same mirrored current the design still works. RN0, RN1, RN2, RN3 should be placed near each other in the layout to maximize tracking.

3. Diode Calculations

Once $I_{Mirror} = 100nAmp$ and $V_{Diode-Small} = 0.450Volts$ were chosen the diode area was dictated the current density. The simulator was used to obtain this value.

4. Calculate the voltage variation the PMOS current mirror sees. The current and the voltage across the diode legs must be equal to achieve the BGR function.

Current mirror requirement: In order to maintain a 10mVolt window in the output the current mirror has to match to better than 2nAmp . I will budget 1nAmp for the PMOS mirror to allow some budget for the other parts.

Drain voltage maximum temperature variation is calculated below from the $V_{Threshold}$values simulated. This is the value that the current mirror will see and must hold current to within 1nAmp in value between legs.

$\Delta V_{TP4-Drain_{Temperature}} = \Delta V_{TP_{Temperature}} = -0.375) - (-0.450) = 0.250$

$\Delta V_{TN_{Temperature}} = 0.300 - 0.350 = -0.050$

$\Delta V_{Diode_{Temperature}} = 0.325 - 0.500 = -0.175$

$\Delta V_{TP0-Drain_{Temperature}} = \Delta V_{TN_{Temperature}} + \Delta V_{Diode} = -0.05 - 0.175 = -0.225$

$\Delta V_{PMOS-Mirror_{Temperature}} = 0.250 - (-0.225) = 0.475 Volts$

5.Calculate the PMOS current mirror FET length

Current mirror equation

$\frac{I_{out}-I_{in}}{I_{out}} = \frac{V_{out}-V_{in}}{V_{Early}}$ **or** $\frac{\Delta I_D}{I_{out}} = \frac{\Delta V_{DRAIN}}{V_{Early}}$

Assume: $I_{LEG} = 100nAmp$ and using $\Delta V_{DRAIN} = 0.475 Volts$ from above

$\frac{1nAmp}{100nAmp} = \frac{0.475}{V_{Early}}$

$V_{Early} = 47.5$

$L_{PMOS} = 47.5/8.7 = 5.5$ ....using the value $8.7V/\mu M$ See Early Voltage determination in appendix

Use $L_{PMOS} = 6\mu Meter$

6. PMOS Current mirror Width calculation

In order to minimize the supply voltage required all the MOSFET in the design need to operate in weak inversion. Given:

- $L_{PMOS} = 15\mu Meter$
- $I_{Specific-Square} = 50nA$
- $I_{Drain} = 100nAmp$

$i_f = 1$ is a reasonable value to attain relatively low saturation voltages. This yields: $\sqrt{1+i_f}+3 = 4.4\phi_T$

Thus the width should be set to:

$\frac{100nAmp}{50nAmp} * 6\mu M = 12uM$

It was found during simulation that this held output values in a 15mVolt window over temperature window 0 to 80 degrees and Vsupply = 1.2 to 1.8 with the NMOS FETS sized overly large to eliminate them as a source of output spread.

7. Voltage Follower MOSFET Length

The NMOS voltage follower pair TN1 & TN2 also must act as a current mirror as their source pins are tied to equal voltage nodes. The same voltage change is impressed upon the drains of TN1 & TN2 as was across the PMOS current mirror. Thus they must hold their current balance. See Appendix: “What happens when voltage follower NMOS FETS are too short”.

$V_{Early} = 47.5 Volts$

$L_{NMOS} = 47.5/1.5V/\mu M = 30\mu M$

8.Voltage Follower MOSFET Width

The NMOS MOSFETS need to stay in saturation for the circuit to function over temperature. Use $i_f = 1$ again as with the PMOSFETS.

$L_{NMOS} = 30\mu M$

$W_{NMOS} = \frac{I_D}{I_{Specific-Square}} * L_{NMOS} = \frac{100nA}{250nA} * 30uM = 12uM$ for $i_f = 1$

Simulation: Hand Design Performance

The only values modified from hand calculated values below are the resistor values and diode sizing.

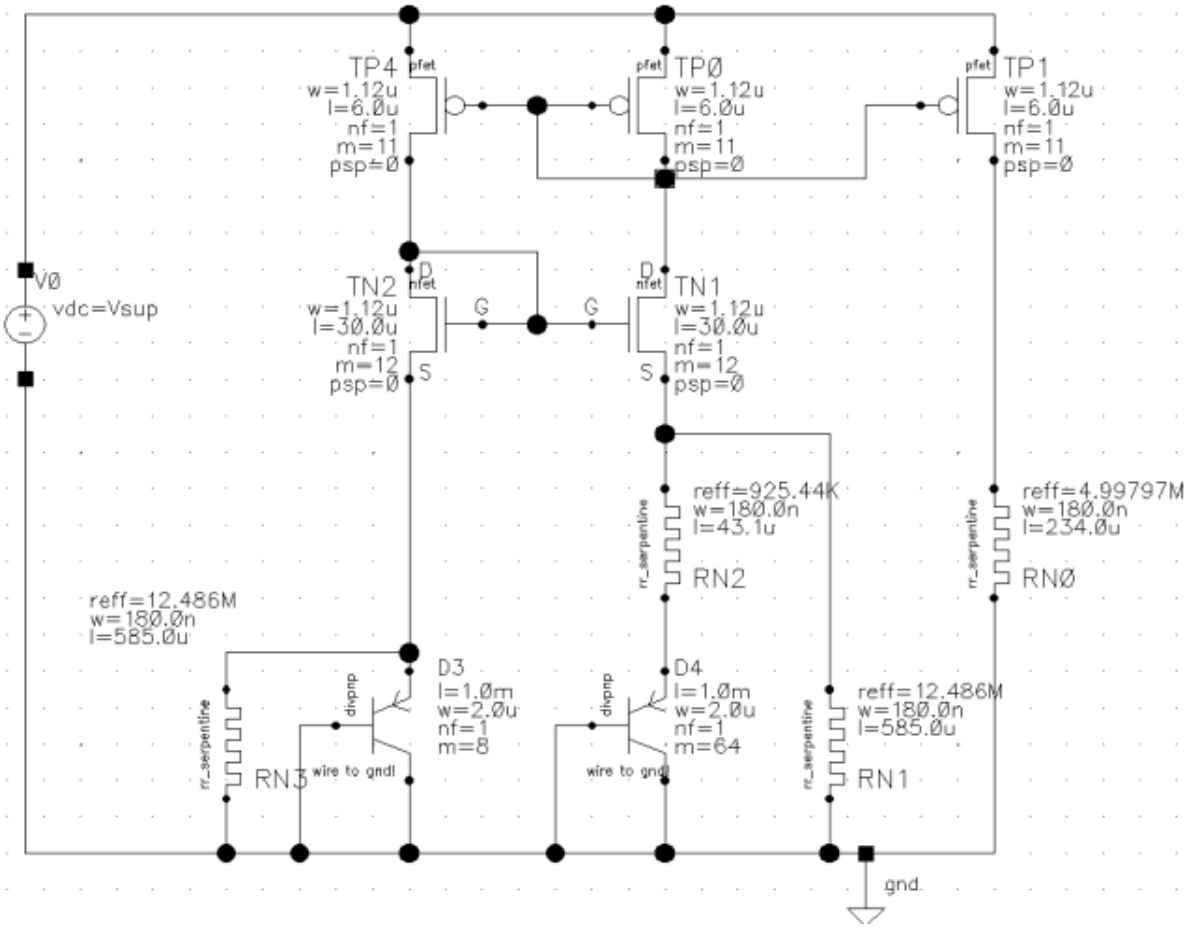
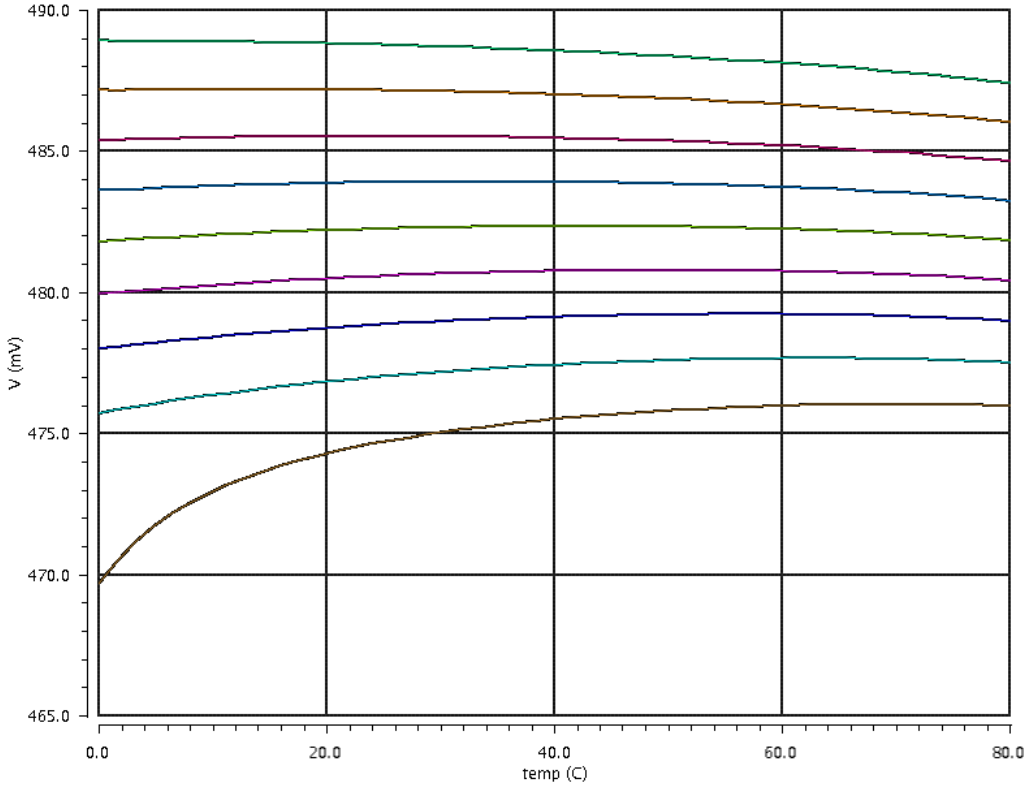


Figure above: All MOSFET are set for nominal $i_f = 1$

Figure below: The following plot is over temperature range of 0 to 80 degrees C and power supply as a parameter V_{SUPPLY}=1.0, 1.1 ....1.8Volts .



Band gap reference output voltage: from lowest curve is $V_{Suppy} = 1.0$ step 0.1 to $1.8V$ for the highest curve

Start Up Circuit

At startup the gates of the current mirror will be close to the positive supply voltage and no current will be flowing in the current mirror TP4/TP0. The gate of the voltage mirror TN2/TN1 will be low and cause TN3 to be off. The gate of TN6 will be high and turn it on causing the PMOS current mirror to be pulled low and turn on the current mirror. As this happens the gate of TN3 will go high and turn on resulting in a low voltage on the gate of TN6 causing it to turn off and leave the band gap reference at the desired operating point

A transient analysis was run to verify stability and check start up time of the circuit.

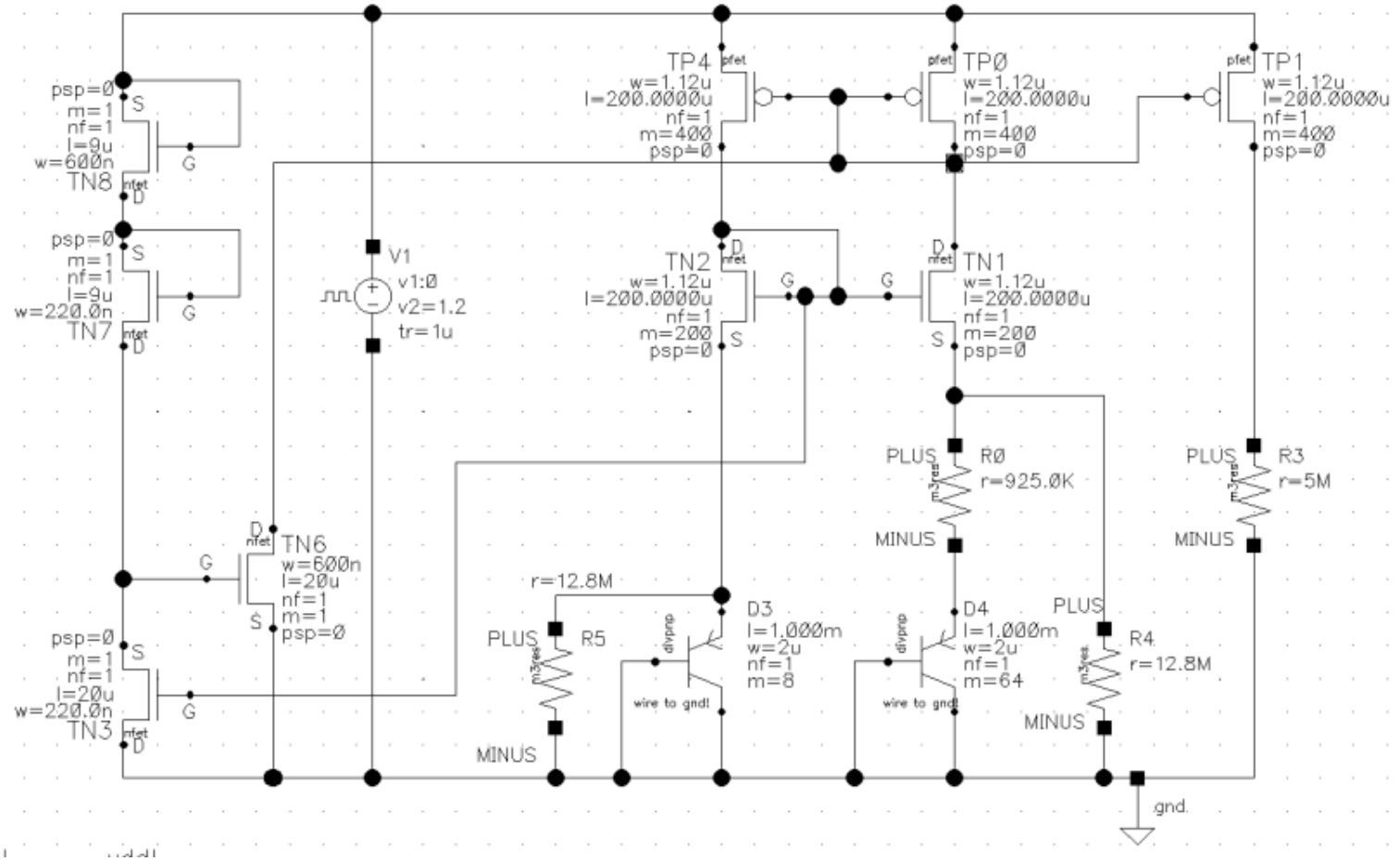


Figure above: Band Gap Reference circuit + StartUp Circuit

Figure: Left: Start Up time without start up circuit - appears to be 4.2 seconds in the worse case. This occurs at Temp=0C

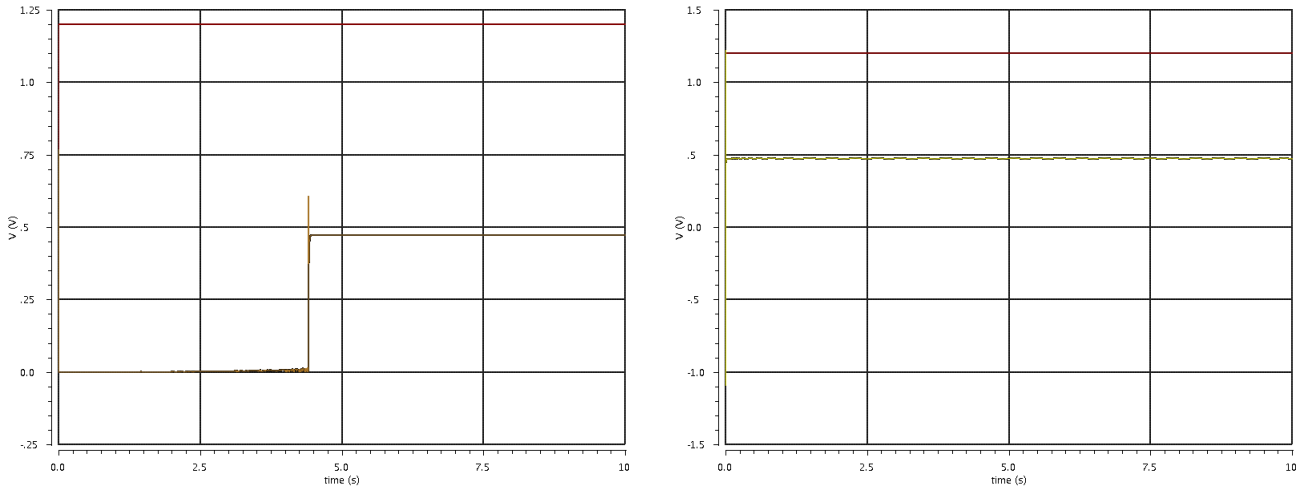
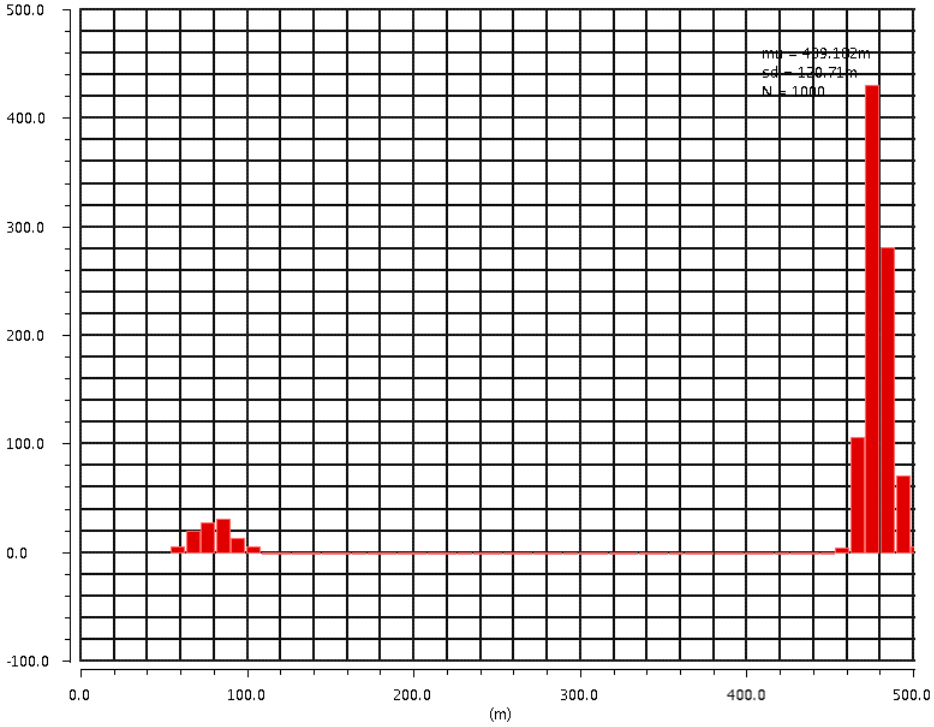


Figure: Right below: BGR with start up circuit. Start up time with start up circuit worst case is 2mSec.

Monte Carlo Analysis

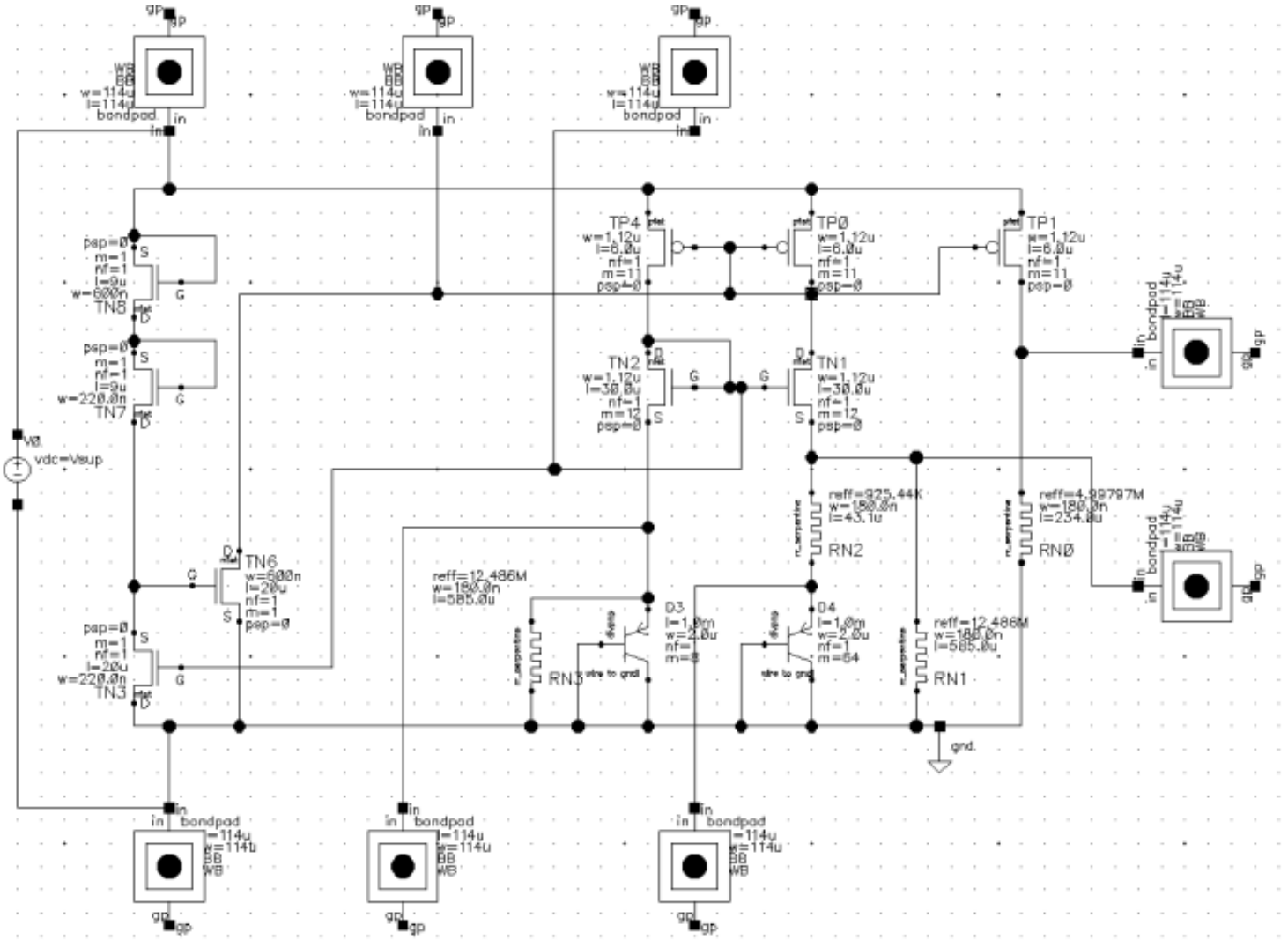
- All components included in the Monte Carlo analysis except the startup circuit.
- N=1000
- Good news: When it works it stays within a 20mV window
- Bad news: It is broken 10% of the time with output values at about 80mV
- There are 5 occurences that are at about 500mV or above.
- Of the "intended group" $\mu = 0.4796 Volts$ and $\sigma = 0.0071 Volts$

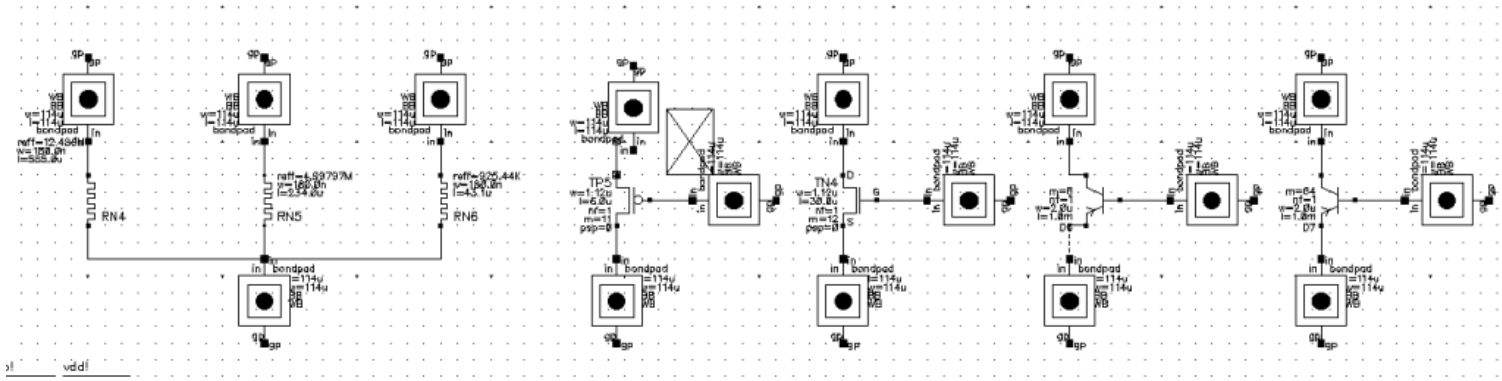


Test and Evaluation Circuit

Equipment required

- Power supply: 1 to 2 volts
- Probe station with volt meter
- Temperature control





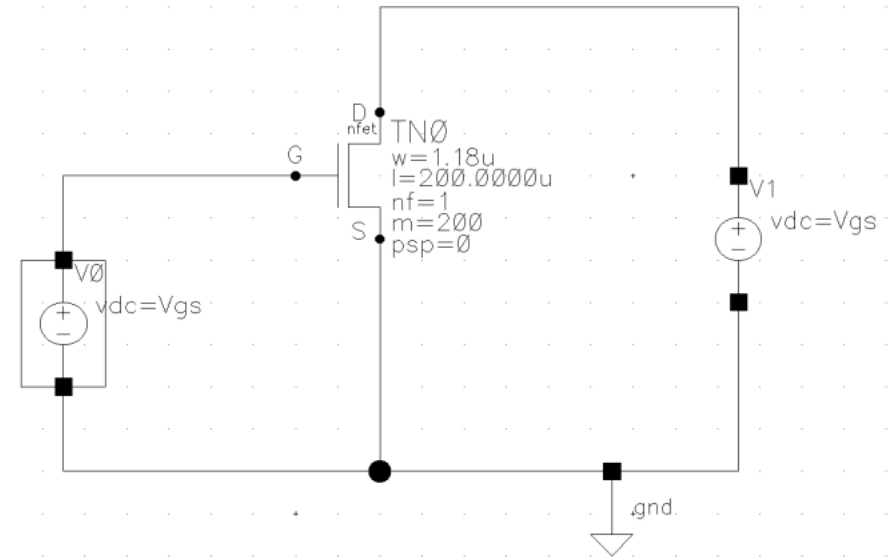
Appendix

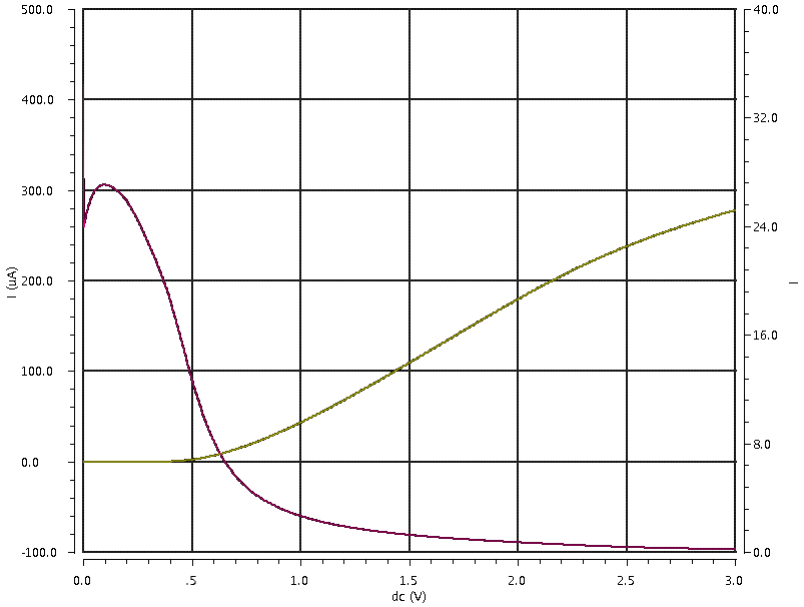
Things to do next

- Write a spreadsheet area calculator to minimize silicon area
- Die size estimate
- Fix the issue that came up in the Monte Carlo simulation
- Process corners. These were quickly tried and discarded in favor of Monte Carlo analysis. This was because the symmetry in the circuit only varied the output voltage characteristic over a small window while Monte Carlo ended up with some "broken" results and was thus much more useful.

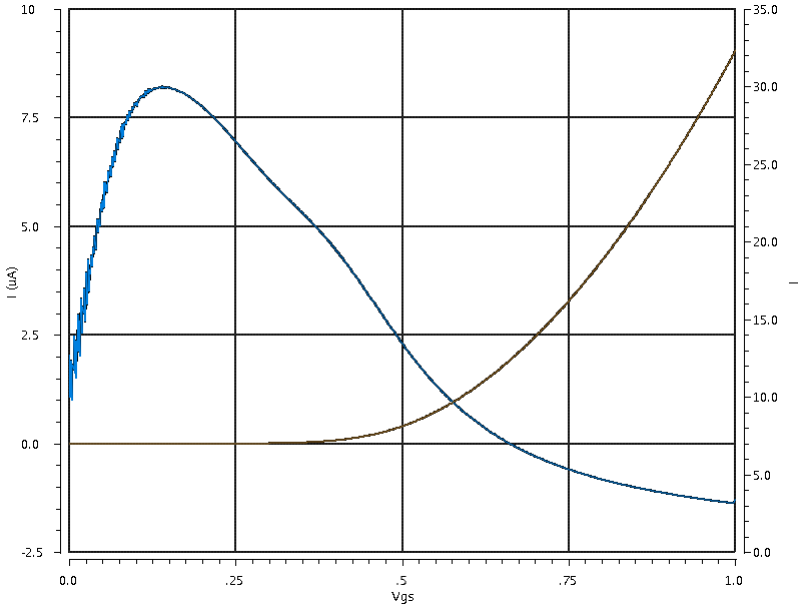
Deriving Specific Current Using Simulation

NMOS Specific Current Simulation: Gate Measurement





NMOS:Ispecific = ~ 0.250 uAmpere with maximum gm/Id = 27 => n=1.48: IBM 7RF process: W= 600nM L=600nM



PMOS: Ispecific = 35nA with max gm/Id=29: IBM 7RF Process: pfet: W=1.18u*200 L=200u

Threshold Voltage versus Temperature Characterization

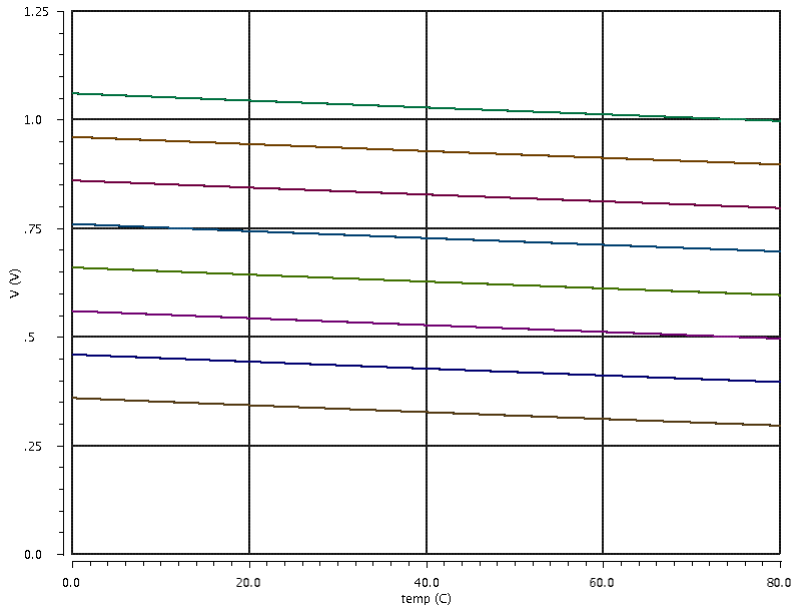


Figure above: NMOS Vt versus Temperature for $Vs = 0$ to 0.7 step 0.1

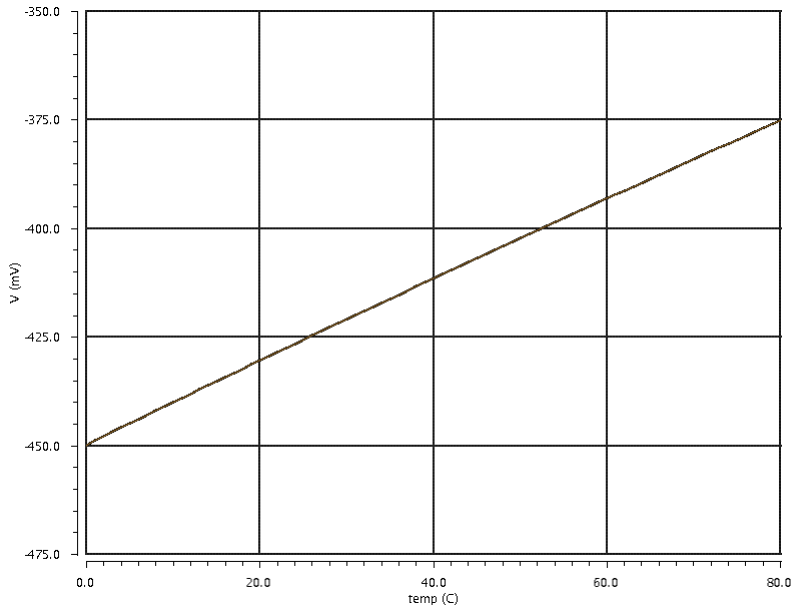


Figure above: PMOS Vt versus temperature for Vs=Vdd

PMOS Early Voltage

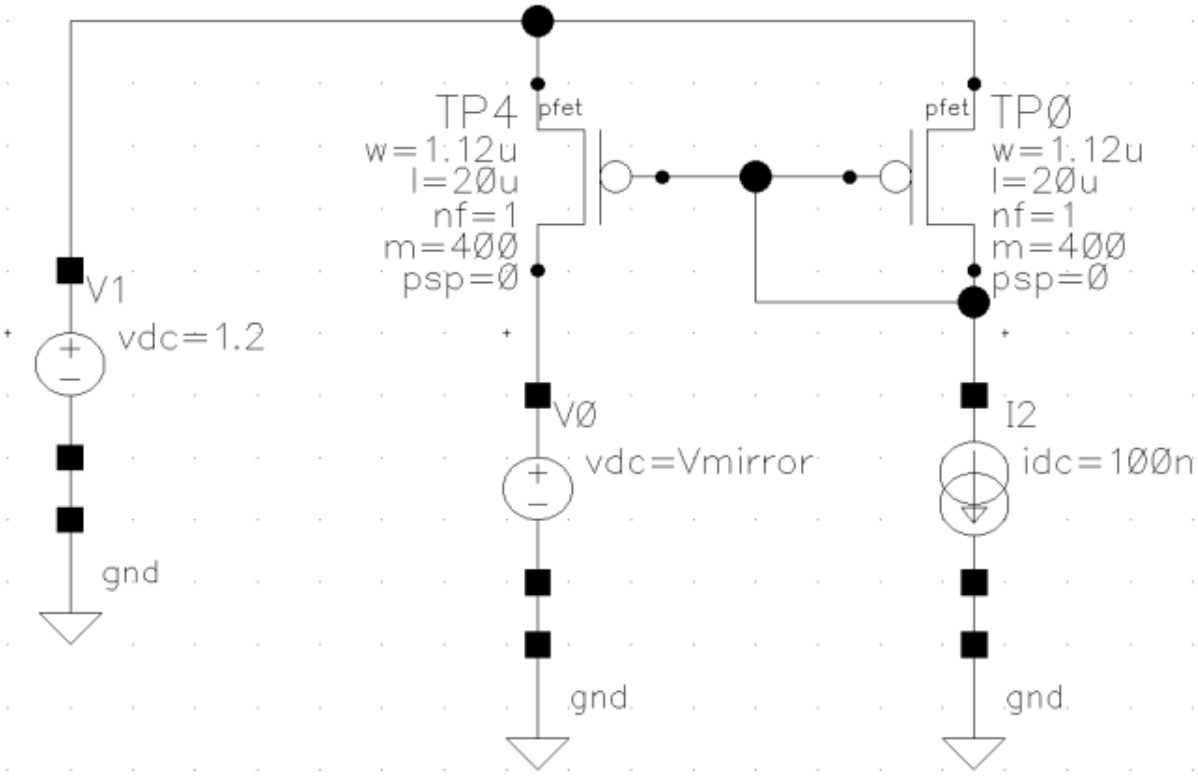


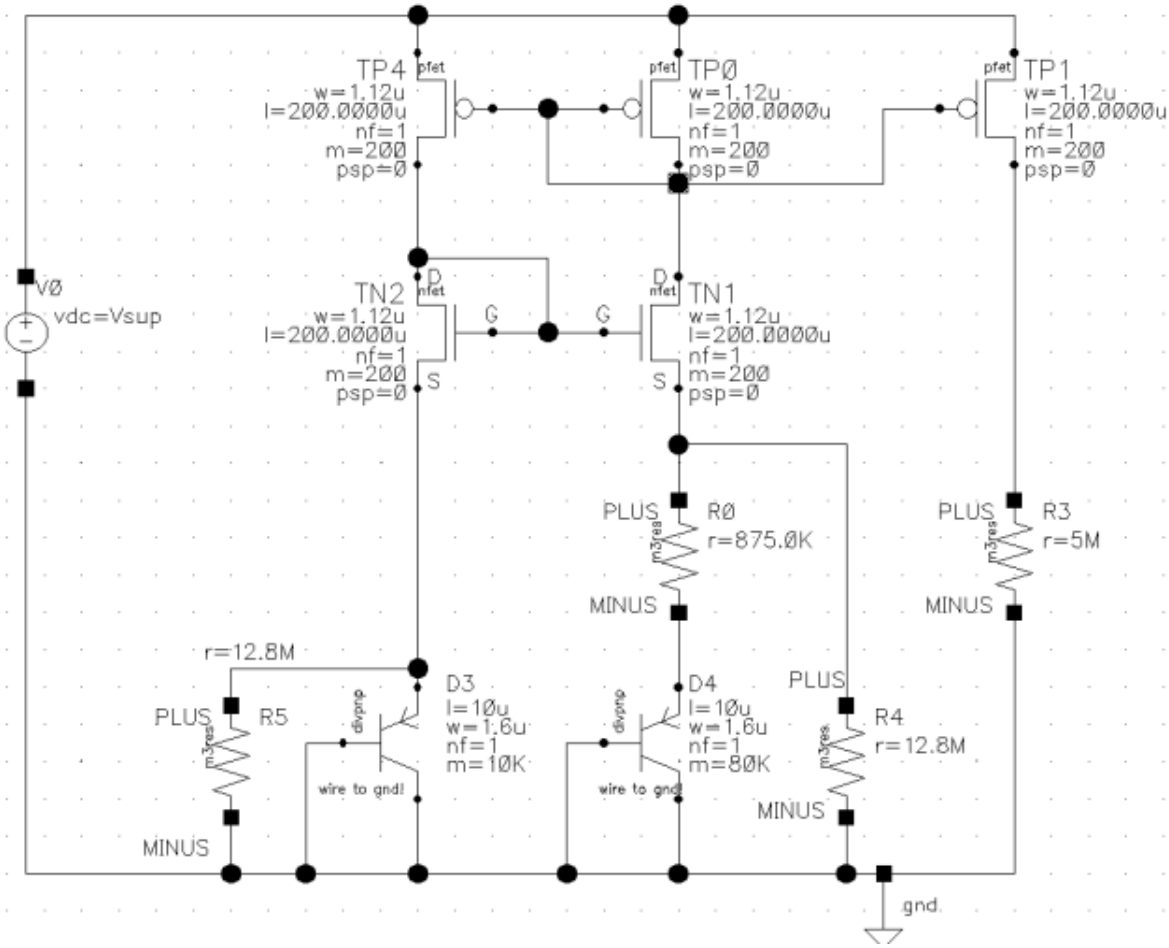
Figure: Early voltage simulation schematic.

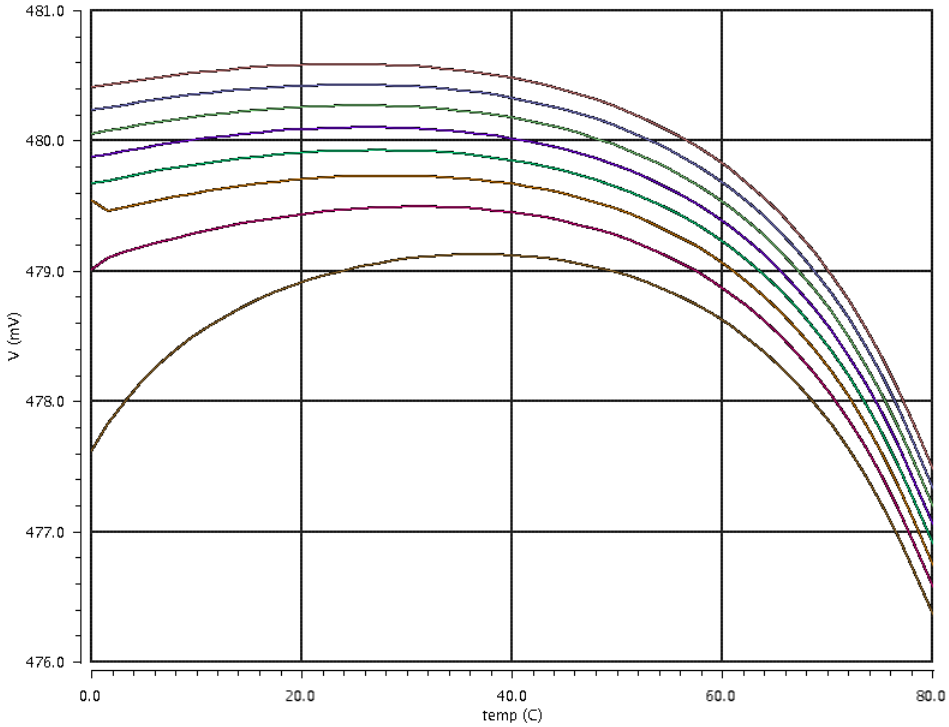
- PMOS Early voltage coefficient simulates at 8.7 Volts per uMeter.
- NMOS Early voltage coefficient simulates at 1.5 Volts per uMeter.

There appears to be a large difference is PMOS and NMOS early voltage coefficient.

How well can the design work?

Hacked together Design with to determine how well the topology can work. Uses gigantic transistors.

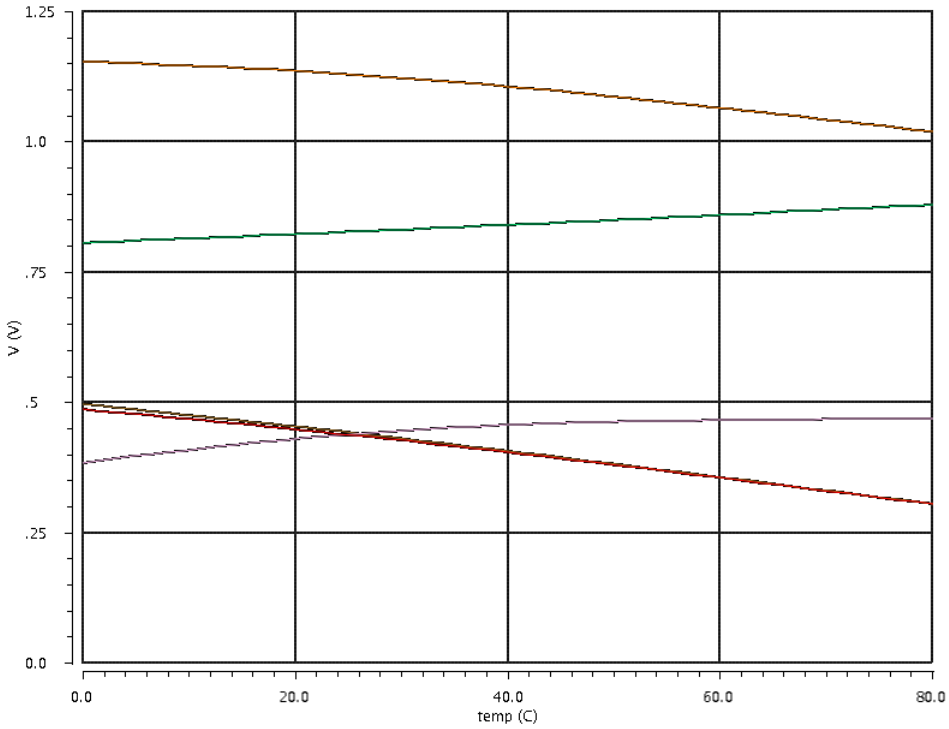




Parametric analysis of first cut of Band Gap Reference with running parameter $V_{Supply} = 1.0V$ to $1.8V$. While this version has a $5mV$ window of operation I am not sure this tight window would remain after a Monte Carlo analysis.

What happens when voltage follower NMOS FETS are too narrow?

Upper left PMOS FET TP4 falls out of saturation at low temperatures. Drain source voltage falls to 50mV



What happens when voltage follower NMOS FETS are too short

When the NMOS FETs are too small they can not hold the voltage on the diode section voltages equal.

- Rising / descending drain voltage causes an increase in NMOS FET current differential.
- Length must be enough to provide g0 that allows 1nAmp or less change in current with the attendent change in drain voltage.