An Inductorless DC–DC Converter for Energy Harvesting With a 1.2-μW Bandgap-Referenced Output Controller

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***Abstract*—We present a fully integrated dc–dc converter for micropower energy harvesting. A 1.2-μW bandgap-referenced output controller provides output regulation at 1.4 V, achieving quiescent power of 3 μW and a maximum overall efficiency of 58% at 11 μW output power. A modified four-phase charge pump provides a 3$\times$ voltage boost and a minimum input voltage of 270 mV in free-running mode. Using dual switches driven from both the converter input and output, the chip achieves boost without external excitation or external components.**

***Index Terms*—Boost converter, charge pump (CP), dc–dc converter, energy harvesting, regulator.**

I. Introduction

WEARABLE or implantable low-power electronics such as active contact lenses [1] or intraocular pressure sensors [2] require an exceedingly small-form factor and cannot tolerate surface mount components or standard batteries. Photovoltaic (PV) energy naturally exists in the human daily environment (0.1 mW/cm^2 $\sim$ 100 mW/cm^2) [3], which can be harvested with miniature photodiodes or flexible thin-film PV cells to eliminate the need for batteries. Their output voltage levels are usually small (300 mV $\sim$ 600 mV). While this low voltage level is acceptable and possibly beneficial for low-power digital operation, it is lower and much less stable than the supply voltage required for analog subsections of the chip (usually at least 1 V regulated). Therefore, a regulated dc–dc step-up converter is needed. For extremely volume-constrained batteryless applications, the output of the dc–dc converter directly powers the chip without any significant energy storage. Thus, the converter must start-up from the input voltage without other electrical or mechanical assist to broaden its applicability. Additionally, the converter must exhibit a very low quiescent power to achieve high system efficiency for ultralow power wearable sensors, of which the active power consumption can be as low as a few microwatts [1], [2].

In this paper, we present a fully integrated low quiescent power dc–dc converter for wearable sensors using PV energy harvesting. Its block diagram is shown in Fig. 1. A design methodology for a size-constrained PV energy harvesting charge pump (CP) is also presented. Due to the unavailability of external energy storage in a miniaturized system, we cannot rely on an external "start-up" mechanism or energy reservoir. Therefore, one main objective of this work is to lower the threshold input power (or the start-up voltage) for a given output load, rather than tracking the maximum power point of the PV cell under different light conditions. The proposed circuit exhibits a free-running start-up voltage of 270 mV to achieve 3$\times$ voltage boost with a 1-MΩ load. A 1.2-μW controller provides output regulation at 1.4 V. The quiescent power of the proposed dc–dc converter is less than 3 μW, making it suitable for ultralow power battery-free electronics using energy harvesting.

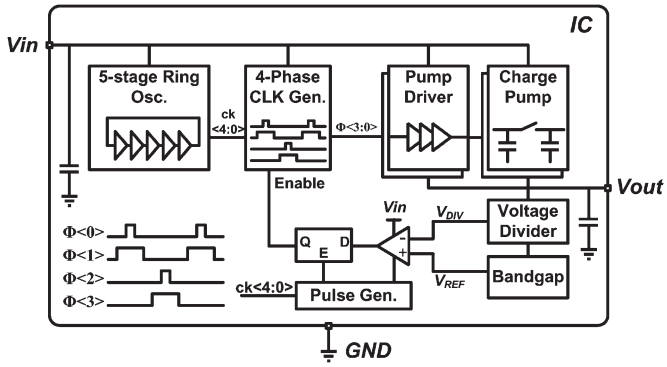

Fig. 1. Block diagram of the IC. The pumping circuitry is directly powered from the input voltage, and the converter requires no off-chip components.

II. Prior Art

There are two basic types of dc–dc converters, namely, inductive boost converters and switched capacitor converters. Inductor-based boost converters can achieve very low input voltages and high efficiencies [4] but usually require an off-chip inductor in the micro-Henry range. The associated size penalty prohibits this type of converters to be used in certain applications with extreme size constraints. Thus, for fully integrated dc/dc converters, capacitive CPs are preferred. A previously published work on capacitive micropower converters was designed for battery recharging applications and depends on the constantly available high voltage of the battery for start-up [5]. Postfabrication Vth trimming is also proposed to achieve 95 mV input voltage operation, using an SC pump to kick-start a boost converter [6], which requires an external inductor and capacitor. The SC pump itself in [6] is designed to kick-start a boost converter at around 0.5 V, which is lower than the supply

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of many analog and RF circuits. While the hybrid system (CP + boost converter) achieves a free-running output efficiency of 72% with more than 1 mW of output power, the efficiency and the quiescent power of the CP alone are not reported. In [7] and [8], integrated PV cells are used to charge an external battery/capacitor for duty-cycled operation. In contrast, our work aims for applications where the system is powered directly and solely from the PV cells without significant energy storage.

For size-constrained low-power wearable sensor applications, low quiescent power is important, particularly with low output power levels. Thus, this paper proposes a standalone CP dc/dc converter that can directly power wearable electronics with high efficiency at low output power levels.

III. Architecture and Circuit Design

The impetus for this work is a micropower wireless sensing system integrated on a flexible biocompatible substrate. Thus, our objective is to design a fully integrated dc–dc converter to supply a regulated voltage higher than 1 V and an output current of up to 5 μA, while exhibiting a chip area smaller than 0.5 mm^2. This size will allow space for other circuitry and meet the practical constraint of the standard incision size ($\sim$1.6 mm) for an implantable intraocular device [2].

A. Architecture

Fig. 1 shows the block diagram of our CP IC. We use the unboosted Vdd to directly power the pump clock and the four-phase CPs, eliminating the need for an external start-up voltage. A five-stage current-starved ring oscillator generates five phases ($\mathrm{ck}_{\langle 4:0\rangle}$), which, in turn, generate nonoverlapping four-phase clocks ($\varphi_{\langle 3:0\rangle}$). Two identical CP branches clocked 180° out of phase drive an on-chip 500-pF output capacitor to reduce ripple. On-chip test registers can be used to reconfigure the oscillation frequency for source–load matching for a given load current and to accommodate different photodiode technologies.

Output regulation is achieved using skip mode to decrease switching dissipation for light loads. The scaled output voltage is compared with an on-chip bandgap reference and gates the four-phase pumping clock, thus providing output regulation. This regulation allows looser power-supply rejection ratio (PSRR) requirements in the subsequent circuits and increases device reliability by avoiding excessive high voltage at the output under high input voltages. This on-demand pumping scheme sources current from the power source to the pump only when needed, lowering the average current consumption. A latch-type comparator is used to avoid static current consumption and save power. Again, the latch comparator is powered from the input voltage for accurate comparison at different V_{out} during start-up. A gated latch is used to synchronize the comparison result to the system clock.

B. Number of Pump Stages

A PV cell presents a relatively unstable supply voltage to a dc/dc converter. The input voltage depends on the photo current generated by the PV cell, the $I-V$ characteristic of the PV cell, and the current draw of the converter. Therefore, the CP optimization approach is different from the traditional methods

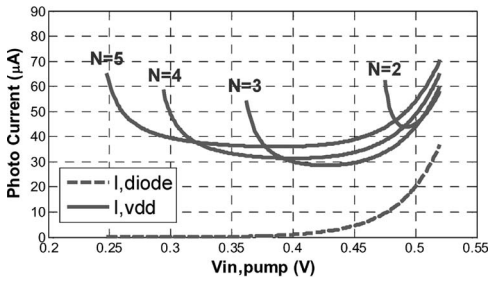

Fig. 2. Required photo current for different number of CP stages.

[9], where the input of the CP is often considered an ideal voltage source. Thus, we model the characteristics of the PV cell and the CP together to find the optimal number of stages and the corresponding operating point.

In steady state, the photo current generated by the PV cell, I_{photo}, supplies the forward bias current of the PV cell itself, I_{diode}, and the input current to the CP, I_{cp}. The expression of I_{cp} as (1) is given in [9], where I_{LOAD} is the load current to the CP, N is the number of stages, and V_{in} and V_{out} are the input and output of the CP, respectively. The parameter α is the ratio between the bottom-plate parasitic capacitance to the nominal capacitance value of the pumping capacitors. It is about 3% in the process we use. It plays little role in optimizing N but has a significant influence on the resulting pump efficiency.

Together with the PV cell $I-V$ curve as (2), one can determine the minimum required photo current for a given number of CP stages, CP output current, and output voltage. In (2), V_T is the thermal voltage, η is the nonideality factor of the PV cell, and I_S is the saturation current. Thus

$$I_{\mathrm{cp}} = I_{\mathrm{LOAD}}\left[(N+1)+\alpha\frac{N^2V_{\mathrm{in}}}{(N+1)V_{\mathrm{in}}-V_{\mathrm{out}}}\right)\Bigg] \quad (1)$$

$$I_{\mathrm{photo}} = I_{\mathrm{diode}} + I_{\mathrm{cp}} = I_S e^{\frac{V_{\mathrm{in}}}{\eta V_T}} + I_{\mathrm{cp}}. \quad (2)$$

Numerical analysis is used to find the optimal number of stages given our CP specification and the PV cell characteristics. The target output current load is 5 μA, and the output voltage is 1.4 V. This will allow enough headroom for a 1.2-V bandgap reference while delivering enough power to the regulation circuitry and our target wireless sensor system. It is shown in Fig. 2 that the theoretical minimum photo current can be achieved with a CP of three stages. The corresponding optimal input voltage is between 0.4 and 0.45 V.

C. Capacitor Size and Clock Frequency

Next, the pumping capacitor size and clock frequency must be determined. To achieve high conversion efficiency, the pumping capacitor size is maximized for the available area (thus minimizing the clock frequency for a given load current) to reduce the switching loss associated with charging and discharging the switch capacitance. It is shown in [9] that total pumping capacitance C_{total} is a function of the number of stages N, load current I_{LOAD}, clock frequency f, input voltage V_{in}, and output voltage V_{out}, assuming ideal charge transfer switches (CTS), i.e.,

$$C_{\mathrm{total}} = NC_P = \frac{I_{\mathrm{LOAD}}}{f}\frac{N^2}{(N+1)V_{\mathrm{in}}-V_{\mathrm{out}}}. \quad (3)$$

Additionally, sufficient output bypass capacitance must be integrated on chip to reduce the output ripple. The size of the required output capacitance $C_{\rm out}$ is proportional to the load current and inversely proportional to the clocking frequency and ripple tolerance $V_{\rm ripple}$. It can be expressed as $C_{\rm out} > I_{\rm LOAD}/(f \cdot V_{\rm ripple})$ in steady state. Inserting the inequality into (3), we find

$$C_{\rm out} > \frac{C_{\rm total}}{V_{\rm ripple}} \frac{(N+1)V_{\rm in} - V_{\rm out}}{N^2}. \tag{4}$$

The pumping and output capacitors share a total area budget, which is the total chip area excluding the control circuit, the switches, and the switch drivers. This sets a constraint on the inequality (4)

$$\frac{C_{\rm out}}{C_{a,1}} + \frac{C_{\rm total}}{C_{a,2}} < \text{Area} \tag{5}$$

where $C_{a,1}$ and $C_{a,2}$ are the capacitance densities of $C_{\rm out}$ and $C_{\rm total}$, respectively. The parameters $C_{a,1}$ and $C_{a,2}$ depend on the different types of capacitors used. For $C_{\rm total}$, low bottom-plate parasitic capacitors such as metal–insulator–metal (MIM) capacitors are preferred, whereas for $C_{\rm out}$, higher density capacitors such as stacked MOS and MIM capacitors can be used. For our process, $C_{a,1}$ is 4 fF/μm^2, and $C_{a,2}$ is 7.5 fF/μm^2. Solving (3) and (4) with a total area of 0.1 mm^2, ripple tolerance of 15 mV, and $V_{\rm in}$ of 450 mV, $C_{\rm total}$ is calculated to be 150 pF, and $C_{\rm out}$ is 450 pF. To allow design margin, we choose $C_{\rm out}$ to be 500 pF. Most wireless sensors incorporate an internal linear regulator for the internal supply regulation [1], [2], [10]. Assuming a pessimistic 40-dB PSRR specification of a linear regulator, a 15-mV ripple on the CP output results in a 0.15-mV output ripple. This can be well tolerated in low to medium resolution data converters.

With the pumping capacitor size and the desired output current, we can calculate the clock frequency to be 750 kHz using (3). We choose a nominal clock frequency of 800 kHz and design the clock frequency to be configurable between 600 kHz and 1 MHz to accommodate different power requirements and different PV cell technologies. Considering source–load matching between the PV cell and the pump for a given load condition, the optimal input voltage to achieve a minimum required light level can be found using the numerical analysis in Section III-B. Once the optimal $V_{\rm in}$ is known, the clock frequency can be configured accordingly based on (3).

In summary, the above analysis concludes that the clock frequency should be around 800 kHz, and the number of stages is 3 (50 pF per stage). This gives a theoretical 5-μA CP output current with input and output voltages of 0.45 and 1.4 V, respectively.

D. Charge Pump

Fig. 3 shows a simplified schematic of the CP circuit. Each stage comprises two CTS's formed by nFETs (M_{A^*}) and CMOS pass-gate switches (S_*), where $*$ is $1 \sim 4$. These dual CTS's are driven by the boosted voltage and output voltage from the input, respectively. Zero- and low-Vth ($\sim$250 mV) transistors are used to facilitate low voltage operation. Components M_{A^*}, M_{B^*}, and C_{P^*} form a four-phase Dickson

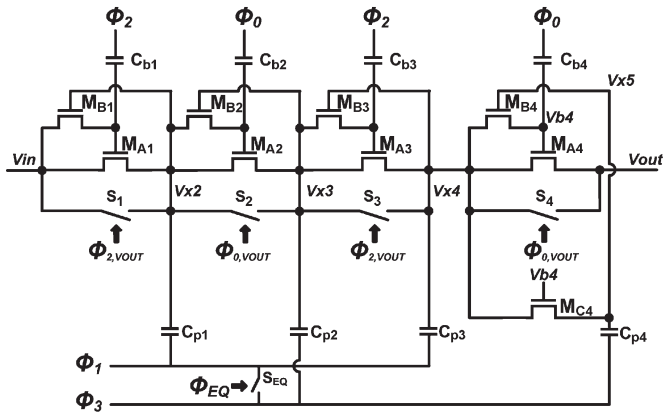

Fig. 3. Simplified schematic of the four-phase CP.

CP cell [11] to reduce the back current in their two-phase counterparts. The boosted gate swings of M_{A^*} are limited by the input voltage level to about 0.9 $V_{\rm in}$. At low supply voltages (where the clock swing approaches the transistor threshold voltage), charge transfer becomes less efficient due to the poor on/off ratio of the pass transistors M_{A^*}. Simply upsizing the M_{A^*} would increase the back current and the switching loss, degrading the overall efficiency.

Instead, we employ auxiliary switches S_* clocked with $\varphi_{1,\rm vout}/\varphi_{3,\rm vout}$, which are in-phase with φ_1/φ_3 but with a voltage swing of $V_{\rm out}$. These switches function more effectively under higher voltage swing (high $V_{\rm out}$). Although these S_* switches are less efficient at low $V_{\rm out}$ during start-up, the boosted switches M_{A^*} provide the necessary pumping current to raise $V_{\rm out}$ before S_* functions. The OR combination of the two switches optimizes charge transfer operation at different output voltage levels, thus improving conversion efficiency while achieving a low start-up voltage.

Fig. 4 shows the simulated average output current of the bootstrap transistor M_{A1} (zero-Vth) and $V_{\rm out}$-driven switch S_1 (low-Vth) with input voltages of 270 and 400 mV. It can be seen that, at low output voltages ($<$ 0.6 V), the $V_{\rm out}$-driven CTS transfers much less current compared with the bootstrap CTS. On the contrary, at higher voltages, the $V_{\rm out}$-driven CTS's become more effective and contribute to the majority of the pumping current. The combined CTS's thus achieve better overall efficiency at different levels of the output voltage compared with either the bootstrap CTS or the $V_{\rm out}$-driven one alone.

In this design, $C_{P1\sim3}$ are 25 pF, and C_{P4} is 400 fF in both of the two 180° out of phase CP branches. The CP cell in the last stage uses a small amount of charge to provide a boosted voltage on V_{b4} to eliminate the voltage drop in the output stage. In addition, charge recycling for pump capacitor bottom plates with switch $S_{\rm EQ}$ [12] further contributes to a measured 1.6% efficiency improvement

E. Output Voltage Controller

Fig. 5 shows the schematic of the output control circuit and the latch comparator. At the rising edge of Latch_1, derived from the system clock, a scaled output of the CP, $V_{\rm DIV} = \beta \cdot V_{\rm out}$, is compared with the bandgap reference voltage to gate the pump clock $\varphi_{\langle 3:0\rangle}$. The divide ratio of the voltage divider is denoted as β. Thus, $V_{\rm out}$ is regulated to $V_{\rm ref}/\beta$ through this

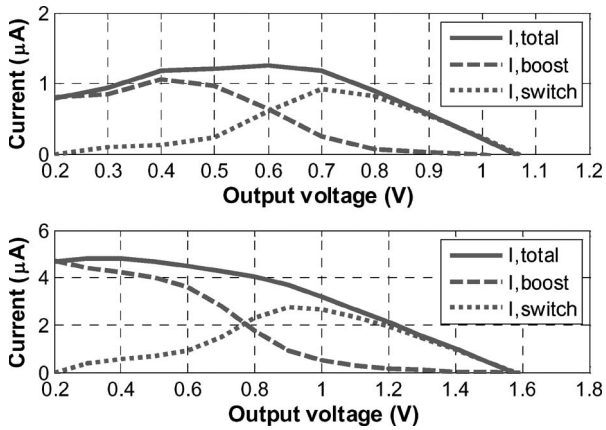

Fig. 4. Simulated pumping current contribution of the two switches. (Top) $V_{\rm in} = 270$ mV. (Bottom) $V_{\rm in} = 400$ mV.

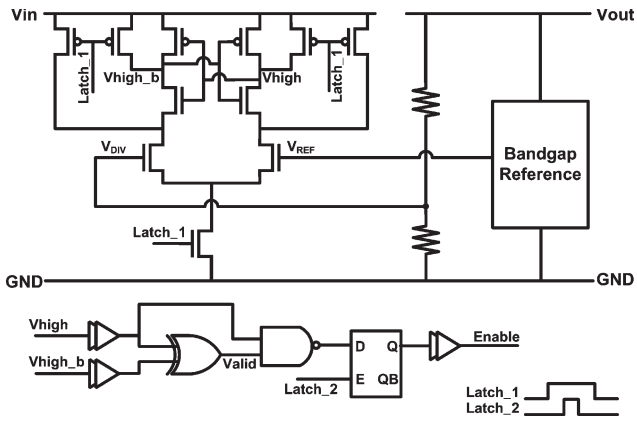

Fig. 5. Output voltage controller.

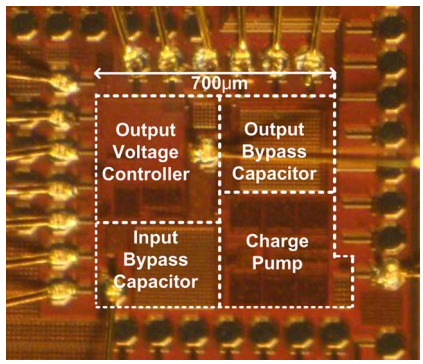

Fig. 6. Die photo.

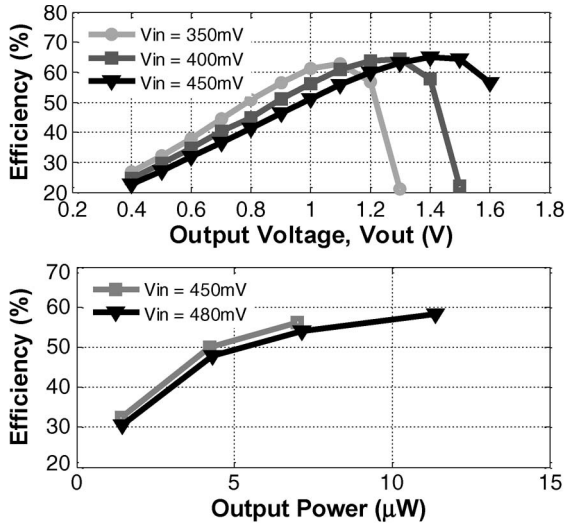

Fig. 7. Conversion efficiency at different input voltages in (top) free-running and (bottom) regulation modes.

feedback mechanism. The use of a resistive divider results in a more stable RC time constant at different $V_{\rm out}$ levels compared with a MOSFET divider. The comparison result is latched on the falling edge of Latch_2 until next comparison. The detailed implementation of the bandgap circuit can be found in [10].

The scaled output voltage $V_{\rm DIV}$ and the bandgap reference voltage $V_{\rm REF}$ are fed to the input nFET pair of the latch comparator. All the transistors in the latch comparator are either low- or zero-Vth transistors for low voltage operation except for the input nFET pair. High-Vth 3.3-V I/O nFETs are used for the input pair to accommodate higher input levels around 1.2 V despite the low supply voltage $V_{\rm in}$.

When $V_{\rm out}$ rises from zero during start-up, both $V_{\rm ref}$ and $V_{\rm div}$ are low, and the latch comparator cannot resolve in time before the falling edge of Latch_2. Therefore, an XOR operator is used to gate the comparator output. When the differential output of the comparator fails to swing to the opposite rails, the comparison result is bypassed, and the pump is kept enabled. This ensures correct pump control for a wide range of $V_{\rm out}$, even when $V_{\rm out}$ is very low.

IV. Results

A prototype chip was designed and fabricated in an IBM 0.13-μm CMOS process. Fig. 6 shows a die photograph. The chip measures 0.42 mm^2 in active area, including two 500-pF on-chip input and output filtering capacitors.

Fig. 7 shows the measured conversion efficiency of the CP in free-running mode and in regulation mode with ideal voltage sources. In free-running mode, the pump is not gated and runs at 100% duty cycle with a regulation circuitry controller disabled (bandgap reference, voltage divider, and comparator). A maximum free-running efficiency of 65% was measured.

In regulation mode, the measured maximum overall efficiency is 58% at an output power of 11 μW. At higher output power levels, the power consumption in the control circuitry becomes negligible, and the overall efficiency approaches the free-running efficiency. The pump can source up to 5 μA to the load in regulation mode at an input of 450 mV. The bandgap reference, voltage divider, and latch comparator have a measured total power consumption of 1.2 μW. Together with the power consumption of the on-chip clock and pump drivers, the measured quiescent power is less than 3 μW with input voltages of up to 0.5 V. Table I shows the simulated quiescent power consumption in each circuit block at a 450-mV input.

With a 10% variation around an input voltage of 450 mV, the output is regulated to 1.4 V within 23 mV variation (1.6%). Low dropout linear regulators with a relaxed 40-dB PSRR specification can be used to further stabilize the output. This will result in a 0.23-mV output variation, exceeding the supply requirement of many analog circuits.

The converter starts up in free-running mode with a measured input voltage of 270 mV while providing 3$\times$ voltage boost.

TABLE I
QUIESCENT POWER CONSUMPTION AT 450 mV

Circuit Block	Power
Ring oscillator	248nW
Clock Generator†	136nW
Pump Driver†	1617nW
Charge Pump†	377nW
Comparator†	175nW
Band-gap*	648nW
Voltage Divider*	335nW
Total (Simulated)	2.55μW
Total (Measured)	2.62μW

† Circuit blocks partially gated by the output controller
* Powered from the charge pump output – already accounted for by the Pump Driver/Charge Pump

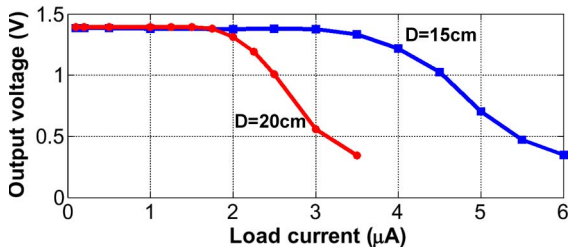

Fig. 8. Output voltage using a single 1.21-mm^2 photodiode at 15 and 20 cm away from a 60-W light bulb.

This result shows sufficient start-up voltage margin considering transistor threshold voltage process variations. The low start-up voltage characteristic also makes this chip useful for boost converter kick-start applications similar to those in [6] or battery recharging circuits in cases when a battery is present in the system but is depleted.

To test indoor PV energy harvesting, we connected our chip to a 1.21-mm^2-active-area silicon photodiode (S2836-18 K, Hamamatsu). When illuminated with a 60-W incandescent light bulb 15 cm away (roughly 7× less intensity than that of direct sunlight), our energy harvester provides a regulated 1.4 V while delivering up to 4 μW of power (see Fig. 8). The corresponding PV cell output voltages range from 420 to 470 mV, depending on the load current. The output power provided by the energy harvester is enough to power wearable electronics such as [1] and [2].

Table II shows a performance summary and comparison of our designed CP. To the authors' knowledge, this is the first reported fully integrated self-starting regulated dc–dc upconverter to allow sub-10 μW energy harvesting down to 400 mV

V. CONCLUSION

We present an autonomous fully integrated capacitive dc–dc converter using a modified four-phase CP. In free-running mode, this fully integrated CP circuit can provide 3× voltage multiplication while autonomously starting up at an input voltage down to 270 mV without any external excitation. An on-chip 1.2-μW skip mode output controller provides output regulation at 1.4 V, achieving a maximum overall efficiency of 58%. The chip exhibits a 3-μW quiescent power and a volume of 0.33 mm^3, including test pads and excluding the volume occupied by other designs shared in the same test chip. The converter can be applied for energy harvesting with PV cells or in general with other dc energy sources such as microscale thermoelectric generators. Without using any external components, this sub-cubic-millimeter dc–dc converter is suitable for micropower energy harvesting applications with stringent size constraints.

TABLE II
PERFORMANCE SUMMARY

	[4]	[6]	[5]	This work
Process	0.13μm	65nm	0.35μm	0.13μm
Die size	1.6mm^2	0.17 mm^2	59mm^2	0.42 mm^2
External excitation for start-up	Yes (vibration)	No	Yes (2V buffer)	Not needed
External components	MEMS switch, inductor, capacitor	Inductor, Capacitor	Not needed	Not needed
Start-up voltage	35mV	95mV	500mV	270mV (unregulated) 400mV (regulated)
Output regulation	1.8V	No	No	1.4V
Max unregulated efficiency	n/a	72%	70%	65%
Max regulated efficiency	58%	n/a	n/a	58%

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