speed of such PLA's would exceed the speed of bipolar PLA's commonly on the market, but at the same time have a higher density and draw much less current.


## ACKNOWLEDGMENT

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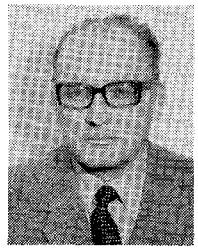

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# On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique

JOHN F. DICKSON


*Abstract*—**An improved voltage multiplier technique has been developed for generating +40 V internally in p-channel MNOS integrated circuits to enable them to be operated from standard +5- and −12-V supply rails. With this technique, the multiplication efficiency and current driving capability are both independent of the number of multiplier stages. A mathematical model and simple equivalent circuit have been developed for the multiplier and the predicted performance agrees well with measured results.**

**A multiplier has already been incorporated into a TTL compatible nonvolatile quad-latch, in which it occupies a chip area of 600 μm × 240 μm. It is operated with a clock frequency of 1 MHz and can supply a maximum load current of about 10 μA. The output impedance is 3.2 MΩ.**


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## INTRODUCTION

ALTHOUGH MNOS technology is now well established for fabricating nonvolatile memory circuits, the relatively high potentials necessary to write or erase information, typically 30–40 V, are an obvious disadvantage. In many applications, the need to generate these voltages has prevented the use of MNOS devices being economically viable, especially when only a few bits of nonvolatile data are required. To overcome this problem, a method of on-chip high-voltage generation using a new voltage multiplier technique has been developed, enabling MNOS circuits to be operated with standard

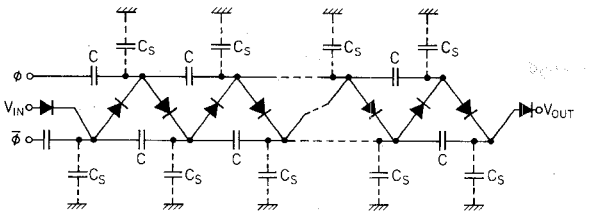


Fig. 1. Basic Cockcroft-Walton voltage multiplier. Usually implemented with discrete components such that $C >> C_S$.

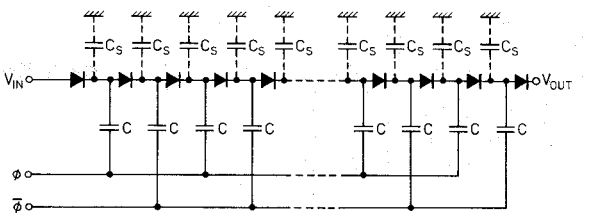


Fig. 2. Improved voltage multiplier configuration. In monolithic form, $C > C_S > 0.1C$, typically.

supplies and interfaces. The technique has already been demonstrated to be practical in a nonvolatile quad-latch circuit and is currently being designed as standard in a range of nonvolatile memory products.

## Multiplier Technique

In principle, voltages higher than that of the power supply can be generated in an integrated circuit using a Cockcroft-Walton multiplier similar to that shown in Fig. 1. Its operation is well known and will not be described in detail here, except to note that since the coupling capacitors are connected serially, the following comments apply.

1) Efficient multiplication will occur only if the coupling capacitors, $C$, are much greater than the stray capacitors, $C_S$.

2) The output impedance increases rapidly with the number of multiplying stages.

Historically, the Cockcroft-Walton multiplier [1] has been used to generate voltages greater than those which could be easily handled by electromagnetic transformers. This is possible since the maximum voltage across any of the coupling capacitors is only equal to the input drive voltage, irrespective of the number of multiplying stages. In this type of application, however, the circuit is implemented with discrete components, so that the coupling capacitors can be made sufficiently large for efficient multiplication and adequate drive capability.

This type of multiplier does not, however, lend itself to integration in monolithic form since in practice, on-chip capacitors are limited to a few picofarads with relatively high values of stray capacitance to substrate. A generalized analysis of the Cockcroft-Walton multiplier taking stray capacitance into account is extremely complex and will not be given here, but it is found that in practice it is difficult to generate voltages significantly greater than twice the supply voltage, irrespective of the number of multiplying stages. In fact, if the number of stages is increased beyond a critical number (typically, 3 or 4), determined by the ratio of $C$ and $C_S$, the output voltage actually decreases due to voltage drops in the diode chain.

In order to overcome these limitations, the voltage multiplier circuit shown in Fig. 2 was devised. It operates in a similar manner to the classical Cockcroft-Walton multiplier and can be shown to be an equivalent circuit. However, the nodes of diode chain are coupled to the inputs via capacitors in parallel instead of in series, so that the capacitors have to withstand the full voltages developed along the chain. This is not a problem here, provided that the integrated circuit process limits are not exceeded. As will be shown, the advantages of this configuration are that efficient multiplication can be achieved with relatively high values of stray capacitance, and that the current drive capability is independent of the number of multiplier stages.

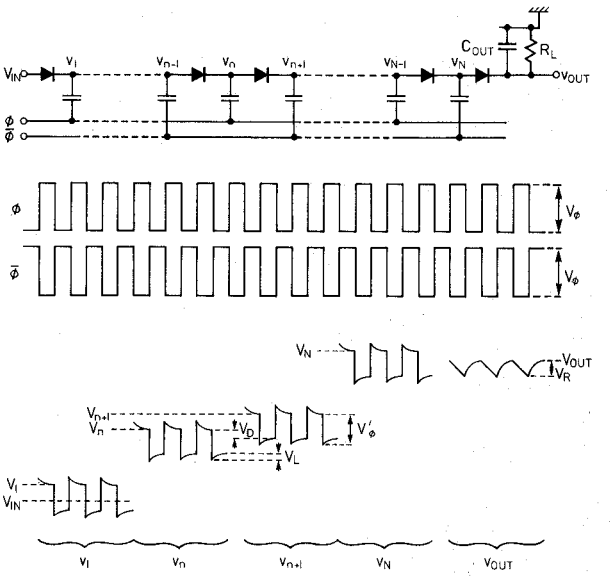


Fig. 3. Voltage waveforms in $N$-stage multiplier showing voltage relationship between successive nodes of the diode chain.

The operation of the circuit is illustrated in Fig. 3, in which the typical voltage waveforms in an $N$-stage multiplier are shown. As can be seen, the two clocks $\phi$ and $\bar{\phi}$ are in antiphase with amplitude $V_\phi$, and are capacitively coupled to alternate nodes along the diode chain. The multiplier operates in a manner similar to a bucket-brigade delay line, by pumping packets of charge along the diode chain as the coupling capacitors are successively charged and discharged during each half of the clock cycle. Unlike the bucket-brigade delay line, however, the voltages in the diode chain are not reset after each pumping cycle so that the average node potentials increase progressively from the input to the output of the diode chain. This operation is also similar in principle to the well-known "bootstrap" technique often used in MOS integrated circuits [2] in that a bootstrap circuit incorporates a voltage doubler. Here, however, the coupling capacitor is connected to the input clock, unlike bootstrap circuits in which it is connected to the output. As can be seen in Fig. 3, the difference between the voltages of the $n$th and $(n + 1)$th nodes at the end of each pumping cycle is given by

$$V_{n+1} - V_n = V'_\phi - V_D - V_L \tag{1}$$

where $V'_\phi$ is the voltage swing at each node due to capacitive coupling from the clock, $V_D$ is the forward bias diode voltage, and $V_L$ is the voltage by which the capacitors are charged and discharged when the multiplier is supplying an output current, $I_{OUT}$.

For a clock coupling capacitance, $C$, and stray capacitance $C_S$, at each node, capacitance division gives

$$V'_\phi = \left(\frac{C}{C + C_S}\right) \cdot V_\phi.$$

Also, since the total charge pumped by each diode per clock cycle is $(C + C_S)\, V_L$, the current supplied by the multiplier at a clock frequency, $f$, is given by

$$I_{OUT} = f(C + C_S)\, V_L.$$

Substituting for $V'_\phi$ and $V_L$ in (1) we get

$$V_{n+1} - V_n = \left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D - \frac{I_{OUT}}{(C + C_S) f}$$

so that for $N$ stages,

$$V_N - V_{IN} = N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D - \frac{I_{OUT}}{(C + C_S) f}\right] \tag{2}$$

where $V_{IN}$ is the input voltage. In a practical multiplier, an additional isolating diode is required at the output to prevent clock breakthrough so that the peak output voltage, $V_{OUT}$, is given by

$$V_{OUT} - V_{IN} = N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D - \frac{I_{OUT}}{(C + C_S) f}\right] - V_D.$$

Rearranging, we get

$$V_{OUT} = V_{IN} + N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D\right] - V_D - \frac{N I_{OUT}}{(C + C_S) f}. \tag{3}$$

There is also a ripple voltage, $V_R$, at the multiplier output due to the load resistance, $R_L$, discharging the output capacitance, $C_{OUT}$. Usually, $C_{OUT}$ is sufficiently large for $V_R$ to be small compared to $V_{OUT}$, so that

$$V_R = \frac{I_{OUT}}{f C_{OUT}} = \frac{V_{OUT}}{f R_L C_{OUT}}. \tag{4}$$

In practical multipliers there will also be an additional ripple component due to capacitive coupling from the clocks through the diodes. In the case of nonoverlapping clock phases, there will be significant breakthrough from only one phase through the isolating diode. With overlapping clocks, however, there will also be breakthrough from the other clock phase occurring when the isolating diode is conducting. The magnitude of the breakthrough from either phase is given by

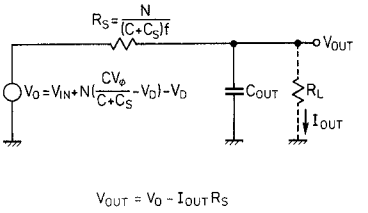


Fig. 4. Equivalent circuit of $N$-stage multiplier.

$$V_{BT} = \left(\frac{C_D}{C_{OUT} + C_D}\right) V'_\phi = \frac{C_D}{C_{OUT}} V'_\phi \quad \text{for} \quad C_{OUT} \gg C_D$$

where $C_D$ is the capacitance across each diode, so that for nonoverlapping clock phases,

$$V_R = \frac{I_{OUT}}{f C_{OUT}} + \frac{C_D V'_\phi}{C_{OUT}} \tag{4a}$$

and for overlapping clock phases,

$$V_R = \frac{I_{OUT}}{f C_{OUT}} + \frac{2 C_D V'_\phi}{C_{OUT}}. \tag{4b}$$

From (3), it can be seen that voltage multiplication occurs, provided that

$$\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D - \frac{I_{OUT}}{(C + C_S) f} > 0. \tag{5}$$

It is important to note that this expression is independent of $N$, so that there is, in principle, no limit to the number of stages in a multiplier of this type. Furthermore, provided that (5) is satisfied, the current drive capability of the multiplier is also independent of the number of multiplier stages.

Also from (3), we can write

$$V_{OUT} = V_O - I_{OUT} R_S \tag{6}$$

where

$$V_O = V_{IN} - V_D + N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_D\right] \tag{7}$$

and

$$R_S = \frac{N}{(C + C_S) f}. \tag{8}$$

$V_O$ and $R_S$ are the open-circuit output voltage and output series resistance of the multiplier, respectively, so that (6) leads to an extremely simple equivalent circuit of the multiplier output, as shown in Fig. 4.

In deriving this model for the voltage multiplier, it has so far been assumed that the capacitors are completely charged and discharged with a diode cutoff voltage, $V_D$. In practice this is not the case due to the nonlinear voltage-current characteristics and internal series resistance, $R_D$, of the diodes. This results in a residual voltage in addition to $V_D$ remaining across

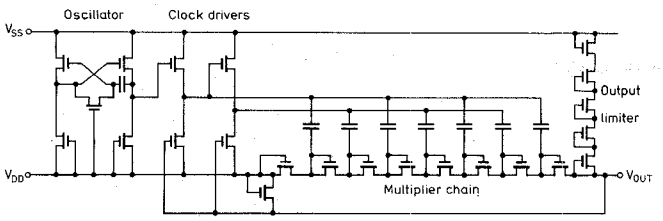


Fig. 5. Practical implementation of multiplier using MOS technology.

the diodes at the end of each cycle, causing the multiplier output series resistance, $R_S$, to increase in a nonlinear manner with load current. However, by making $R_D$ sufficiently small such that

$$R_D(C + C_S) f < 3 \tag{9}$$

the increase of $R_S$ due to this effect is less than 5 percent.

## Practical Implementation

A circuit diagram of the multiplier circuit used in the nonvolatile MNOS quad-latch is shown in Fig. 5. Since this is fabricated using p-channel Al-gate MOS technology in which isolated diodes are not available, the multiplier chain is implemented using diode-connected MOS transistors, as shown. In this case, since MOS transistors are used instead of diodes, the diode forward voltage, $V_D$, is replaced by the MOS threshold voltage, $V_T$, in (3), giving

$$V_{OUT} = V_{IN} - V_T + N\left[\left(\frac{C}{C + C_S}\right) \cdot V_\phi - V_T\right] - \frac{NI_{OUT}}{(C + C_S) f}. \tag{10}$$

Since, in the circuit shown in Fig. 5, $V_{IN} = V_{DD}$ and $V_\phi = (V_{DD} - 1)$, we get

$$V_{OUT} = 1 + \left[1 + \frac{NC}{C + C_S}\right](V_{DD} - 1) - (N + 1) V_T - \frac{NI_{OUT}}{(C + C_S) f}. \tag{11}$$

In the circuit shown in Fig. 5, the clocks are generated by two cascaded MOS inverters driven from an oscillator circuit. In addition, the output is limited by a chain of MOS transistors in series with field-controlled protection diodes. This was found to be necessary to prevent the output voltage exceeding the process limits if the supply voltage, $V_{DD}$, was accidentally increased above the specified range. A microphotograph of the multiplier is shown in Fig. 6, in which it can be seen that it occupies a chip area of approximately 600 $\mu$m X 240 $\mu$m (24 mils X 9.6 mils).

In the multiplier shown in Fig. 6, there are seven stages with $V_{IN}$ equal to the supply voltage, $V_{DD}$. The design values of the coupling capacitors and stray capacitors at each node are 2 and 0.2 pF, respectively. The coupling capacitors are actually implemented using the nitride dielectric available in the MNOS process. The voltage characteristics of the multiplier when

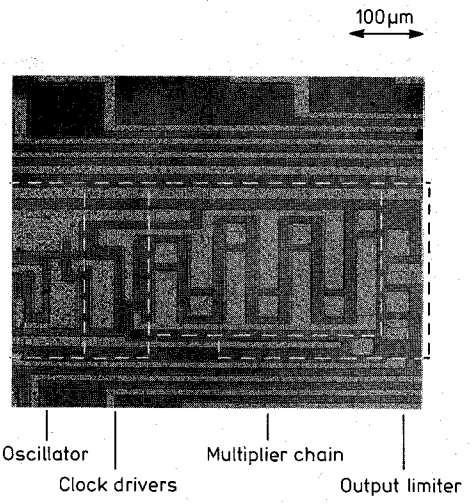


Fig. 6. Photomicrograph of MOS voltage multiplier. Active area approximately 600 $\mu$m X 240 $\mu$m (24 mils X 9.6 mils).

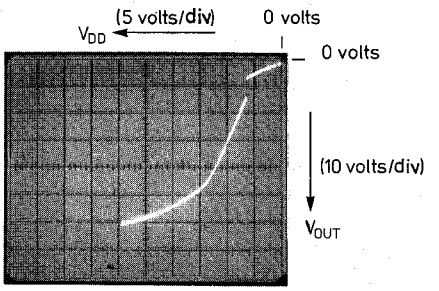


Fig. 7. Voltage characteristics of MOS voltage multiplier driving a 10-M$\Omega$ load.

driving a 10-M$\Omega$ scope probe are shown in Fig. 7. As can be seen, there are three regions in the characteristics:

1) an initial region before the multiplier is operating;
2) a linear multiplication region;
3) a region in which the voltage is limited by the output protection circuit.

The clock frequency, $f$, was about 1 MHz, so that the slope of 5 in the linear multiplication region agrees well with the figure of 5.5 predicted by (11). The multiplier was designed to operate with $V_{DD}$ varying between 15 and 19 V, over which range the multiplier output, $V_{OUT}$, varies between 48 and 54 V, respectively. In Fig. 8, the rise time of the multiplier is shown for $V_{DD}$ = 15 V and an output load capacitance of 1 nF. The time constant over the linear multiplication region of about 3.5 ms agrees well with the 3.2-M$\Omega$ output series resistance predicted by (8).

The multiplier was fabricated with a process which gave MOS transistors with a zero-bias threshold of about 2.0 V and a body constant of 0.4. The MOS transistors in the multiplier chain were designed with a gain factor of 8 $\mu$A/V$^2$ so that the coupling capacitances would be charged to within 1 V of equilibrium in each pumping cycle. Hence in predicting the performance of the multiplier, a good approximation will

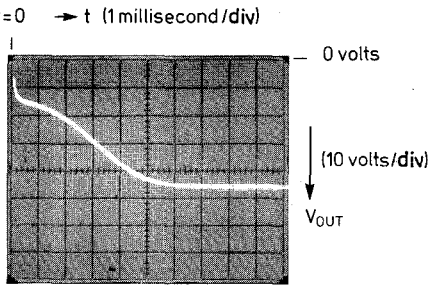


Fig. 8. Rise time of MOS voltage multiplier driving 1 nF output load capacitance. Theoretical value of multiplier output resistance, $R_S$, is typically 3.2 MΩ.

TABLE I
MULTIPLIER OUTPUT AND RIPPLE VOLTAGES AS A FUNCTION OF LOAD CURRENT

| Load Current $I_{OUT}$ (μA) | Output Voltage $V_{OUT}$ (volts) | | P - P Ripple Voltage $V_R$ (volts) | |
|---|---|---|---|---|
| | Predicted | Measured | Predicted | Measured |
| 3.9 | 44.3 | 39.1 | 0.29 | 0.28 |
| 5.4 | 39.5 | 37.5 | 0.31 | 0.30 |
| 6.6 | 35.7 | 33.3 | 0.32 | 0.32 |
| 8.2 | 30.6 | 27.2 | 0.34 | 0.34 |

be achieved by using a value of 5 V for the threshold voltage in (11). This gives

$$V_{OUT} = 7.36\,(V_{DD} - 1\text{ V}) - 39\text{ V} - 3.18 \times 10^{6}\ \text{M}\Omega\, I_{OUT}. \tag{12}$$

Since the clock drivers in Fig. 5 produce overlapping clock phases, the ripple voltage is given by (4b). In this case the calculated value of $C_D$ (the gate-source capacitance of the diode–connected MOS transistors) is 0.1 pF, giving

$$V_R = \frac{1}{C_{OUT}}\left(\frac{I_{OUT}}{10^6\ \text{Hz}} + 2 \times 10^{-13} \times \frac{14}{1.1}\ \text{As}\right)$$

i.e.,

$$V_R = \frac{1}{C_{OUT}}\left(\frac{I_{OUT}}{10^6\ \text{Hz}} + 2.54 \times 10^{-12}\ \text{As}\right). \tag{13}$$

In Table I, below, a comparison is made between the measured values of output and ripple voltage for various load currents, and those predicted by (12) and (13), respectively. The supply voltage, $V_{DD}$, is chosen to be 14 V to ensure that the multiplier is operating in the linear region of its characteristics, and the output capacitance, $C_{OUT}$, is approximately 10 pF. As can be seen, there is a good agreement between the predicted and measured results.

## CONCLUSIONS

The voltage multiplier technique has been demonstrated to be practical, and measured results agree well with the theoretical model. Although developed especially for generating high supply voltages in MNOS integrated circuits, the technique is equally applicable for many other applications. In particular, it may be possible to implement a fully monolithic dc-dc up-converter chip using bipolar technology, utilizing the better frequency performance to operate at much higher current levels.

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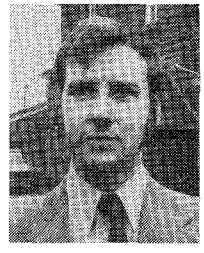

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