A 0.35-μm CMOS Solar Energy Scavenger with Power Storage Management System

M. Ferri, D. Pinna, E. Dallago, P. Malcovati
Department of Electrical Engineering, University of Pavia, Italy
E-Mail: {massimo.ferri, daria.pinna, enrico.dallago, piero.malcovati}@unipv.it

***Abstract*—In this paper we present an integrated solar energy scavenger realized in a 0.35 μm CMOS technology. The proposed system collects solar energy from the environment through integrated diodes, accumulates it and, delivers it to the load when it is enough to allow proper operation of the CMOS circuitry. The proposed system is suitable for discrete-time regime applications, such as sensor network nodes or, generally, systems that require power supply periodically for short time slots. In order to properly design the system, we developed a model of the integrated solar cell on the basis of measurement data extracted from a test chip. The power management circuit, including a charge pump a comparator and a linear voltage regulator, has been extensively simulated.**

I. Introduction

Since a solar energy scavenger is intrinsically a discrete-time power source, which varies with the environmental conditions, photovoltaic systems need an energy storage device and a power management system [1]. Fortunately, many applications, such as sensor network nodes [2]–[5] or, in general wireless embedded systems [6], [7] that operate in descrete-time regime, consume power only during short time-slots [8]. In the system presented in this paper, an integrated miniaturized solar cell is used as energy source and a power management system has been developped [7], to handle the collected energy. The block diagram of the system is shown in Fig. 1, where a generic sensor system has been adopted as load [9]. The circuit elevates with a charge pump the voltage produced by the miniaturized solar cell and charges an external capacitor, in order to supply with 3.3 V through a linear voltage regulator (LDO) the load for a given time-slot, in asynchronous discrete-time regime. The time-slots dedicated to energy accumulation and system operation are established automatically by the system. With this solution it is possible, by choosing the value of the capacitance, to trade the amount of power available for the load with the time required to accumulate it, thus allowing to supply the load for the required time-slot with the required current with a given duty-cycle. The proposed power management circuit consists of an hysteresis comparator and an unbalanced inverter, that controls a switch to connect the load to the storage capacitance. The comparator monitors the charge voltage on the storage capacitor. When the stored charge is sufficient to reach a voltage equal to 4.3 V the comparator provides a signal that, by means of the unbalanced inverter, connects the LDO to the supply voltage (i. e. the storage capacitor), thus supplying the load. When the voltage on the storage capacitor decreases below

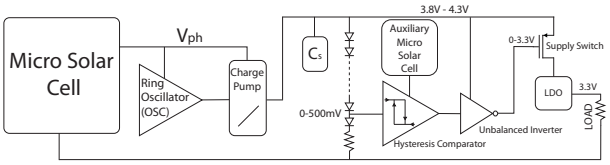

Fig. 1. Block diagram of the proposed system

3.8 V, the LDO is disconnected and the load switched off. In Section II we present the solar source characterization, based on the experimental results obtained from a test chip including several miniaturized solar cells. These results are fundamental for the design of the subsequent power management system. In Section III we describe the charge pump used to elevate the solar cell voltage to a usable value, while Section IV and Section V present the power management system and the LDO, respectively. Finally, in Section VI we derive the criteria for the choice of the value of the storage capacitance.

II. Miniaturized Solar Cell

In order to create a reliable circuit model of the miniaturized solar cell, to be used in the simulation environment for designing the power management system, several cells [10] have been implemented on a test chip in a 0.35 μm CMOS technology. In particular several photodiodes [11], [12], with different dimension of the n-well and different geometry of the p-diffusions, has been realized. Fig. 2 shows the different geometries, while Tab. II summarizes the dimensions and the equivalent active area for each structure. The equivalent circuit model for each solar cell consists of a couple of pn-junctions. As each solar cell must be used as supply harvesting source for an integrated microsystem realized on the same silicon substrate, it is not possible to exploit the photo-generated power of the deeper junction, since this would imply direct biasing of the junction between n-well and substrate, leading to a negative voltage at the n-well terminal with respect to the substrate. Furthermore, the cells cannot be connected in series, because the different cells share the same substrate. Fig. 3 shows the output power of the most efficient structure (structure B), in terms of p-diffusion geometry, obtained with 300 W/mm^2 illumination. The efficiency of the cell is unfortunately reduced by the recombination effect in the base of the parasitic PNP vertical transistor when the junction between n-well and substrate is short-circuited. This curve

978-1-4244-3732-0/09/$25.00 ©2009 IEEE

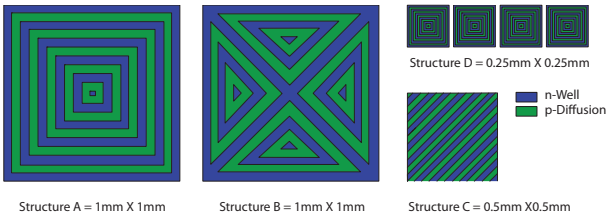

Fig. 2. Geometries of the cells implemented of the test chip

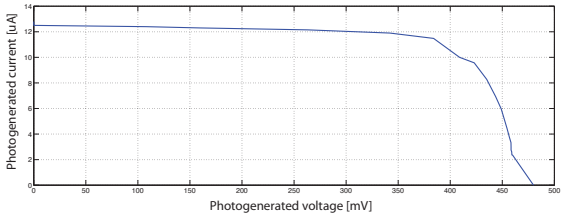

Fig. 3. Measured output power of the most efficient cell, obtained with 300 W/mm^2 illumination

have been used to dimension the solar cell circuit model used for simulation shown in Fig. 4. In particular, we developed a Matlab algorithm wich needs only five measured values of the output power to find the appropriate model parameters. The algorithm provides the following result:

- $I_{ph} = 12.28$ µA;
- $A_D = 100$ µm^2;
- $P_D = 40$ µm;
- $R_{sh} = 40$ kΩ;
- $R_s = 2.27$ kΩ.

III. Ring Oscillator and Charge Pump

The ring oscillator and the charge pump shown in Fig. 5 represent the front-end block of the power management circuit. In order to allow the voltage across the storage capacitor to reach at least 4 V, a Dickson charge pump [13] has been implemented. The circuit requires two non-overlapping

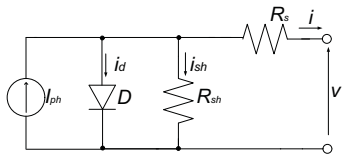

Fig. 4. Solar cell circuit model

TABLE I
Solar Cell Structures

Type	Harvester Area [mm^2]	Harvester Perimeter [mm]	Parasitic Area [mm^2]	Parasitic Perimeter [mm]
A	24.39	642.5	1	4
B	0.29	827.8	2	5.6
C	0.072	207.4	0.5	2.9
D	0.18	47.1	0.06	1

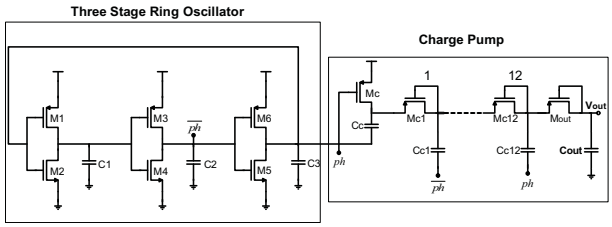

Fig. 5. Schematic of the ring oscillator and of the charge pump

clock phases, ph and $\overline{ph}$, with amplitude equal to the voltage produced by the micro solar cell V_{ph}. The charge pump operates by moving charge along the diode chain, charging the capacitors to increasing voltages. The charge pump has been designed to obtained a voltage of 5 V, starting from $V_{ph} \cong 500$ mV, thus requiring 12 stages. A three stage ring oscillator provides the clock phases for the charge pump with a frequency equal to 29.5 kHz, which correspond to the best trade-off between time required to charge C_c and the charge tranfer rate. The perfomance of the system is limited by the sypply voltage, which is equal to the open-circuit voltage V_{ph} of the integrated micro solar cell, that forces all transistors to work in the sub-threshold region. Such a system provides a very low current flow throught each transistor, introducing an efficiency loss in terms of charge transfer, and hence, in terms of charging time. In order to provide a constant voltage of 3.3 V to the load with a significant current for an estabilished time slot, a storage capacitor is necessary. Therefore, the proposed system is only suitable for loads operated in discrete-time regime, such as sensor network nodes.

IV. Power Management Circuit

In order to control the voltage across the storage capacitor and hence the stored energy, we developed a power management circuit, which consists of an hysteresis comparator and an unbalanced inverter, as shown in Fig. 6. The management circuit provides a control signal to a switch, which connects the load to the storage capacitor when the voltage across the storage capacitor reaches 4.3 V and disconnects the load when it becomes lower than 3.8 V. In order to avoid discharging the storage capacitor, the comparator is supplied directly by an auxiliary solar cell, while the inverter is connected to the storage capacitor voltage. The total power consumtpion of the management block is less than 10 nA when the load is disconnected.

A. Hysteresis Comparator

The hysteresis comparator, whose schematic is shown in Fig. 6, is similar to a mirrored operational amplifier, but we added transistors M_4 and M_5 to obtain a positive feedback loop, which boosts the response time and introduces the hysteresis. This allows to reduce the power consumption during the commutations. Hysteresis in the comparator is needed to avoid continuous commutations of the output when the input voltage is close to the reference voltage. We decided

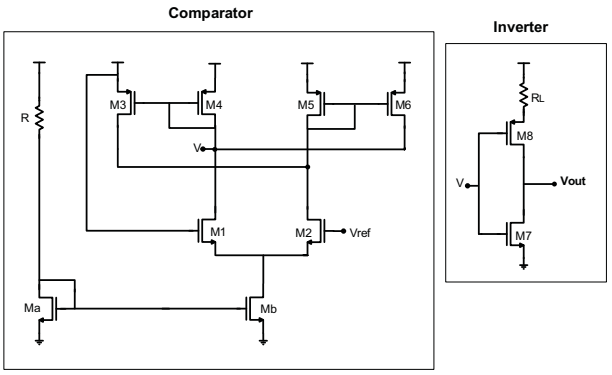

Fig. 6. Schematic of the hysteresis comparator

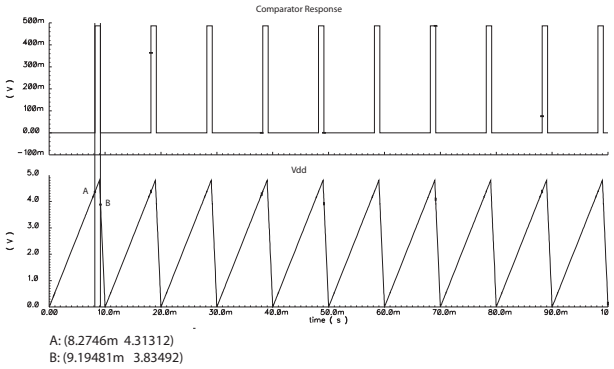

Fig. 7. Simulated comparator response

to use an independent auxiliary solar cell for supplying the comparator, since the main solar cell voltage is affected by the oscillator kick-back. Usually a comparator would need a threshold voltage connected at the gate of M_1, but, in this case, the generation of a threshold voltage from the storage capacitor voltage or from the auxiliary solar cell voltage, would consume too much power. Therefore, we connected directly the photo-generated voltage of the auxiliary solar cell to the gate of M_1 and we unbalanced the comparator input stage, according to

$$\frac{(W_6/L_6)}{(W_5/L_5)} = 10\frac{(W_3/L_3)}{(W_4/L_4)}, \tag{1}$$

thus leading to an equivalent threshold voltage V_{th} lower than the supply voltage.

The response of the comparator is shown in Fig. 7. The total power consumption of the comparator during the charging process is about 5 pW, thus requiring a small area for the auxiliary solar cell.

B. Unbalanced Inverter

The unbalanced inverter, whose schematic is also shown in Fig. 6, features a p-channel transistor M_8 much longer, and hence more resistive, than the n-channel transistor M_7. The degeneration resistor helps to reduce the threshold voltage. In particular the unbalanced inverter has been designed to have a $V_{th} = 390$ mV. This solution reduces the power consumption of the inverter when the input is low (i. e. while charging the storage capacitor). During the charging period, the output voltage of the inverter follows the storage capacitor voltage, turning off the p-channel MOS transistor used as a switch to connect the load to the storage capacitor, thus avoiding any loss of charge. The current consumption of the inverter during the charging process is less than 5 nA.

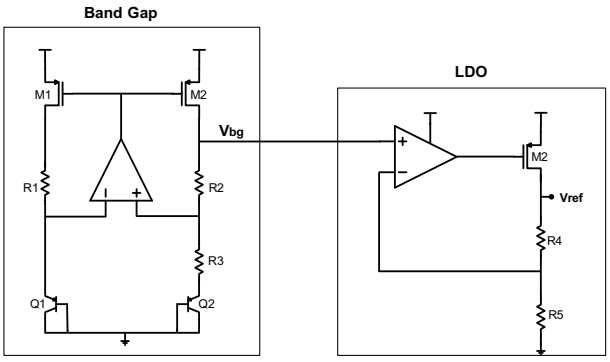

Fig. 8. Schematic of the linear voltage regulator

V. Voltage Regulator

In order to provide a fixed 3.3 V supply to the actual load, a linear voltage regulator (LDO) has been implemented. It consists of a a bangap circuit and a regulator circuit. This block is supplied when the storage capacitor has reached the proper voltage. Fig. 8 shows the schematic of the voltage regulator. The total current consumption of the circuit is less than 2 μA.

A. Bandgap Circuit

The band-gap circuit provides a stable voltage reference (V_{bg}) as reference input of the LDO. It operates compensating the negative temperature coifficient of a pn-junction voltage V_{be}, with the positive temperature coefficient of the thermal voltage V_T. The output voltage of the circuit is

$$V_{bg} = V_{be} + mV_T, \tag{2}$$

where m depends on the bandgap circuit topology. With the topology used, m coefficient is given by

$$m = \frac{R_2}{R_1}\ln\left[\frac{(W_1/L_1)}{(W_2/L_2)}\frac{A_2}{A_1}\right]. \tag{3}$$

Even if the supply voltage follows the discharge curve of the storage capacitor, the V_{bg} remains constant.

B. LDO

The LDO provides a stable 3.3 V supply voltage with an input voltage ranging from 3.3 V to 4.8 V, allowing the actual load to operate properly. In particular, the output voltage is given by

$$V_{ref} = V_{bg}\frac{R_4 + R_5}{R_4}. \tag{4}$$

Simulation results demostrate that the output voltage has a maximum error of 0.3% over the whole input voltage range,

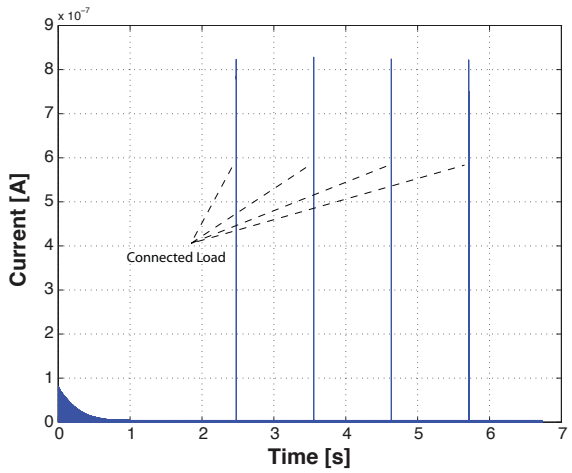

Fig. 9. Simulation of the current flowing through the storage capacitor

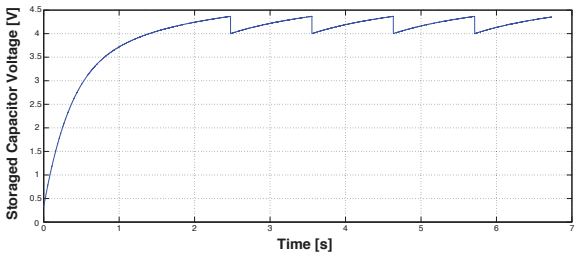

Fig. 10. Simulation of the voltage across the storage capacitor

although, in order to reduce the power dissipation, R_4 and R_5 are in the MΩ range. The total current consumption is about 1 μA.

VI. Storage Capacitor Sizing

The storage capacitor is an external component, and, hence, its value can be chosen on the basis of the actual load power consumption. In particular, the charge trasfer rate of the charge pump in the range from 3.8 V to 4.3 V is less than 10 nA. Most of efficiency is lost in the charge pump, but this is not particulary important, because the system is able to store energy and provide it to the actual load only when it is enough allow proper operation in an estabilished time-slot. Fig. 9 shows the current in a 10 nF storage capacitor during the charge process and when the load is connected. The storage capacitor voltage working cycle is shown in Fig. 10. If the load would require longer working time it is enought to use a larger storage capacitor, leading to a lower duty cycle. In particular the charging time is proportional to the current I_{load} that the load needs for a time-slot t_w.

VII. Conclusions

In this paper a 0.35 μm CMOS solar energy scavenging system has been presented. The entire system is suitable for discrete-time regime applications, such as sensor network nodes or, generally, systems that require power supply periodically for short time slots. A power management circuit has been implemented, to monitor the charging process of an energy storage device and connect the actual load only when the stored energy is sufficient to supply the load for a given time. The system has been extensively simulated to validate the proposed approach.

Acknowledgment

The Matlab algorithm to obtain the solar cell parameters have been developped for other purposes by Patrick Merhej, of the Department of Electrical Engineering of the University of Pavia.

References

[1] N. Guilar, A. Chen, T. Kleeburg, and R. Amirtharajah, "Integrated solar energy harvesting and storage," in *ACM/IEEE ISLPED*, 2006, pp. 20–24.

[2] A. Kansal and M. Srivastava, "An environmental energy harvesting framework for sensor networks," in *Intl. Symp. Low Power Elec. and Design (ISLPED) '03*, 2003, pp. 481–486.

[3] A. Arms, C. Townsed, D. Churchill, J. Galbreath, and S. Mundell, "Power management for energy harvesting wireless sensor," in *SPIE International Symposium on Smart Structures and Smart Materials*, 2005.

[4] B. Otis, Y. Chee, and J. Rabey, "A 400 μW-Rx, 1.6 mW-Tx super-regenerative transceiver for wireless sensor networks," in *IEEE International Solid-State Circuits Conference (ISSCC 2005)*, 2005, pp. 396–397.

[5] M. Rahimi, H. Shah, G. Sukhatme, J. Heideman, and D. Estrin, "Studying the feasibility of energy scavenging in mobile sensor network," in *IEEE International Conference on Robotics and Automation Proceedings*, 2003, pp. 19–24.

[6] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *International Symposium on Informatic Processing in Sensor Networks*, 2005, pp. 457–462.

[7] A. Kansal, J. Hsu, M. Srivastava, and V. Raqhunathan, "Harvesting aware power management for sensor networks," in *ACM/IEEE Design Automation Conference*, 2006, pp. 651–656.

[8] W. Walker, T. Polk, A. Hande, and D. Bhatia, "Remote blood pressure monitoring using a wireless sensor network," in *Sixth IEEE Annual Emerging Information Technology Conference Proceedings*, Dallas, Texas, 2006.

[9] P. Woias, Y. Manoli, T. Nann, and V. Stetten, "Energy harvesting for autonomous microsystems," in *MST News*, vol. 4, no. 05, 2005, pp. 42–45.

[10] D. A. Neamen, *Semiconductor Physics and Devices*, 1st ed., McGraw-Hill, Ed. McGraw-Hill Science/Engineering/Math, 1992.

[11] J. S. Lee, R. I. Hornsey, and D. Renshaw, "Analysis of CMOS photodiodes - part I: Quantum efficiency," in *IEEE Trans. on Electron Devices*, vol. 50, no. 5, 2003.

[12] ——, "Analysis of CMOS photodiodes - part II: Lateral photoresponse," in *IEEE Trans. on Electron Devices*, vol. 50, no. 5, 2003.

[13] J. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," in *IEEE J. Solid-State Circuits*, vol. 11, no. 6, 1976, pp. 347–348.