A sub-1 V high-precision CMOS bandgap voltage reference

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Abstract: A third-order, sub-1 V bandgap voltage reference design for low-power supply, high-precision applications is presented. This design uses a current-mode compensation technique and temperature-dependent resistor ratio to obtain high-order curvature compensation. The circuit was designed and fabricated by SMIC 0.18 μm CMOS technology. It produces an output reference of 713.6 mV. The temperature coefficient is 3.235 ppm/℃ in the temperature range of –40 to 120 ℃, with a line regulation of 0.199 mV/V when the supply voltage varies from 0.95 to 3 V. The average current consumption of the whole circuit is 49 μA at the supply voltage of 1 V.

Key words: bandgap reference; curvature compensation; low power supply; low temperature coefficient

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1. Introduction

Bandgap voltage references (BGRs) are key parts of many analog circuits and mixed signal circuits. The performance of these circuits directly depends on BGR characteristics such as nominal voltage reference value ($V_{\rm ref}$), temperature coefficient ($T_{\rm c}$), temperature range ($T_{\rm r}$), accuracy, consumption, etc. A traditional bandgap reference has a minimum $T_{\rm c}$ around 20 ppm when temperature ranges from –20 to 80 ℃[1], which means that the reference voltage would change almost 2 mV in the whole temperature-range, which is far from the requirements of most high accuracy applications. Many high-order temperature compensation techniques have been proposed to gain lower $T_{\rm c}$ in the last decade, including piecewise-linear compensation[2], exponential temperature compensation[3] and compensation by utilizing a temperature-dependent resistor ratio with a highly resistive poly resistor and a diffusion resistor[4].

Along with the shrinking device dimensions in CMOS technologies, a lower supply voltage is required to ensure device reliability. As a result, low-supply-voltage BGRs are confronted with several challenges: first, the bandgap voltage of silicon, which is around 1.2 V, is higher than supply voltage; second, the base–emitter voltage ($V_{\rm be}$) of forward biased BJT (around 0.7 V) also makes it hard to decrease the supply voltage to sub-1 V; third, the design of operational amplifiers with a low supply voltage is also not an easy task[5, 6].

In this paper, a novel high precision sub-1 V curvature compensated BGR with a compensation approach and high accuracy is presented. A $T_{\rm c}$ of 3.235 ppm/℃ in the range of −40 to 120 ℃ is obtained.

2. Traditional BGR design

Two parts build up the output voltage of a BGR. One is the voltage of base–emitter voltage of a forward biased BJT and the other is a voltage that is proportional to the absolute temperature (PTAT). The positive temperature coefficient of the latter compensates for the negative temperature coefficient of the former. The reference voltage can be expressed as

$$V_{\rm ref} = V_{\rm be}(T) + \Delta V_{\rm be}(T), \tag{1}$$

where $V_{\rm be}$ has a negative temperature coefficient, while $\Delta V_{\rm be}$ is the voltage difference between two BJTs with different current densities, this provides a positive temperature coefficient to cancel the negative temperature coefficient of $V_{\rm be}$.

According to Ref. [7], $V_{\rm be}$ can be expressed as

$$V_{\rm be}(T) = V_{\rm g}(T_0) + \frac{T}{T_0}\left[V_{\rm be}(T_0) - V_{\rm g}(T_0)\right] - (\eta - m)\frac{kT}{q}\ln\frac{T_0}{T}, \tag{2}$$

where $V_{\rm g}$ represents the bandgap voltage at 0 K, η is a constant related with process, k is the Boltzmann's constant, q is the charge of an electron, T_0 is the reference temperature and m is the order of the temperature dependence of the collector current ($m = 0$ when collector current is independent of temperature, $m = 1$ when collector current is PTAT). Obviously, $V_{\rm be}$ contains the first order and higher order terms of T, and it has a negative temperature coefficient ranging from –1.5 to –2 mV.

For BJTs, the base–emitter junction has an $I_{\rm c}$–$V_{\rm be}$ relationship as below:

$$I_{\rm c} = I_{\rm s}{\rm e}^{qV_{\rm be}/kT}. \tag{3}$$

For two diode-connected BJTs with an emitter area ratio of N, when they have the same collector current, it leads to a difference of $V_{\rm be}$ between them:

$$\Delta V_{\rm be} = \frac{kT}{q}\ln N = V_{\rm t}\ln N. \tag{4}$$

Thus $\Delta V_{\rm be}$ exhibits a positive temperature coefficient:

$$\frac{\partial \Delta V_{\rm be}}{\partial T} = \frac{k}{q}\ln N, \tag{5}$$

since $k/q \approx 0.087$ mV/K, a positive temperature coefficient is gained. Thus the reference voltage $V_{\rm ref}$ is:

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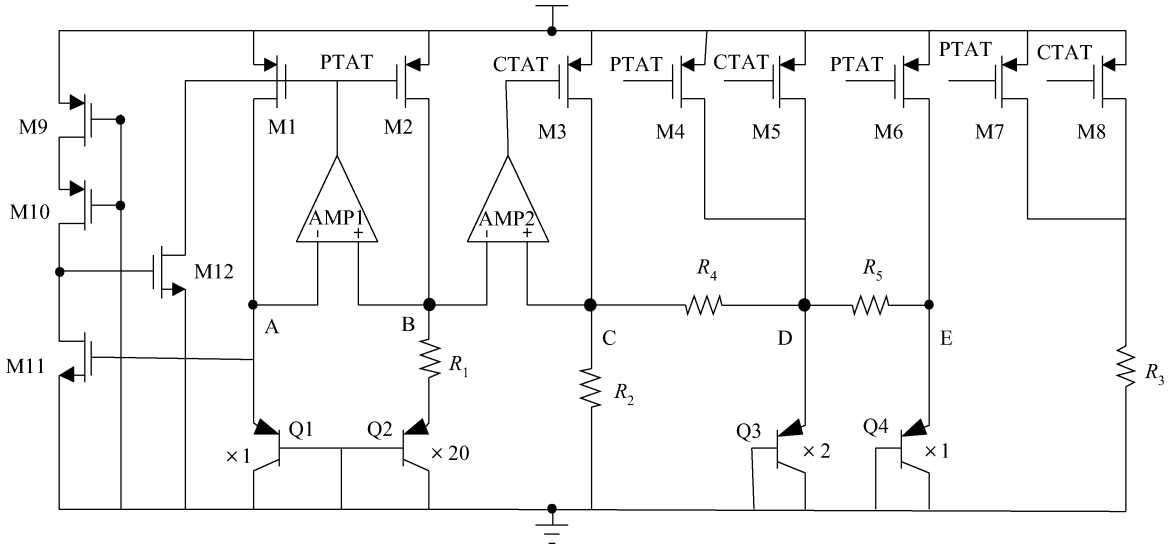

Fig. 1. Proposed compensated bandgap circuit with start-up circuit.

$$V_{\rm ref} = V_{\rm g}(T_0) + \frac{T}{T_0}\left[V_{\rm be}(T_0) - V_{\rm g}(T_0)\right] + \frac{KT}{q}\ln N - (\eta - m)\frac{kT}{q}\ln\frac{T}{T_0}. \quad (6)$$

For traditional BGRs, $V_{\rm ref}$ obtained in Eq. (6) is the silicon bandgap voltage, which is about 1.2 V, with a $T_{\rm c}$ of several tens of ppm/℃. So proper designs must be applied to reduce the supply voltage and the $T_{\rm c}$ of the reference.

3. Proposed curvature compensation with low supply voltage

Traditional BGRs have provided a basic principle of bandgap reference, but as discussed in the last section, they are not suitable for low-supply-voltage, high-precision applications. There are two basic approaches to obtain curvature compensation in low-power-supply BGR designs. One is the voltage-mode reference design, but it suffers from problems such as a low output voltage and a high dependence on process[8]. The other is the current-mode reference design. In this technique, a temperature-independent current is obtained by adding PTAT currents to currents that are complementary to absolute temperature (CTAT). This temperature-compensated current is then mirrored to a resistor to yield a temperature-compensated reference voltage. Because the current-mode technique is easier to be realized in the CMOS technology, it is being increasingly applied in BGR designs. Existing current-mode curvature-compensated BGRs are able to cancel up to 2nd order non-linearity of $V_{\rm be}$, by subtracting a voltage which is proportional to the nonlinearities of $V_{\rm be}$. This basic idea is adopted in the design proposed in this paper.

Various approaches to compensate for the nonlinearities of $V_{\rm be}$ have been proposed. The solution proposed in this paper is similar to the technique proposed in Ref. [5]. The fundamental idea to correct the nonlinearities is to use the differential voltage ($V_{\rm nl}$) between the $V_{\rm be}$ of a BJT that has a temperature-independent current ($m = 0$) and the $V_{\rm be}$ of a BJT that has a PTAT current ($m = 1$). Since the last term of $V_{\rm be}$ is directly proportional to $V_{\rm nl}$, this independent $V_{\rm nl}$ can be used to compensate $V_{\rm be}$.

The core compensated bandgap circuit with startup circuit proposed in this paper is shown in Fig. 1. The emitter area ratio of Q2 and Q1 is 20, thus a voltage of $\Delta V_{\rm eb}$ is generated. The voltage of node B equals the voltage of node A by the function of amplifier AMP1, so the voltage over R_1 is $\Delta V_{\rm eb}$, thus a PTAT current is yielded through R_1. The voltage of node C equals the voltage of point A, which is $V_{\rm eb}$ of Q1, so a CTAT current is yielded through resistor R_2. By adding these two currents together, a current that is comparatively independent of temperature can be gained at node D.

From Eq. (1), $V_{\rm eb1}$ and $V_{\rm eb3}$ can be determined. For Q1, the current across its junction is PTAT, so $m = 1$, thus:

$$V_{\rm eb1} = V_{\rm g}(T_0) + \frac{T}{T_0}\left[V_{\rm eb}(T_0) - V_{\rm g}(T_0)\right] - (\eta - 1)\frac{kT}{q}\ln\frac{T}{T_0}. \quad (7)$$

For Q3, the current across its junction is the combination of a PTAT current and a CTAT current, it is independent of temperature, $m = 0$ in this case, so:

$$V_{\rm eb3}(T) = V_{\rm g}(T_0) + \frac{T}{T_0}\left[V_{\rm eb}(T_0) - V_{\rm g}(T_0)\right] - \eta\frac{kT}{q}\ln\frac{T}{T_0}. \quad (8)$$

Subtracting $V_{\rm eb1}$ from $V_{\rm eb3}$:

$$V_{\rm eb3}(T) - V_{\rm eb1}(T) = V_{\rm t}\ln\frac{T}{T_0} = V_{\rm nl}. \quad (9)$$

With the same idea, the differential voltage between node D and node E is also $V_{\rm nl}$ because the current through the junction of Q4 is a PTAT current. As a result, the current through the output resistor R_3 can be expressed as:

$$I_{\rm ref} = \frac{\Delta V_{\rm eb1.2}}{R_1} + \frac{V_{\rm eb1}}{R_2} - \frac{V_{\rm nl}}{R_4} + \frac{V_{\rm nl}}{R_5}. \quad (10)$$

The implementation of R_4, R_5 brings two advantages. First, because the current created by R_4, R_5 is proportional

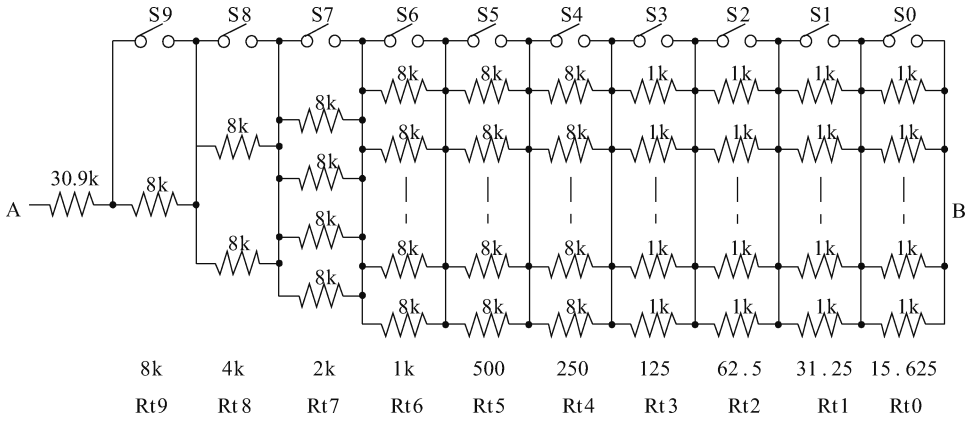

Fig. 2. Trimming resistors.

to $V_{\rm nl}$, it can be used to compensate the last term of $V_{\rm eb1}$. Second, besides compensating the 2nd term of Eq. (10), both R_4 and R_5 use poly-silicon resistors with negative second order temperature coefficient to fine tune the curvature. In fact, after the compensation of $V_{\rm eb1}$ by the implementation of the resistor R_4, the second differential coefficient of output voltage is still negative, so R_4 uses resistors with negative second order temperature coefficient to compensate this negative coefficient. R_5 uses the same type of resistor to fine tune the curvature after the compensation of R_4. So the reference voltage can be expressed as:

$$V_{\rm ref} = R_3\left(\frac{\Delta V_{\rm eb1.2}}{R_1} + \frac{V_{\rm eb1}}{R_2} - V_{\rm nl}\frac{R_5 - R_4}{R_4 R_5}\right). \qquad (11)$$

Two kinds of resistors have been used in the proposed circuit. Resistors R_1, R_2, R_3 use the same type of resistor that contains positive 2nd order temperature coefficient, so the resistor ratio of R_3/R_1 and R_3/R_2 are constant. As a result, the first term of $V_{\rm ref}$ does not contain any nonlinear temperature dependency, but the second term contains high-order temperature coefficient because of $V_{\rm eb1}$. Resistors R_4, R_5 are introduced in the 3rd term to compensate the high order in the second term, negative 2nd order temperature coefficient of resistors R_4 and R_5 can assure a better precision of the output voltage. A precise, 3rd order compensated curvature is achieved by this design in simulation.

4. Trimming resistors

It is expected that the mismatch of resistors will seriously jeopardize the performance of the BGR. Trimming resistors are introduced to solve this problem in this design. R_1, R_2, Q1 and Q2 decide the first order compensation. However, it is difficult to reach a perfect match of the emitter area between Q2 and Q1 in the layout, the mismatch could be even more serious because of the process variations. So, trimming resistors are applied to R_2 to solve this problem. R_4 mainly decides the higher order compensation, so trimming resistors are introduced to R_4 too.

The trimming circuit of R_4 is shown in Fig. 2, where the resistors are connected in series into the circuit. The trimming resistors are connected to a resistor of 30.9 kΩ in series, the resistance of the trimming resistors can change from 0 Ω to (16k−15.625) Ω, so the whole resistance range of R_4 is about 38.9 kΩ ± 8 kΩ. Because the required resistance of R_4 is 38.9 kΩ in the design, the trimming resistors are designed to correct up to ± 20% variations of R_4. The minimum step of the trimming resistors is set to as small as 15.625 Ω to gain high accuracy. The same trimming approach is also applied to R_2 in this design.

In order to reduce the mismatch of the trimming resistors, 8 kΩ resistors are connected in parallel to form the resistors of 8 kΩ, 4 kΩ, 2 kΩ, 1 kΩ, 500 Ω, 250 Ω. But to form lower resistance resistors by connecting 8 kΩ resistors in parallel, a huge number of resistors would be needed and it would dramatically increase the area occupied by the circuit. So 1 kΩ resistors are introduced to form low resistance resistors in this trimming circuit.

A 10-bit digital signal is used to control the state of the switches and the resistance of the trimming resistors can be decided. For example, when the 10-bit control signal is 11 1011 0010, then switches S6, S3, S2, S0 are off, all the other switches are on, so the trimming resistance is $R_{\rm t6} + R_{\rm t3} + R_{\rm t2} + R_{\rm t0} =$ 1 kΩ + 125 Ω + 62.5 Ω + 15.625 Ω = 1203.125 Ω. The trimming resistance can also be calculated as $(2^6 + 2^3 + 2^2 + 2^0) \times 15.625\ \Omega = 1203.125\ \Omega$. As the 10-bit signal changes from 11 1111 1111 to 00 0000 0000, the trimming resistance can change from 0 Ω to $(2^{10} - 1) \times 15.625\ \Omega$.

5. Lower power supply amplifier

$V_{\rm eb1}$ would change from 800 to 550 mV when temperature changes from –40 to 120 ℃, which means the common-mode voltage of the operational amplifier in Fig. 1 would change more than 200 mV in the whole temperature range, so wide common-mode voltage range is another important characteristic of the amplifier besides low supply voltage.

In the 0.18 μm technology, the threshold voltage has been reduced to around 400 mV compared to 700 mV in the 0.35 μm technology, making it more convenient to design the amplifiers in bandgap references with usual structures. In order to keep all of the MOS transistors working in saturation at low supply voltage, cascade configurations are not adopted.

A two stage amplifier was designed in this circuit, as shown in Fig. 3. In order to keep it work over the whole temperature range, self-bias circuit is also implemented in the design. To keep M3 operate in saturation, the common-mode in-

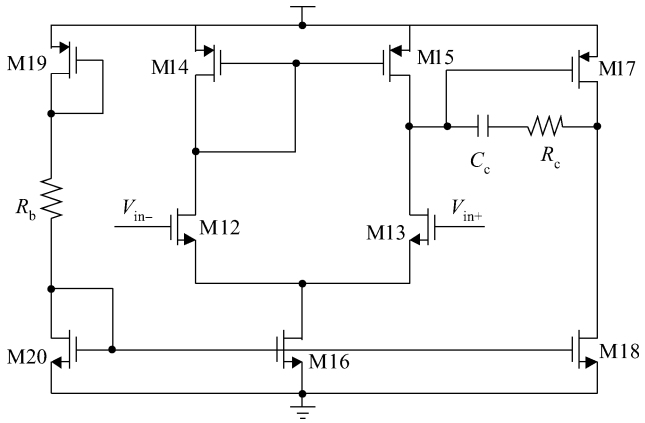

Fig. 3. Two-stage amplifier used in proposed BGR.

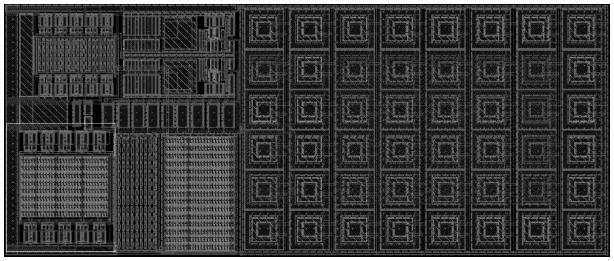

Fig. 4. Layout of the proposed BGR.

put voltage is constrained as below:

$$V_{ic} = \frac{V_{in+} + V_{in-}}{2} \geqslant V_{gs12} + V_{dsat16}, \quad (12)$$

where V_{gs12} represents the gate–source voltage of M12, V_{dsat16} represents the over-drive voltage of M16. To keep all the transistors operating in saturation,

$$V_{DD} \geqslant V_{dsat16} + V_{dsat12} + |V_{th14}| + |V_{dsat14}|, \quad (13)$$

where V_{th3} represents the threshold voltage of M3. Another constraint on V_{DD} comes from Fig. 1:

$$V_{DD} \geqslant V_{ic} + V_{dsat1} \geqslant V_{th12} + V_{dsat12} + V_{dsat16} + V_{dsat1}. \quad (14)$$

The minimum required power supply voltage of the reference is the maximum of these two constraints. Since V_{dsat12}, V_{dsat16} appear in both constraints, the minimum VDD is set by the larger of $|V_{th14}| + |V_{dsat14}|$, $|V_{th12}| + V_{dsat1}$. However, in the 0.18 μm technology, the threshold voltage of PMOS and NMOS are almost the same, so both $|V_{th14}| + |V_{dsat14}|$ and $|V_{th12}| + V_{dsat1}$ have the chance to decide the minimum supply voltage.

6. Simulation and test results

The proposed BGR in this paper was designed and fabricated in an SMIC 0.18 μm process. The layout of the whole circuit is shown in Fig. 4, the whole circuit occupies 268 × 110 μm^2 of area.

The results were measured by using an Agilent 34401A digital multimeter under the environment provided by a high and low temperature test chamber. The measured output reference voltage over temperature after trimming is shown in Fig. 5. A precise, high-order compensated curvature has been obtained through this design, the maximum voltage difference of the reference is 0.369 mV after compensation over the temperature range of –40 to 120 ℃ when the supply voltage is 1 V, thus a T_c of 3.235 ppm/℃ is gained, which is lower than most reported low power BGRs.

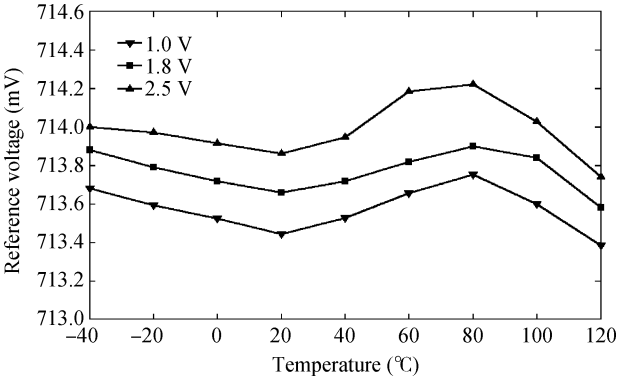

Fig. 5. Measured temperature coefficient of the proposed BGR.

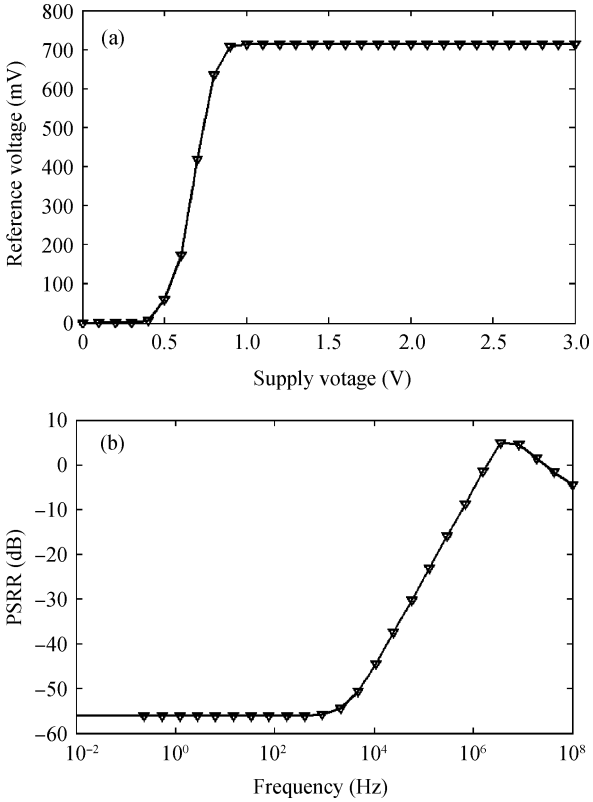

Fig. 6. Measured supply characteristics of proposed BGR. (a) Reference versus supply voltage. (b) PSRR of proposed BGR.

Figure 6(a) shows the dependence of output reference voltage on the supply voltage increases at room temperature of 27 ℃. Measured results show that as the supply voltage increases from 0.95 to 3 V, the reference voltage increases from 713. 523 to 713.931 mV, the voltage difference is 0.408 mV, so this BGR shows a low line regulation of 0.199 mV/V.

In order to keep the circuit working when supply voltage

Table 1. Comparison with other BGRs.

Parameter	This paper	Ref. [12]	Ref. [13]	Ref. [14]	Ref. [15]	Ref. [16]	Ref. [17]
Technology	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	90 nm CMOS
V_{ref} (V)	0.7136	1.012	0.823	0.657	0.487	0.602	0.5847
VDD	1	1.4	1.2	1.1	1.2	1.2	1.2
Power dissipation (mW)	0.05	0.021	0.04	0.047	0.01	0.072	0.16
T_r (℃)	–40 to 120	–30 to 120	–40 to 125	0–150	–70 to 130	0–100	0–125
T_c (ppm/℃)	3.235	4	12.5	10	4.1	2.2	3.343
Line regulation (mV/V)	0.199	0.3	—	5.2	–	—	4.58
PSRR (dB) @ 1 kHz	–57	–66	–60	–55	—	–67	–20.685
Area (mm^2)	0.03	—	—	0.186	0.04	—	0.0085

is lower than 1 V, techniques such as cascade structures are not adopted in this design, so the PSRR of this BGR can only reach a moderate level. The measured PSRR of this BGR is –56 dB at 1 kHz, –25 dB at 100 kHz. The whole current consumed by the BGR is 49.43 μA under the power supply of 1 V.

A comparison between the proposed BGR and other recently reported low-power supply BGRs are presented in Table 1. Reference [12] provides a higher reference voltage with less power consumption, but it needs a higher supply voltage to ensure a low temperature coefficient. The temperature coefficient and line regulation in the designs of Refs. [13, 14] are too high for high-precision applications. Reference [15] shows satisfactory performances on power consumption, temperature range and temperature coefficient, but a low reference voltage would limit its range of application. The design of Refs. [16, 17] is fabricated by advanced CMOS technology. It occupies less area and reaches a lower temperature coefficient. But on the other aspects, the proposed design is superior to them. In summary, the design proposed in this paper has achieved good performances for supply voltage, temperature coefficient and line regulation with a moderate reference voltage and temperature range.

7. Conclusion

A low-voltage high-order curvature-compensated bandgap reference circuit is proposed. Both current-mode compensation technique and the temperature coefficient of resistors are used to achieve high-order compensation. Precise trimming resistors are introduced to overcome the mismatches to ensure high accuracy of the reference. The whole design is verified in a standard 0.18 μm CMOS technology. A reference voltage of 713.6 mV with T_c of 3.235 ppm/℃ is obtained in the temperature range of –40 to 120 ℃. The power dissipation and die area are comparatively small. This BGR has been implemented in a high-precision application, and shows good performance through the measurements.

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