CHAPTER 5 –
MOS FIELD-EFFECT TRANSISTORS

5.1 The MOS capacitor

5.2 The enhancement-type N-MOS transistor

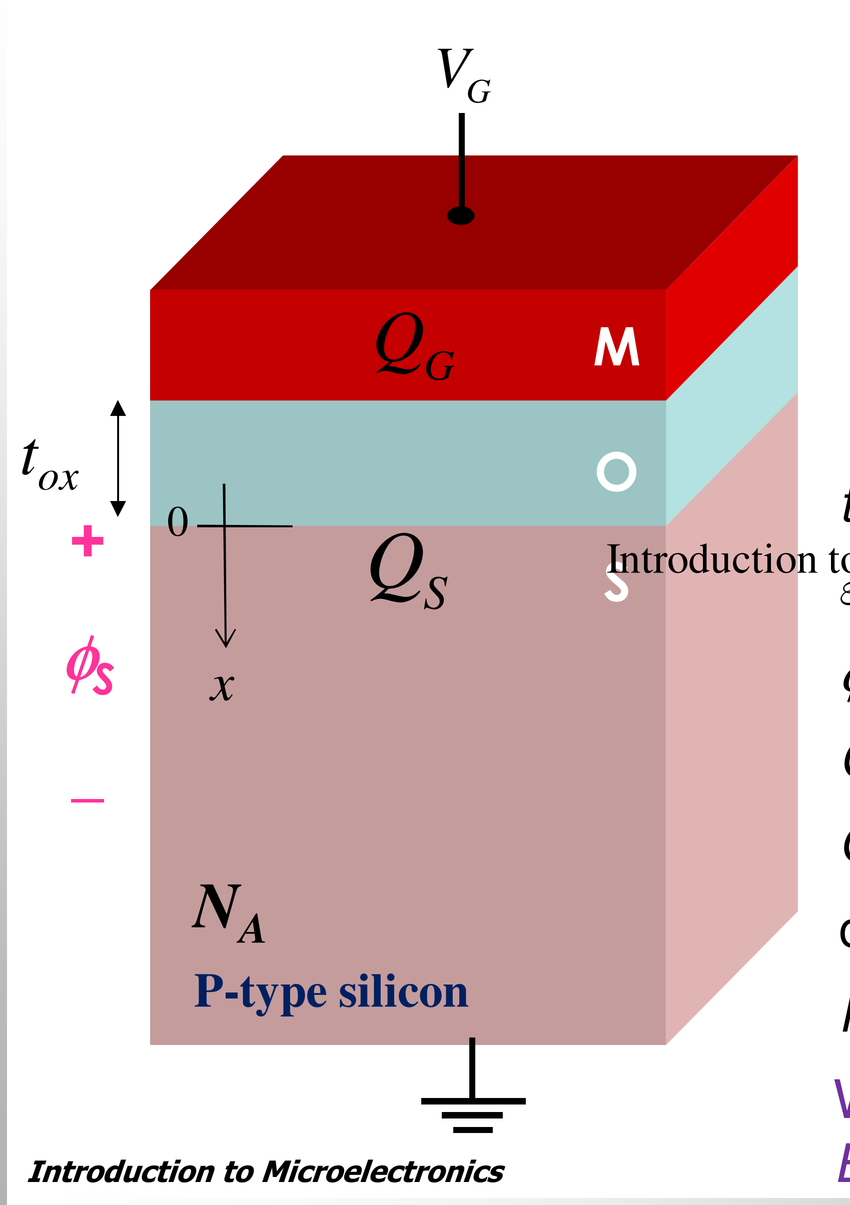
5.3 I-V characteristics of enhancement mode MOSFETS

5.4 The PMOS transistor and CMOS technology

5.5 MOS logic circuits

5.6 Some other considerations on MOSFETs

The "ideal" two-terminal MOS structure



$$V_G - \phi_s = \frac{Q_G}{C_{ox}}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Charge conservation

$$Q_G + Q_S = 0$$

$$V_G = \phi_s - \frac{Q_S}{C_{ox}}$$

Potential balance equation

Introduction to Microelectronics

t_{ox} - oxide thickness

ε_{ox} - permittivity of oxide

ϕ_S - surface potential

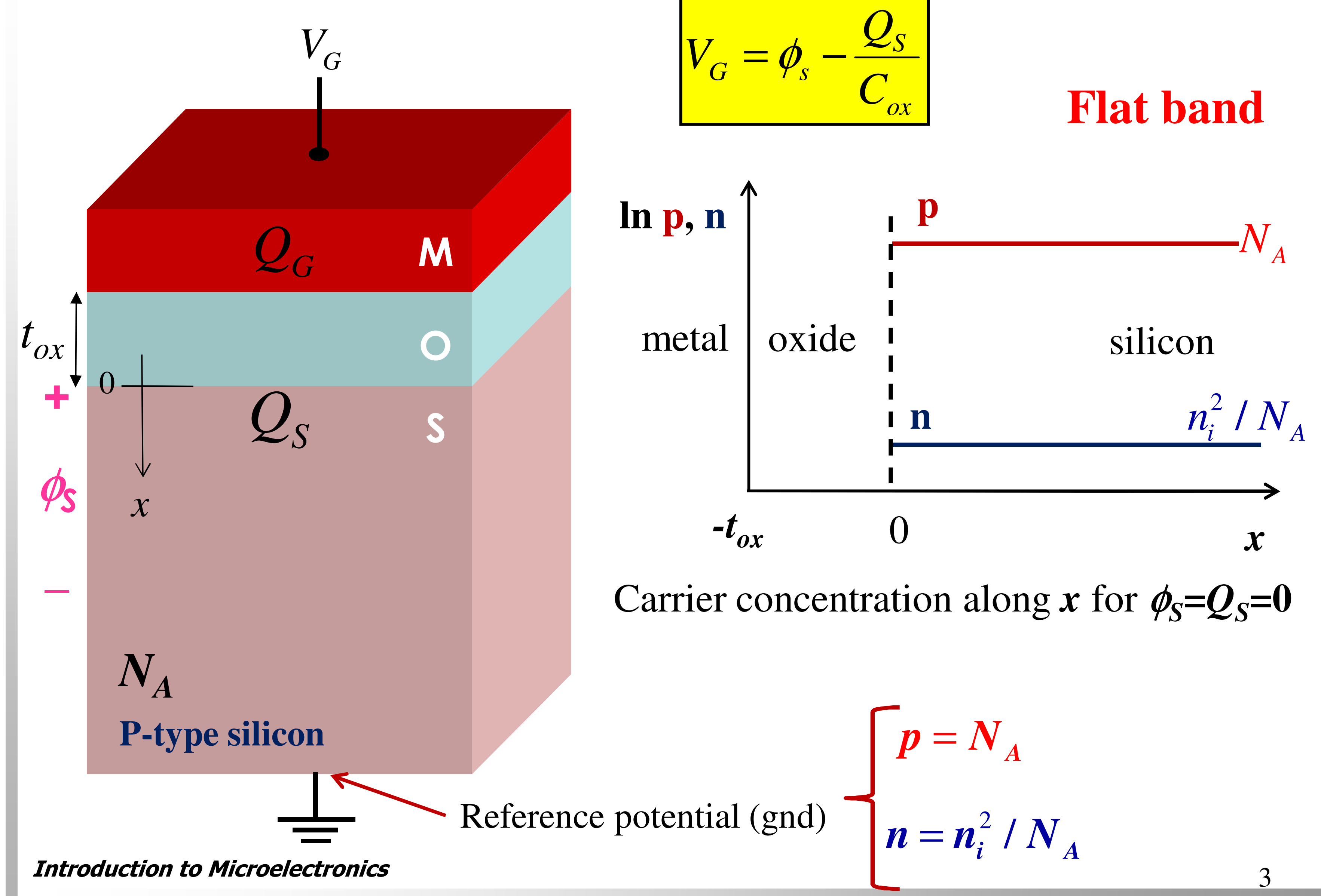
C_{ox} - oxide capacitance/unit area

Q_G (Q_S) - gate (semiconductor) charge/ unit area

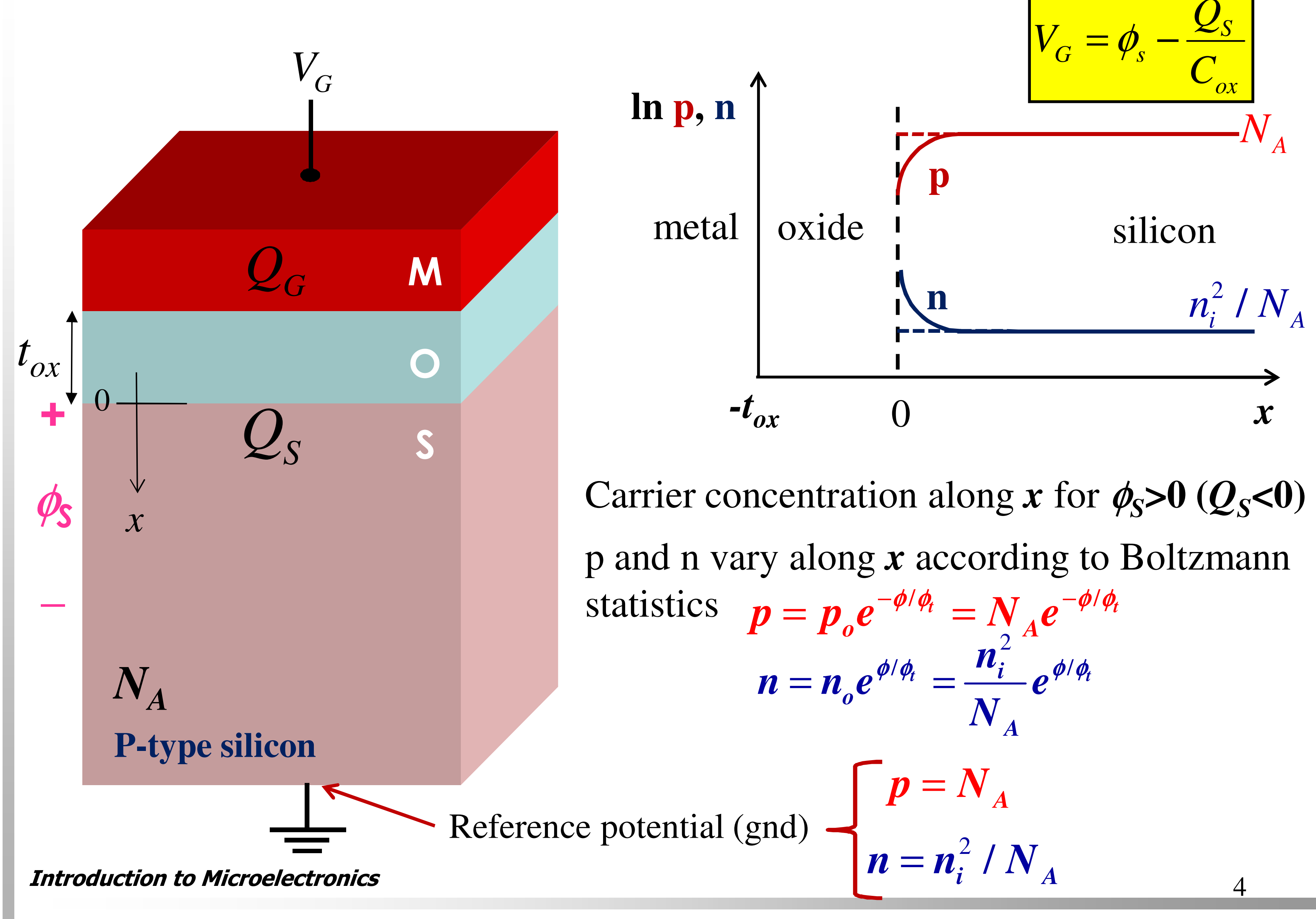
N_A – acceptor concentration

What´s the electric field E_{ox} inside the oxide?

The "ideal" two-terminal MOS structure



The "ideal" two-terminal MOS structure

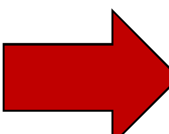


The flat-band voltage (V_{FB})

The flat-band voltage is the gate-to-bulk voltage required to impose $\phi_S = 0$ (and $Q_S = 0$). When $V_{GB} = V_{FB}$ silicon is neutral everywhere.

$$V_{FB} = V_{GB}\Big|_{\phi_s = Q_S = 0}$$

Why is the flat-band voltage not equal to zero?

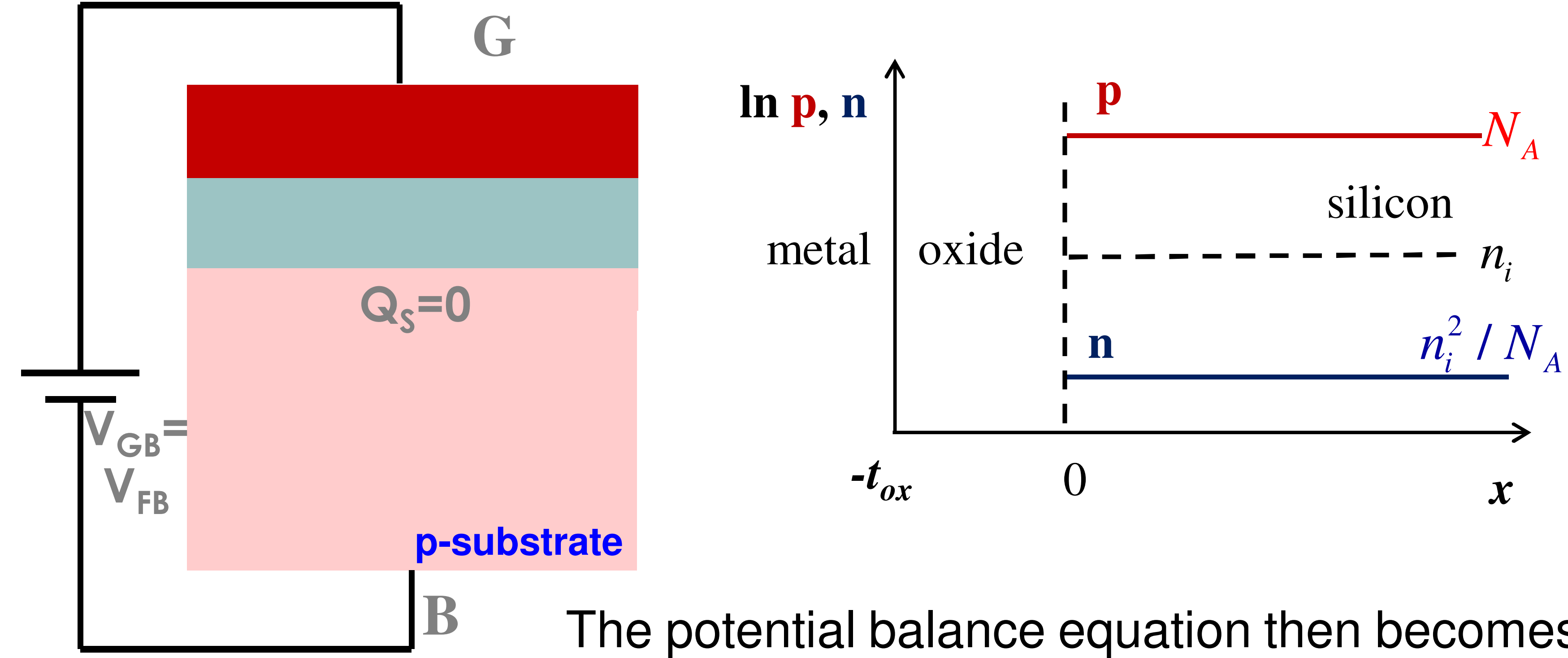


1. Charges inside the insulator and at the semiconductor-insulator interface

2. Contact potential between the gate and the semiconductor substrate

The flat-band voltage (V_{FB})

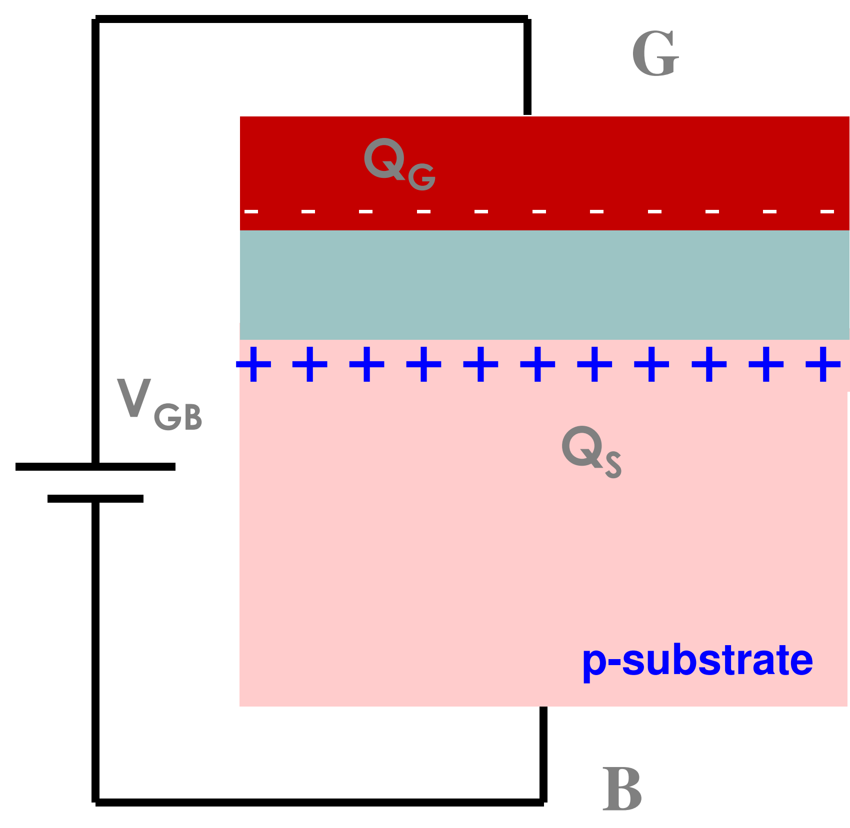
The effect of contact potential and oxide charges can be counterbalanced by applying a gate-bulk voltage called the flat-band voltage V_{FB}.



The potential balance equation then becomes

$$V_G - V_{FB} = \phi_s - \frac{Q_S}{C_{ox}}$$

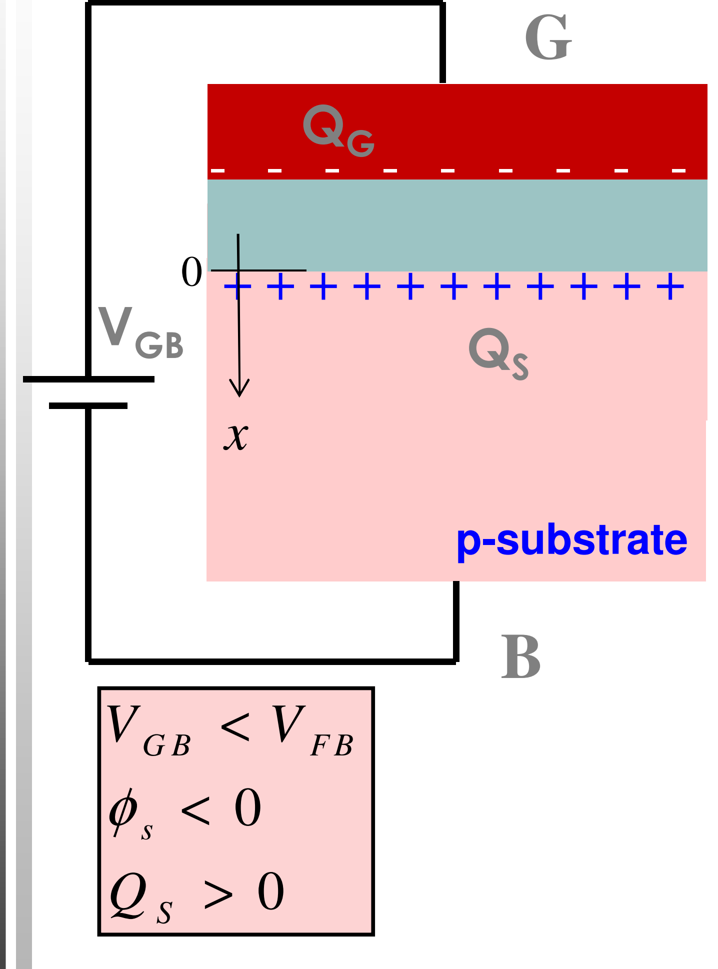
Regions of operation of the MOSFET: Accumulation (p-substrate)



$$V_{GB} < V_{FB}$$
$$\phi_s < 0$$
$$Q_S > 0$$

Holes + accumulate in the p-type semiconductor surface

Accumulation (p-substrate)



ρ

0

$-t_{ox}$

0

x

E

0

$-t_{ox}$

0

E_S

E_{ox}

x

φ

0

$-t_{ox}$

0

x

$V_{GB}-V_{FB}$

$$p = N_a e^{-\frac{q\phi(x)}{kT}}$$

log p, n

p

Na

n

$\frac{n_i^2}{N_a}$

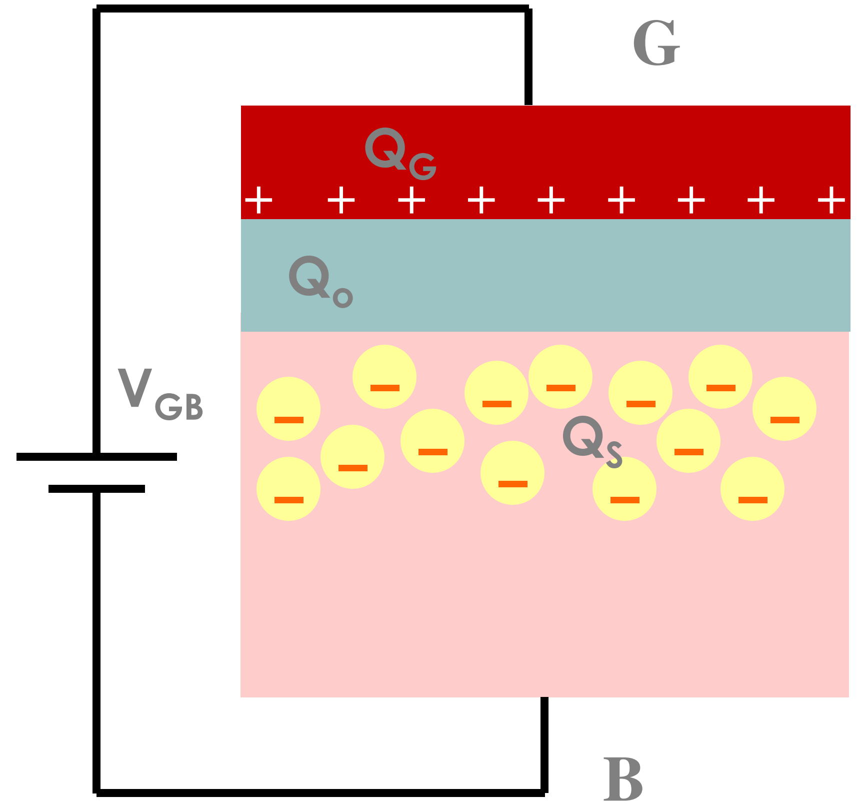
$-t_{ox}$

0

x

$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}}$$

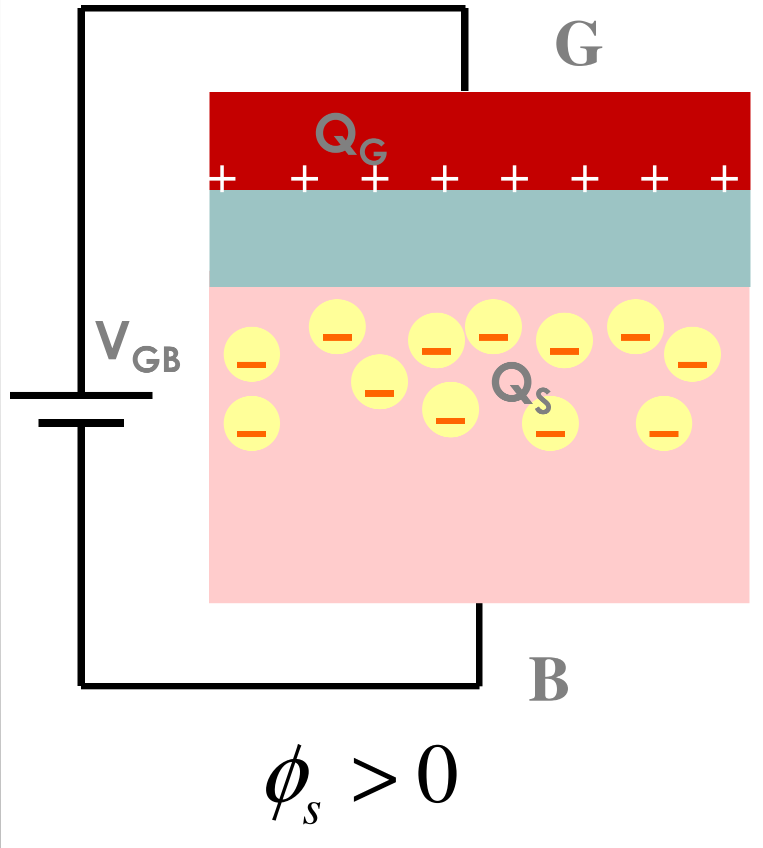
Regions of operation of the MOSFET: Depletion (p-substrate)



$$V_{GB} > V_{FB}$$
$$\phi_s > 0$$
$$Q_S < 0$$

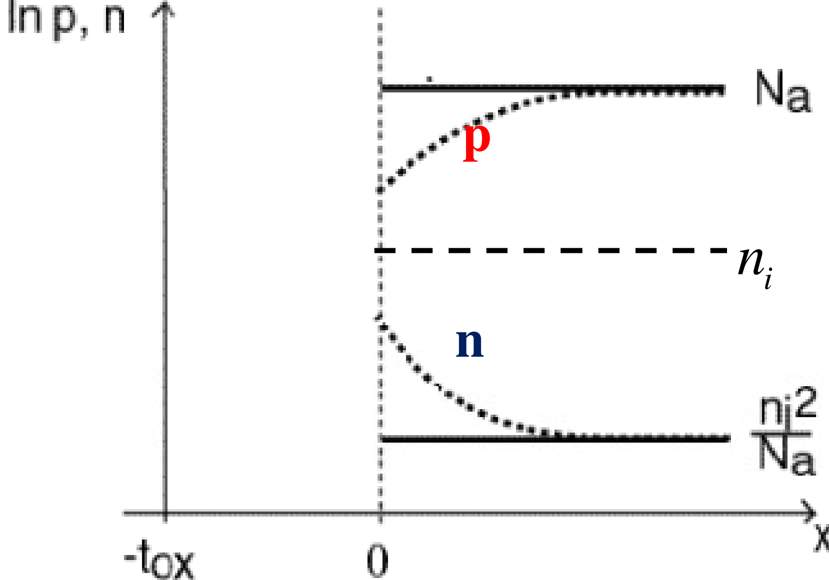
Holes evacuate from the P semiconductor surface and acceptor ion charges – become uncovered

Depletion (p-substrate)



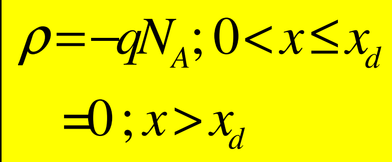
$$\phi_s > 0$$

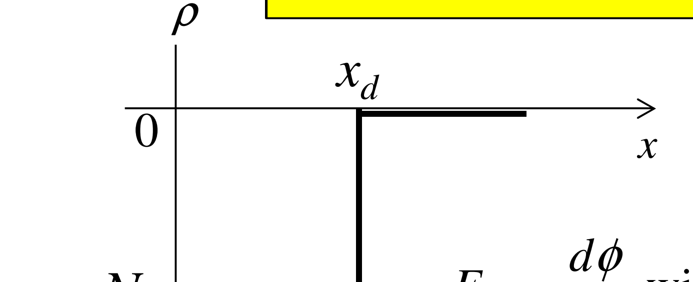
$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}} \qquad p = N_a e^{-\frac{q\phi(x)}{kT}}$$

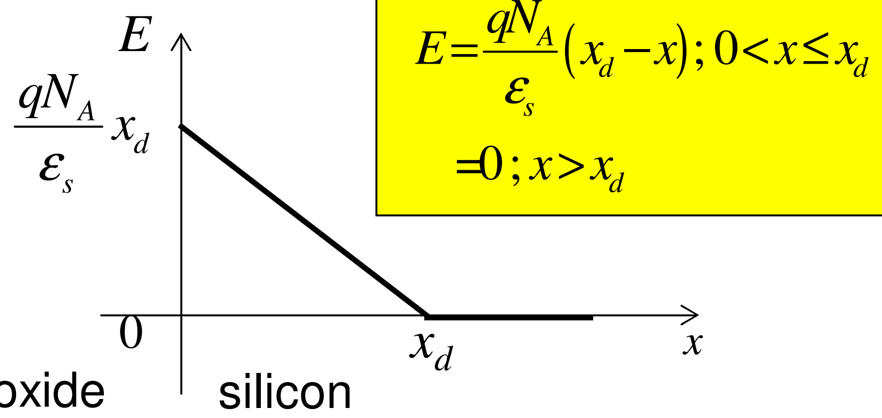


Regions of operation: Depletion (p-substrate)

(depletion approx.)

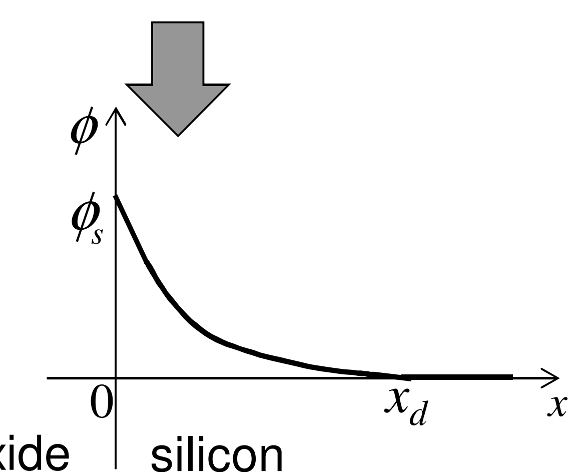






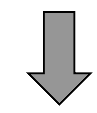
$$E = -\frac{d\phi}{dx} \text{ with } \phi(x_d) = 0 \rightarrow \phi(x) = \frac{qN_A}{2\varepsilon_s}(x_d - x)^2$$

$$\phi(x=0) = \phi_s = \frac{qN_A}{2\varepsilon_s} x_d^2$$



$$Q_D \cong -qN_A x_d = -\sqrt{2q\varepsilon_s N_A \phi_s} = -\gamma C_{ox}\sqrt{\phi_s}$$

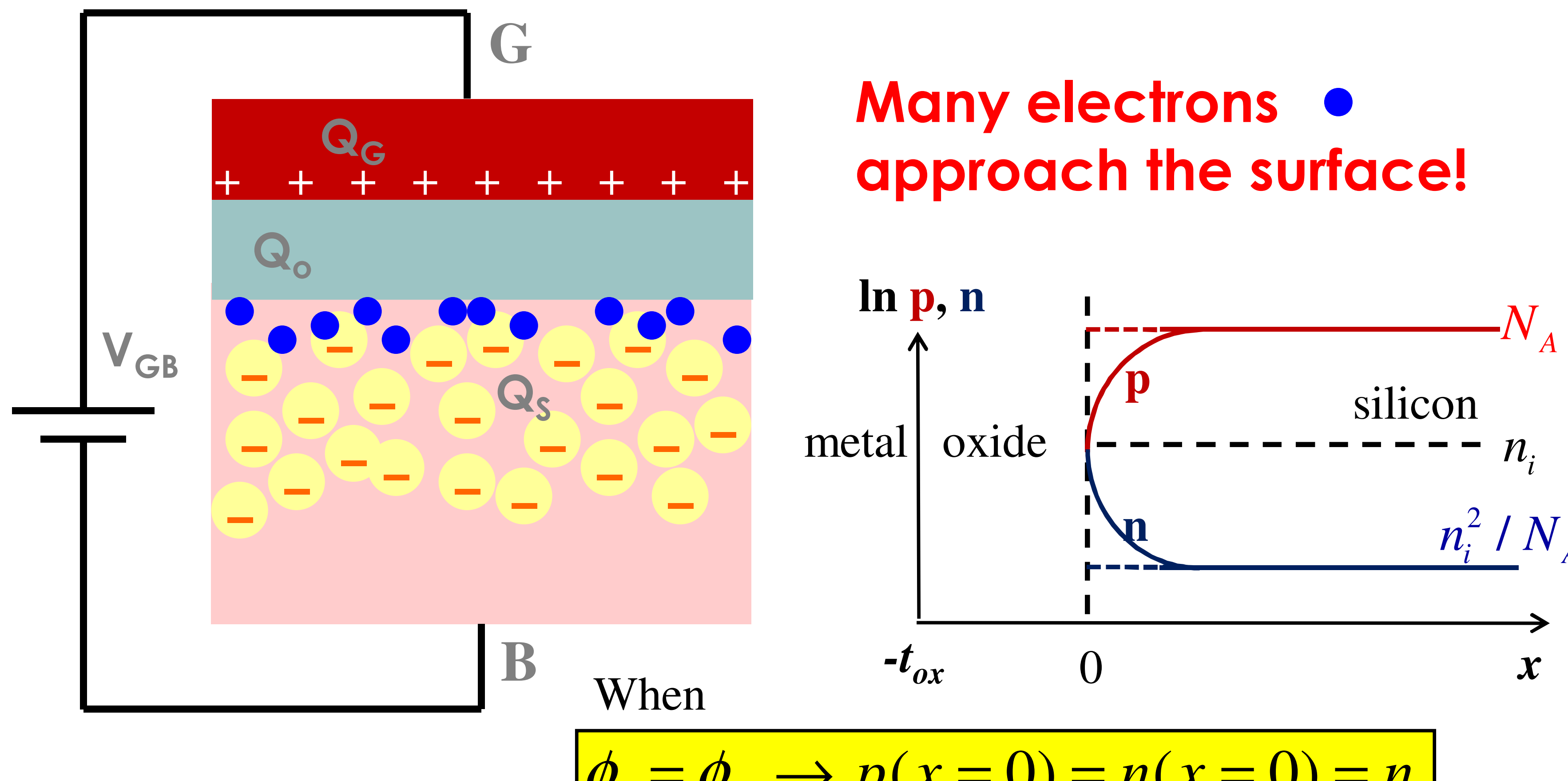
$$\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox}$$



Body effect factor

Regions of operation of the MOSFET: Inversion (p-substrate)

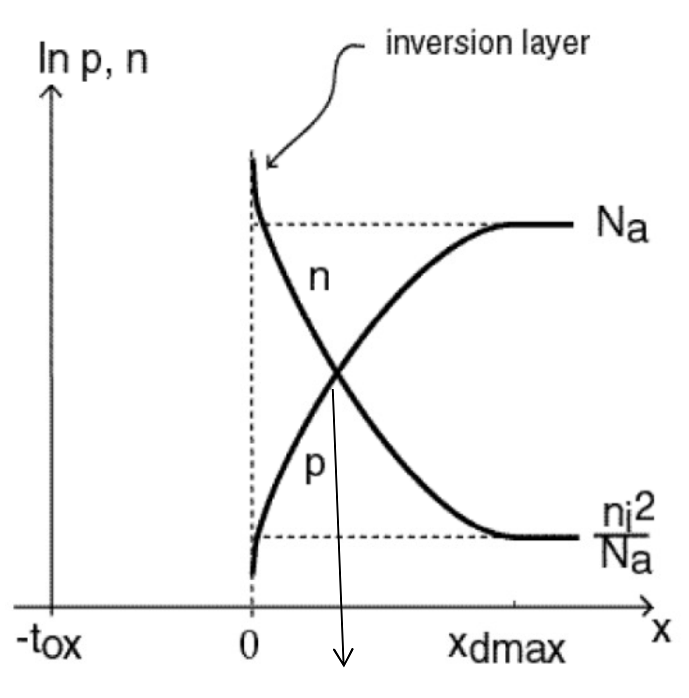
$$\phi_s > \phi_F$$
$$Q_S < 0$$



When

$$\phi_s = \phi_F \rightarrow p(x=0) = n(x=0) = n_i$$

Regions of operation of the MOSFET - Inversion (p-substrate): $\phi_s > \phi_F$ **Φ_F is the Fermi potential**



$$p = N_a e^{-\frac{q\phi(x)}{kT}}$$

$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}}$$

$$n(\phi = \phi_F) = n_i = \frac{n_i^2}{N_a} e^{\frac{q\phi_F}{kT}} \rightarrow \phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i}$$

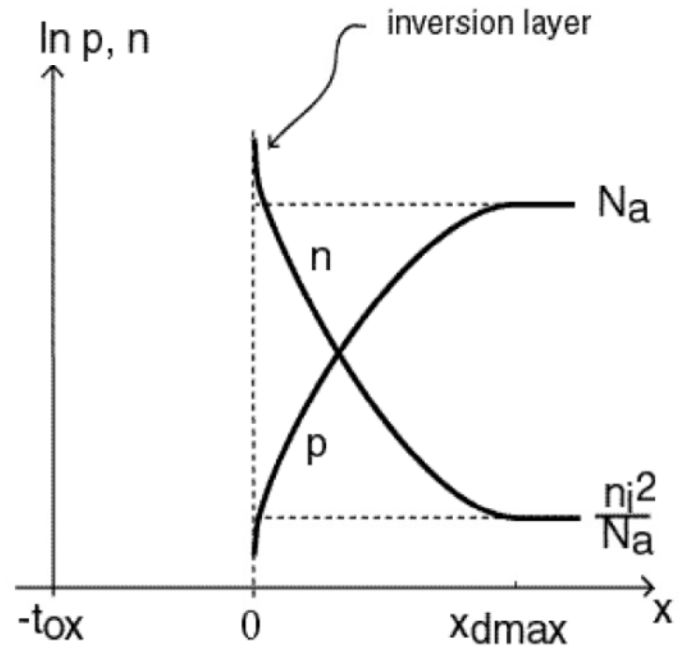
At this point

$p=n=n_i$ and $\phi=\phi_F$

The semiconductor operates in inversion when $\phi_S>\phi_F$

For $\phi>\phi_F$ the concentration of minority carriers (n) at the semiconductor-oxide interface becomes higher than that of majority carriers (p); the semiconductor operates in the inversion region

Strong inversion : the concentration of minority carriers (n) becomes higher than that of holes (majority carriers) deep in the bulk



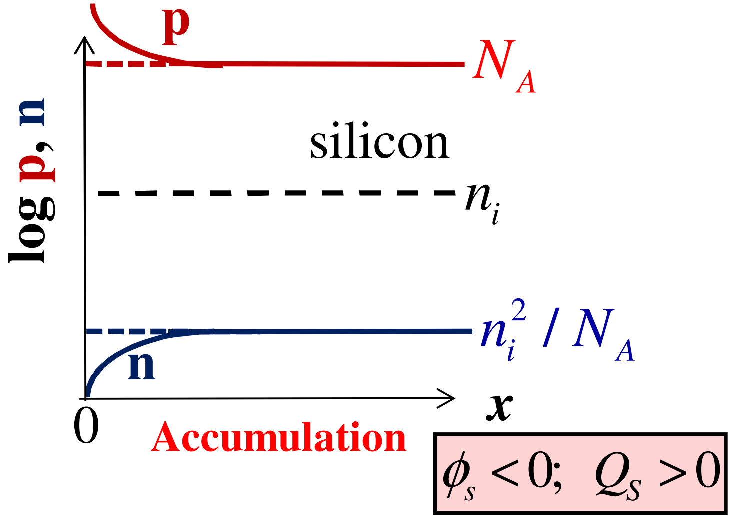
$$p = N_a e^{-\frac{q\phi(x)}{kT}}$$

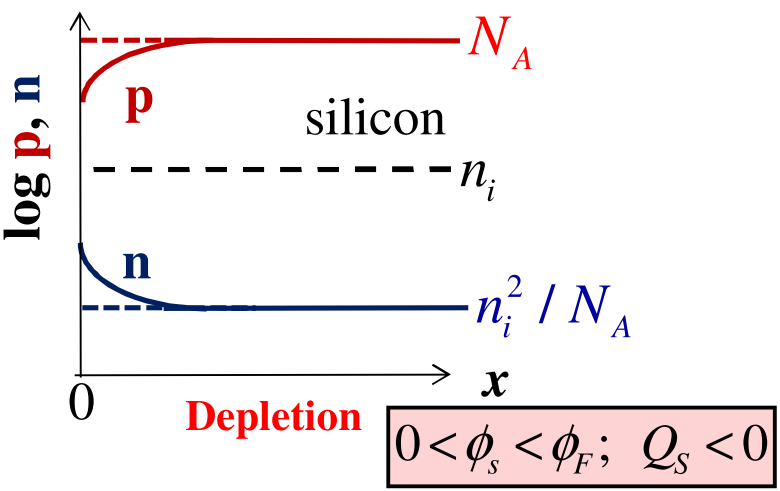
$$n = \frac{n_i^2}{N_a} e^{\frac{q\phi(x)}{kT}}$$

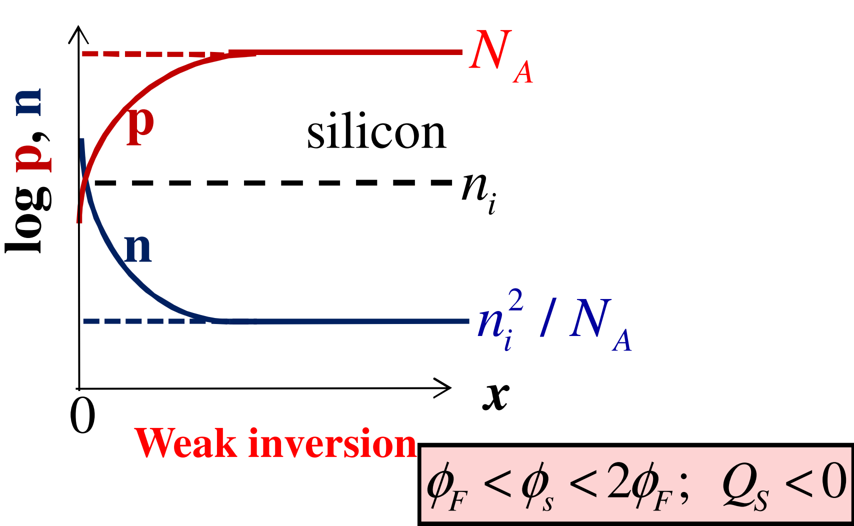
$$n = N_a = \frac{n_i^2}{N_a} e^{\frac{q\phi}{kT}} \rightarrow \phi = 2\frac{kT}{q}\ln\frac{N_a}{n_i} = 2\phi_F$$

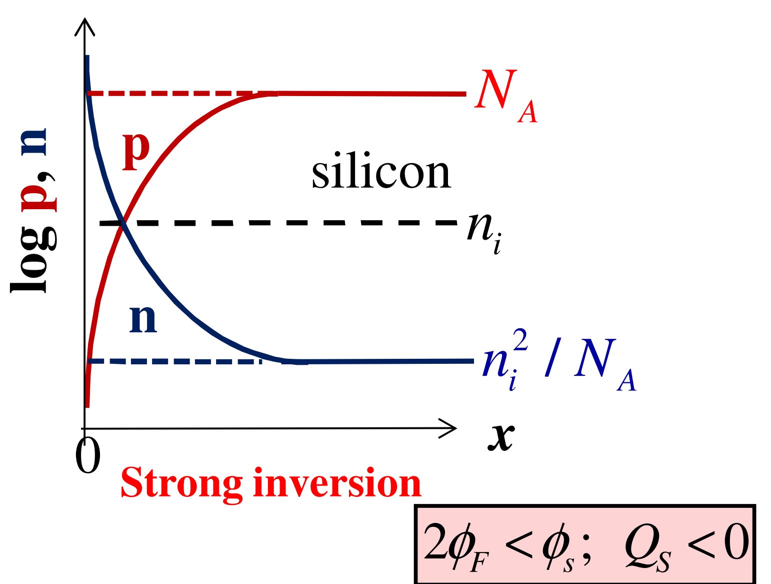
The semiconductor operates in strong inversion when $\phi_S > 2\phi_F$

Operating regions of the MOSFET: Summary









What is n(x) and p(x) if $V_{GB}=V_{FB}$?

Threshold voltage V_T (for strong inversion)

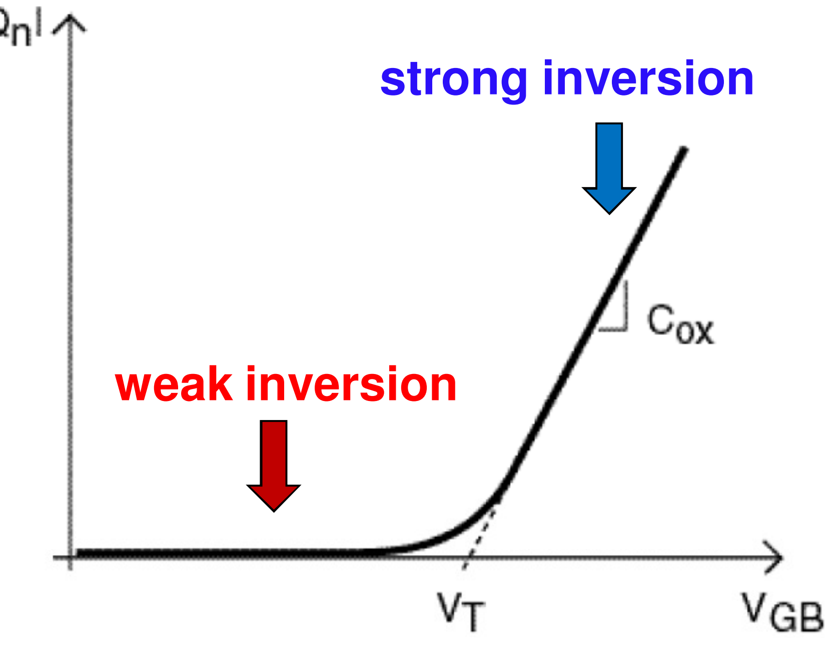
Gate voltage for which $\phi_s = 2\phi_F$

$$V_T = V_{GB}\big|_{\phi_s = 2\phi_F} \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

$$Q_D \cong -qN_A x_d = -\sqrt{2q\varepsilon_s N_A \phi_s} = -\gamma C_{ox}\sqrt{2\phi_F}$$

$\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox} \longrightarrow$ **Body effect factor**

$$Q_N = -C_{ox}\left(V_{GB} - V_T\right)$$



Small-signal equivalent circuit of the MOS capacitor in weak inversion

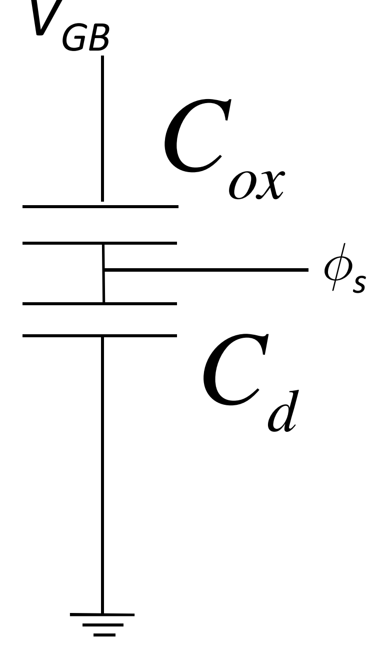
$$C_{gb} = \frac{dQ_G}{dV_{GB}} = -\frac{dQ_S}{dV_{GB}} = -\frac{dQ_S}{d\phi_s - \frac{dQ_S}{C_{ox}}} = \frac{1}{-\frac{d\phi_s}{dQ_S} + \frac{1}{C_{ox}}}$$

$$V_{GB} - V_{FB} = \phi_s - Q_S / C_{ox}$$

In weak inversion $Q_N/Q_D \ll 1$

$$C_s = -\frac{dQ_S}{d\phi_s} = -\frac{d\left(Q_D + Q_N\right)}{d\phi_s} \cong -\frac{dQ_D}{d\phi_s} = C_d$$

C_d: depletion capacitance



$$C_{gb} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_d}}$$

Weak inversion model of the MOS device

$$Q_D \cong -\gamma C_{ox}\sqrt{\phi_s} \rightarrow C_d = -\frac{dQ_D}{d\phi_s} \cong \frac{\gamma C_{ox}}{2\sqrt{\phi_s}} = (n-1)C_{ox}$$

n (slope factor), a dimensionless factor, is a function of ϕ_s , but let us assume it is a constant.

$$\frac{d\phi_s}{dV_{GB}} = \frac{C_{ox}}{C_{ox}+C_d} = \frac{1}{n} \qquad \text{(I)}$$

depletion region

V_{GB}

ϕ_s

p- type neutral region

V_{GB}

C_{ox}

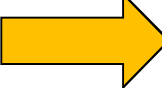
ϕ_s

C_d

Integrating (I) between ϕ_s and $\phi_s = 2\phi_F$ ($V_{GB}=V_T$) leads to

$$\phi_s = 2\phi_F + \frac{1}{n}\left(V_{GB} - V_T\right)$$

Boltzmann statistics applied to the electron charge density (Q_N)

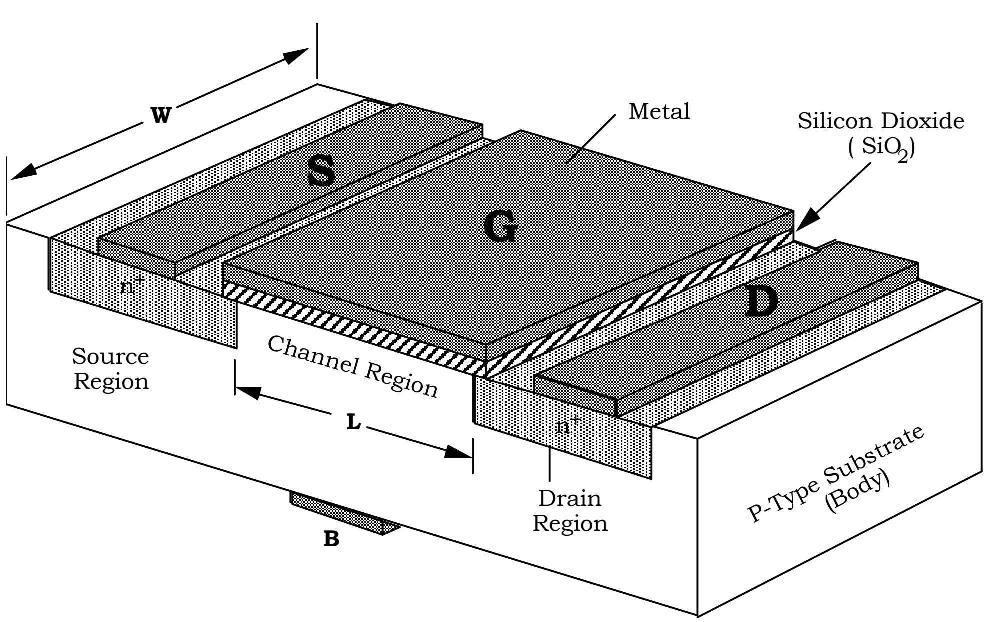


$$Q_N \propto \exp\left(\frac{\phi_s}{\phi_t}\right) \propto \exp\left(\frac{V_{GB}-V_T}{n\phi_t}\right)$$

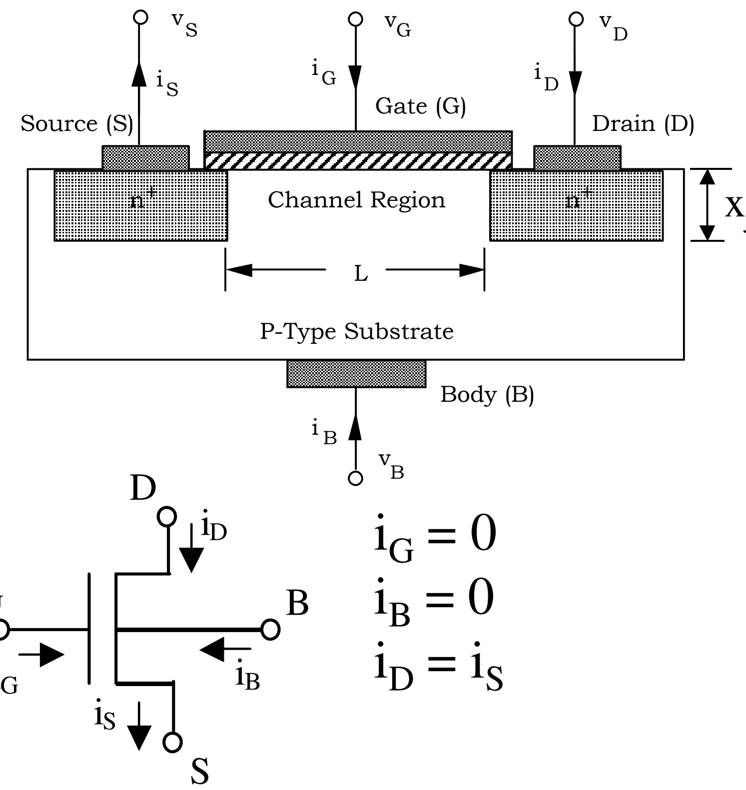
Note: The symbol *n* has been used for both electron concentration and slope factor.

5.2 The Enhancement-Type NMOS Transistor

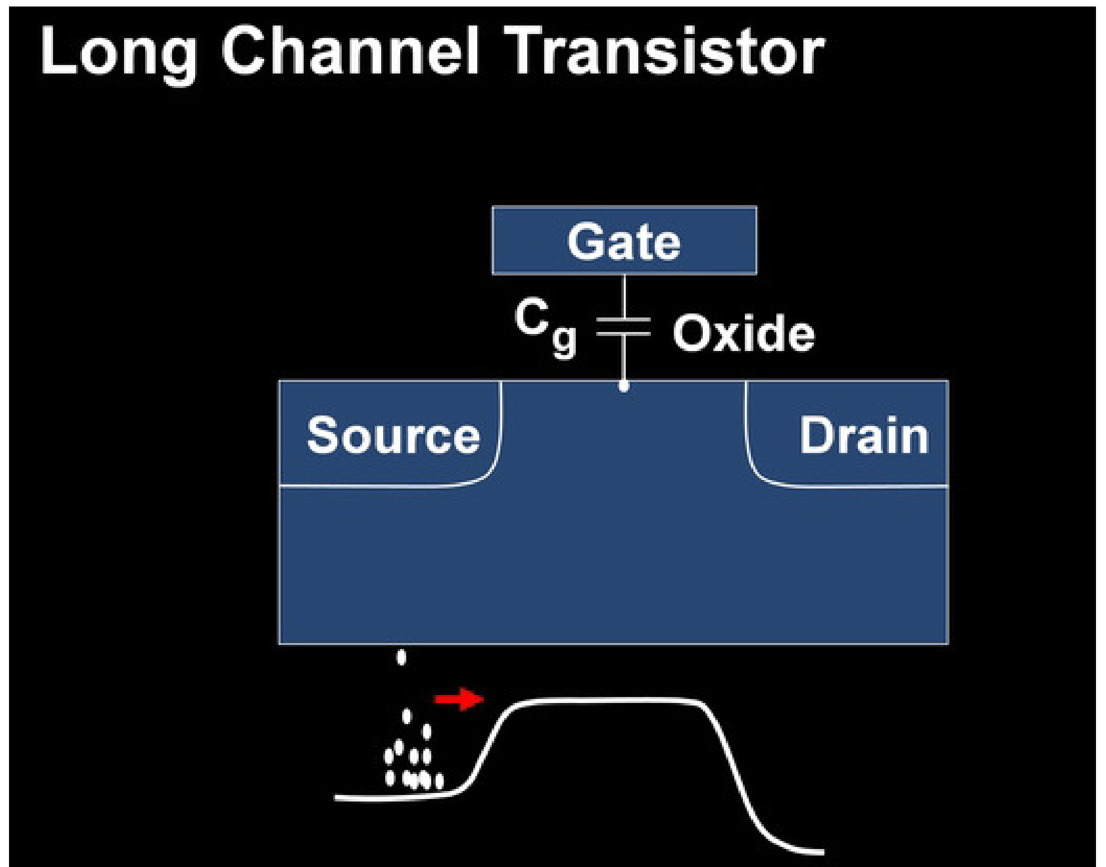
0.8 μ CMOS technology
$L_{min} = 0.8\ \mu m$ metal width $\geq 1.4\ \mu m$
$W_{min} = 2.0\ \mu m$
$t_{ox} = 160$ Å
$X_j = 0.40\ \mu m$



(a) NMOS transistor structure (b) cross section and (c) circuit symbol



$i_G = 0$
$i_B = 0$
$i_D = i_S$



Energy barrier at source controlled by both source and gate voltages

Energy barrier at drain controlled by both drain and gate voltages

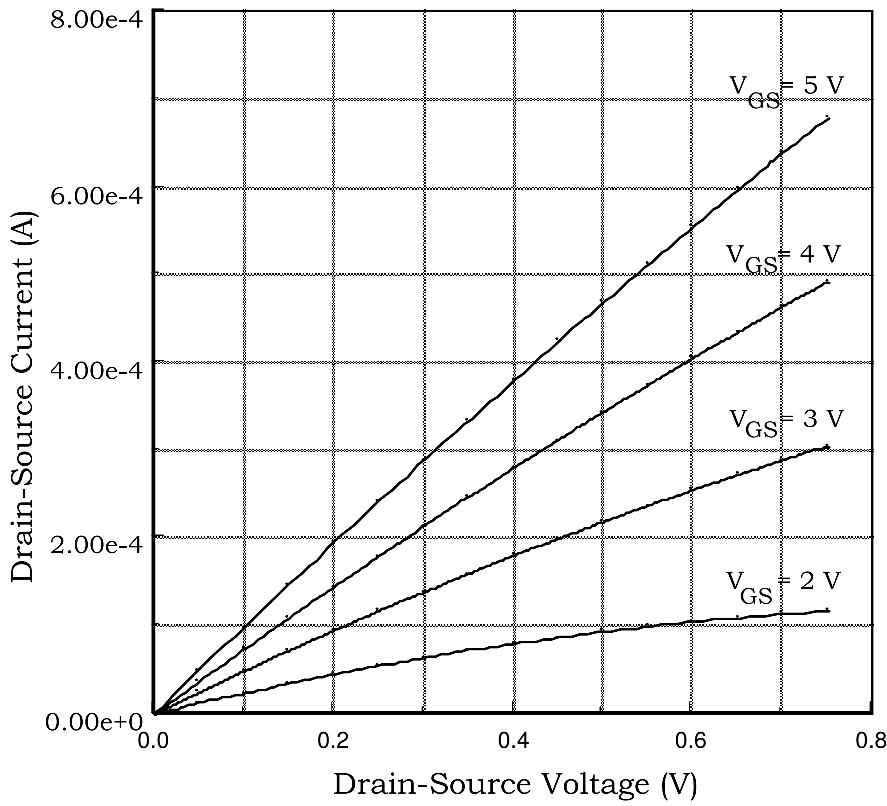
3D FinFET
New Structure Rejuvenates Transistor!
Dr. Chenming Hu
University of California Berkeley
http://www.eecs.berkeley.edu/~hu/

http://www.synopsys.com/Community/SNUG/Silicon%20Valley/Pages/snug-2012-keynote-3d-finfet.aspx

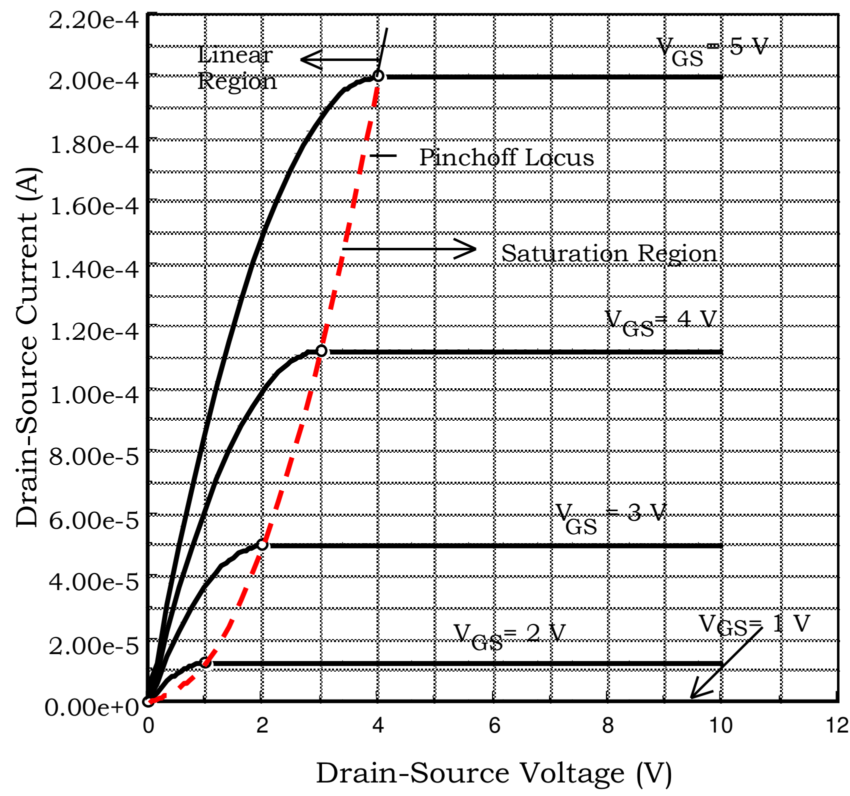
$$I_D = \frac{W}{L}\mu C_{ox}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right]$$

$V_{GS} \geq V_T$
$V_{DS} \leq V_{DSSAT}$

For small V_{DS}: $I_D \cong \frac{W}{L}\mu C_{ox}(V_{GS}-V_T)V_{DS}$ and $\frac{dI_D}{dV_{DS}} = \frac{W}{L}\mu C_{ox}(V_{GS}-V_T)$



NMOS i-v characteristics in the linear region (V_{SB} = 0)



$$I_D \approx 0 \quad for \quad V_{GS} \le V_T$$

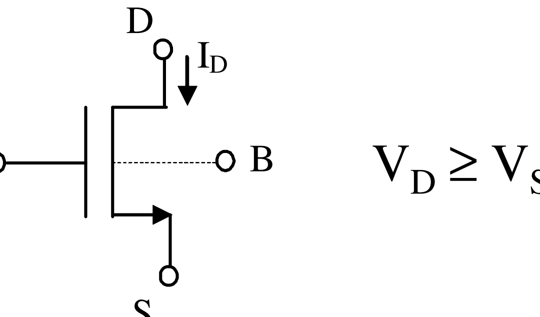
$$I_D = \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$V_{GS} \ge V_T$$
$$V_{DS} \le V_{DSSAT}$$

$$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS} - V_T)^2$$

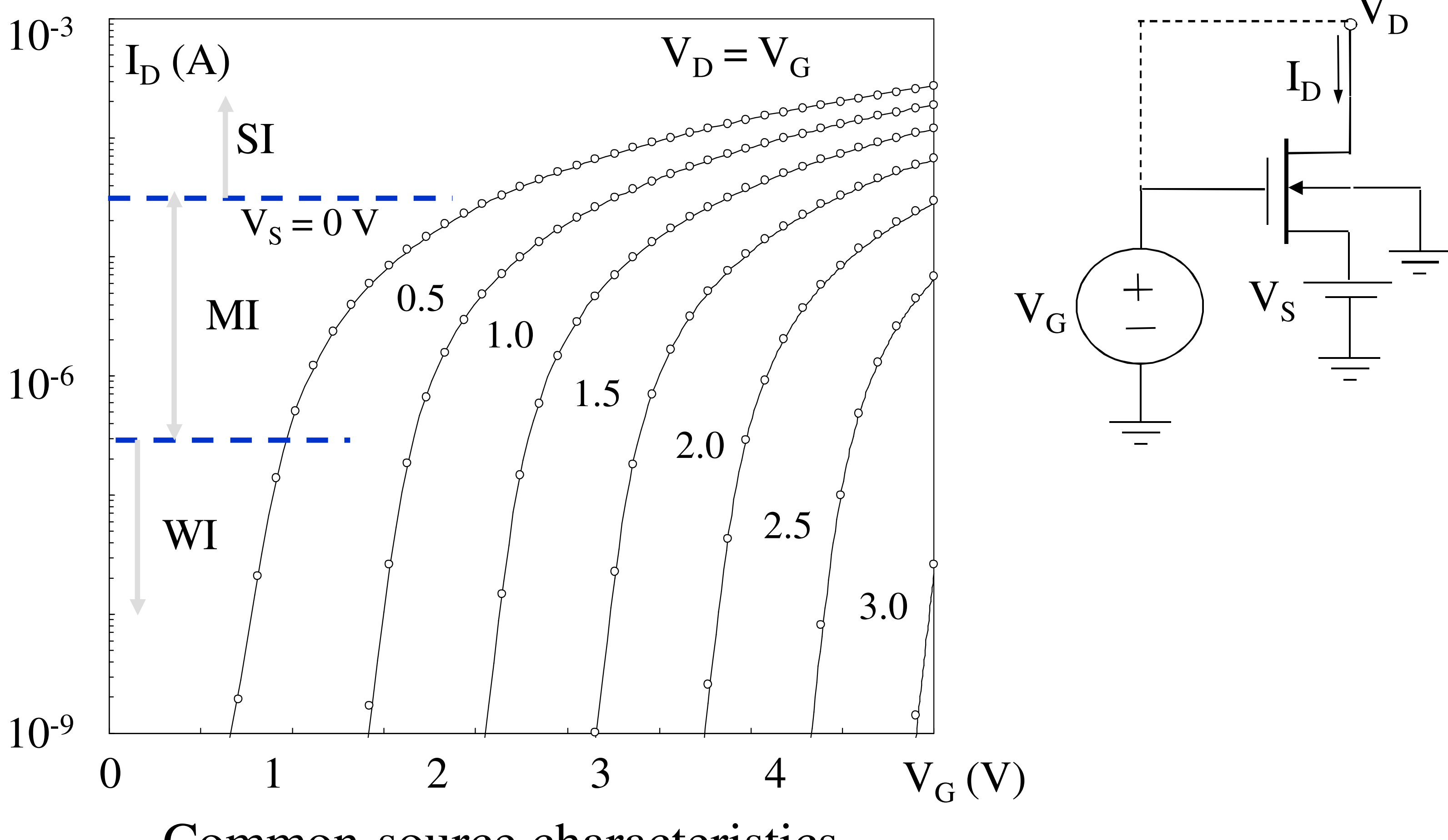
$$V_{GS} \ge V_T$$
$$V_{DS} \ge V_{DSSAT}$$

Output characteristics for an NMOS transistor with $V_{Tn} = 1$ V and $(W/L)\mu_n C_{ox} = 25 \times 10^{-6}$ A / V^2



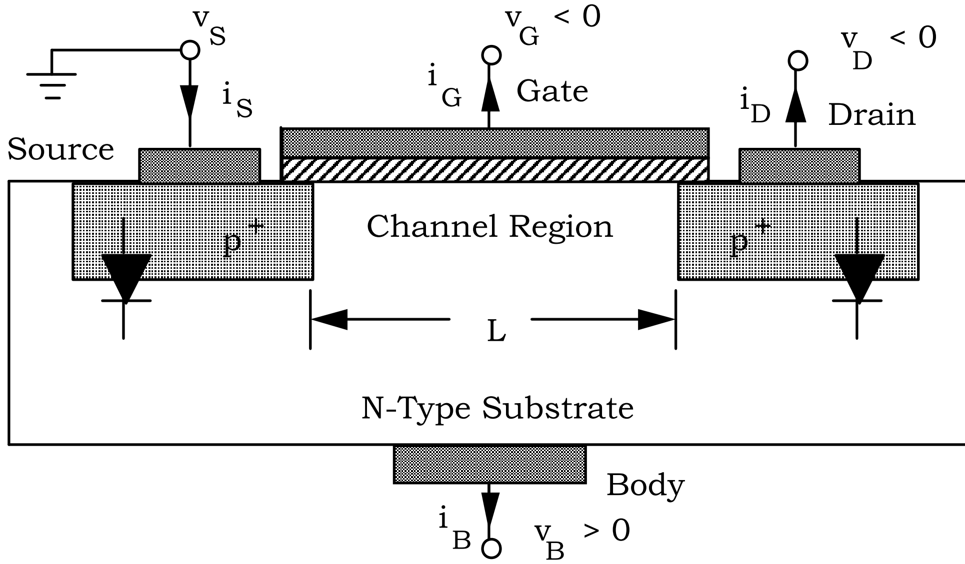
$V_D \ge V_S$

MOSFET I-V RELATIONSHIP

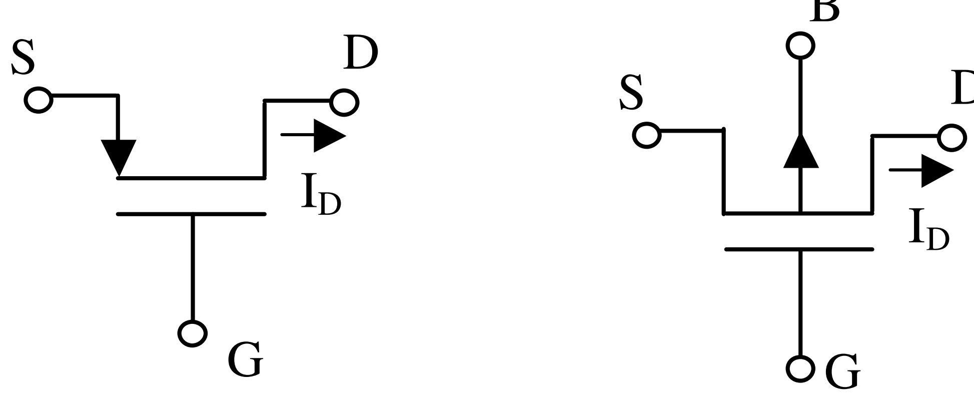


Common-source characteristics

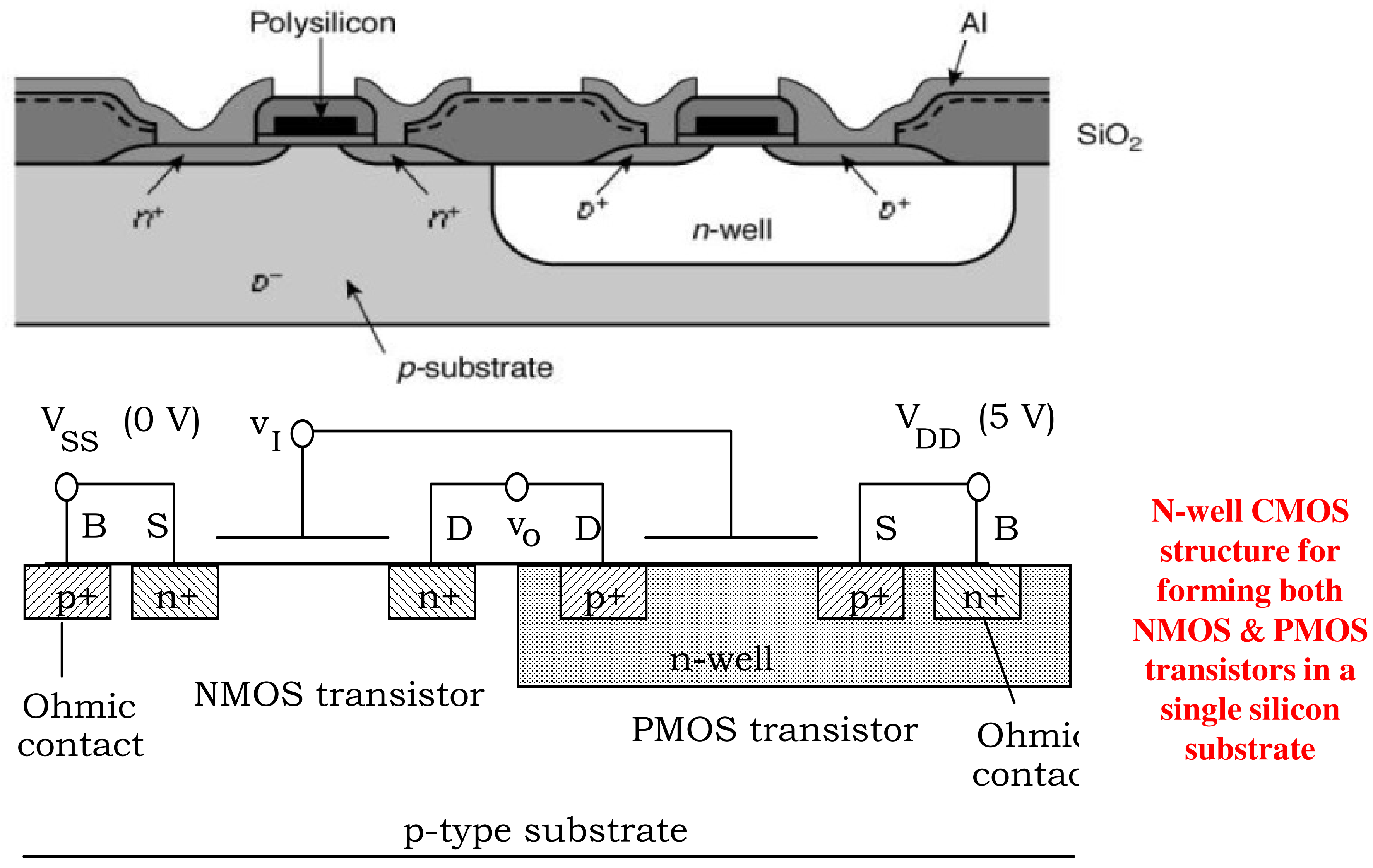
5.4 The PMOS Transistor



Cross section of an enhancement-mode PMOS transistor

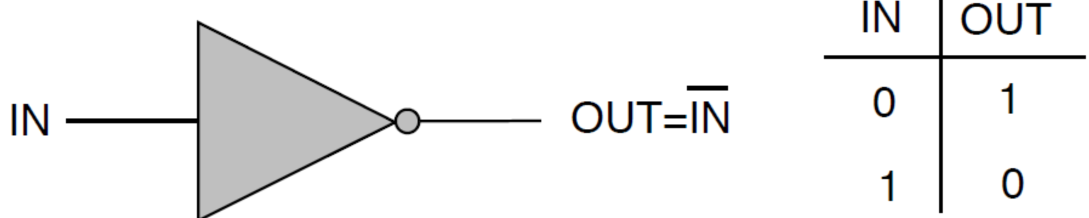


5.4 The CMOS Technology

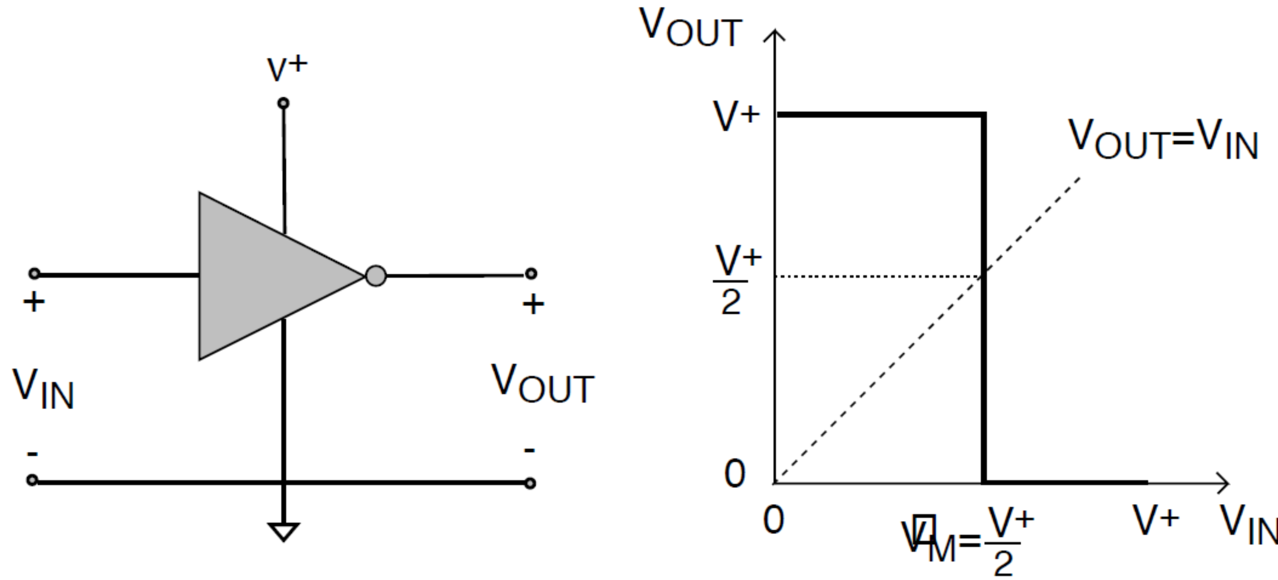


N-well CMOS structure for forming both NMOS & PMOS transistors in a single silicon substrate

5.6 MOS logic circuits: the ideal inverter



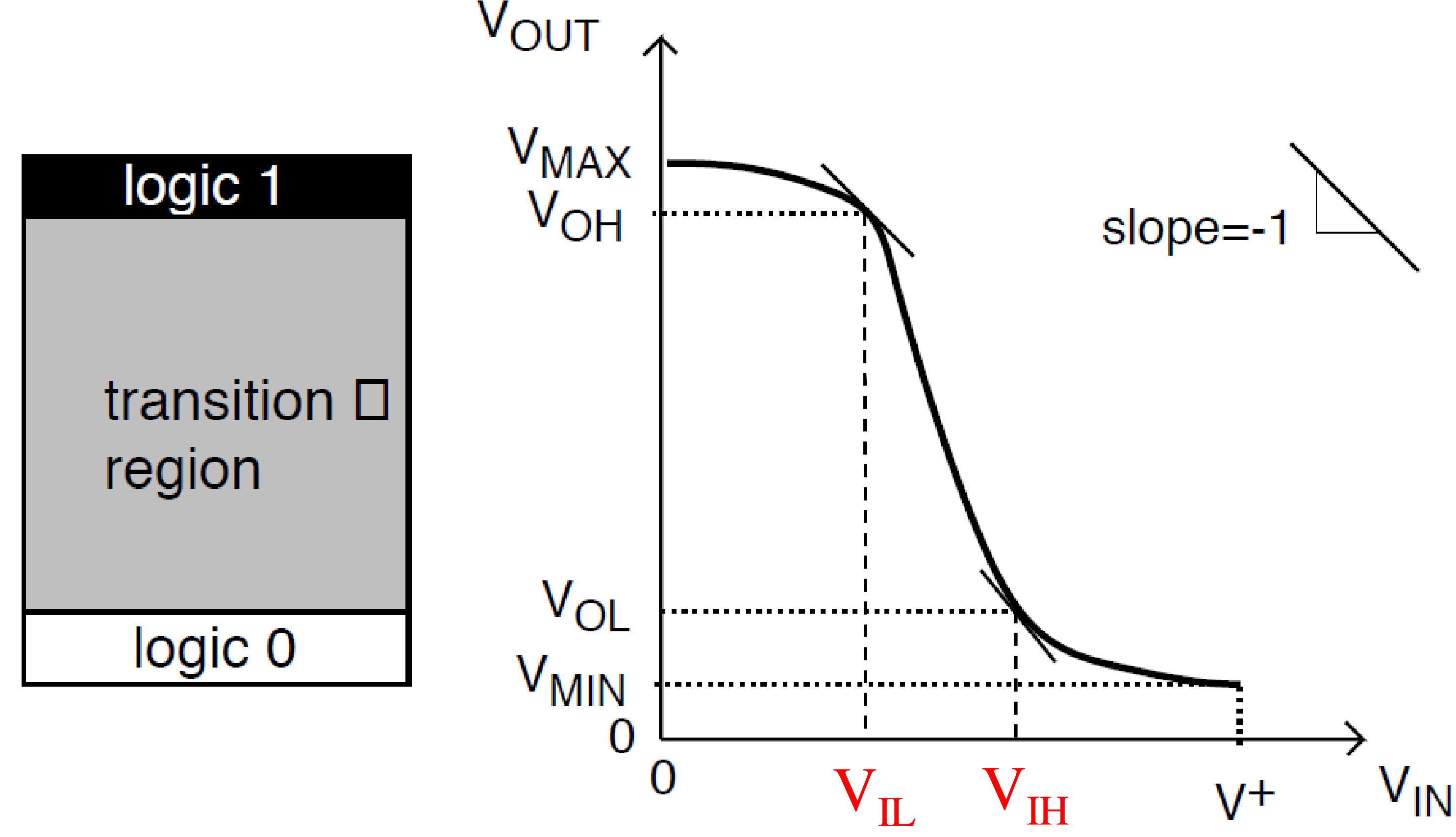
Circuit representation and ideal transfer function:



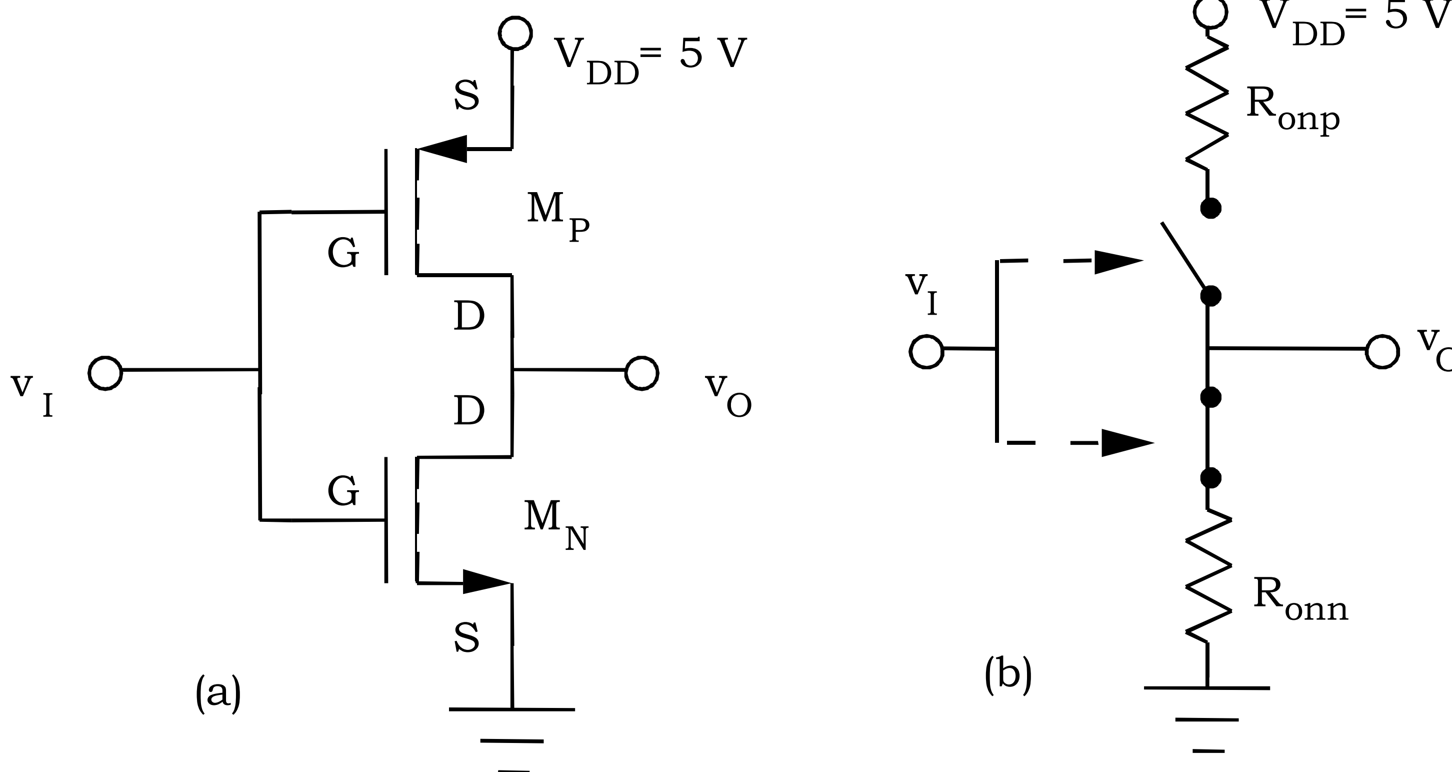
Define ***switching point*** or ***logic threshold*** :

- $V_M \equiv$ input voltage for which $V_{OUT} = V_{IN}$

MOS logic circuits: the real inverter

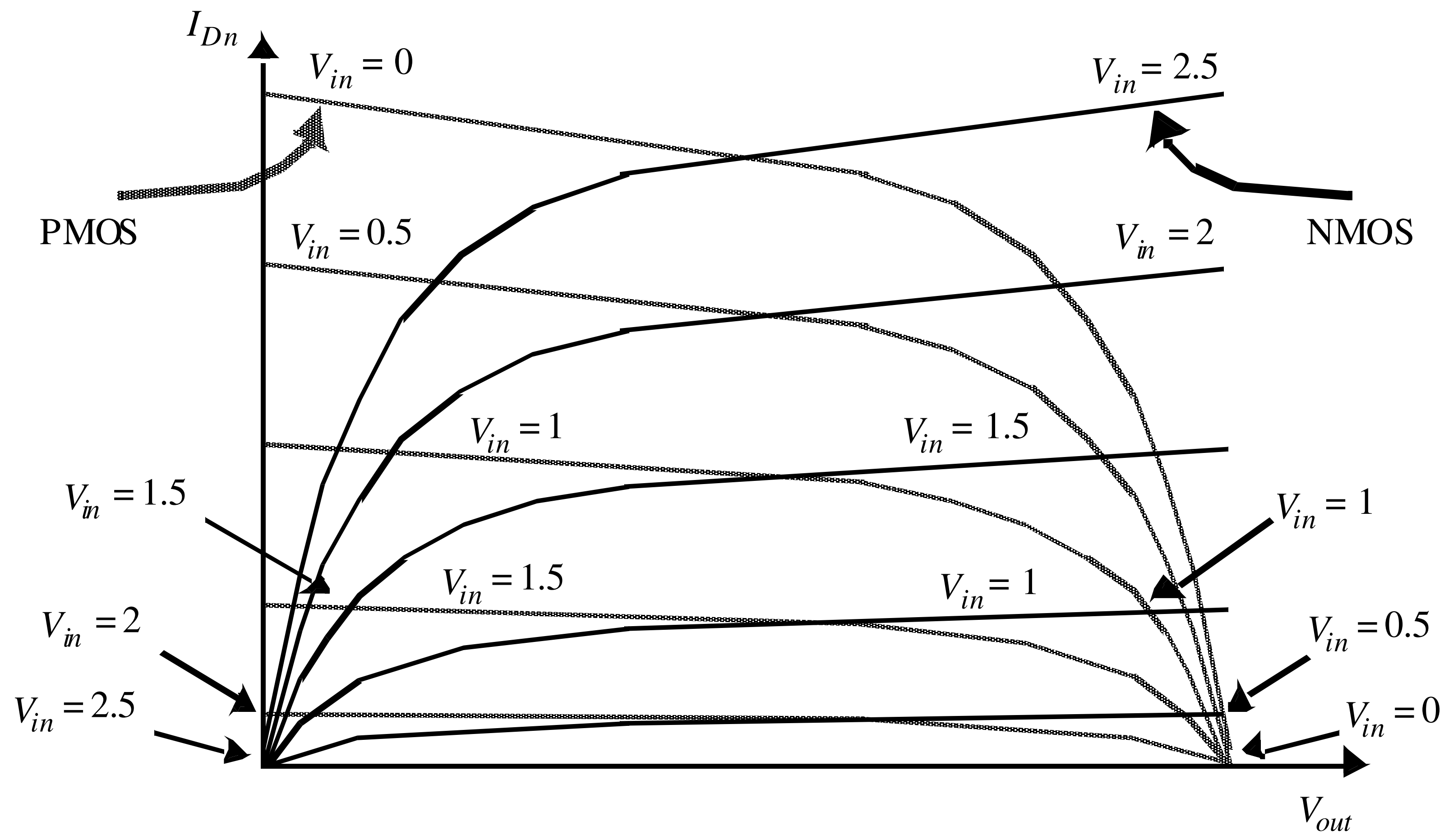


• The CMOS Inverter-I

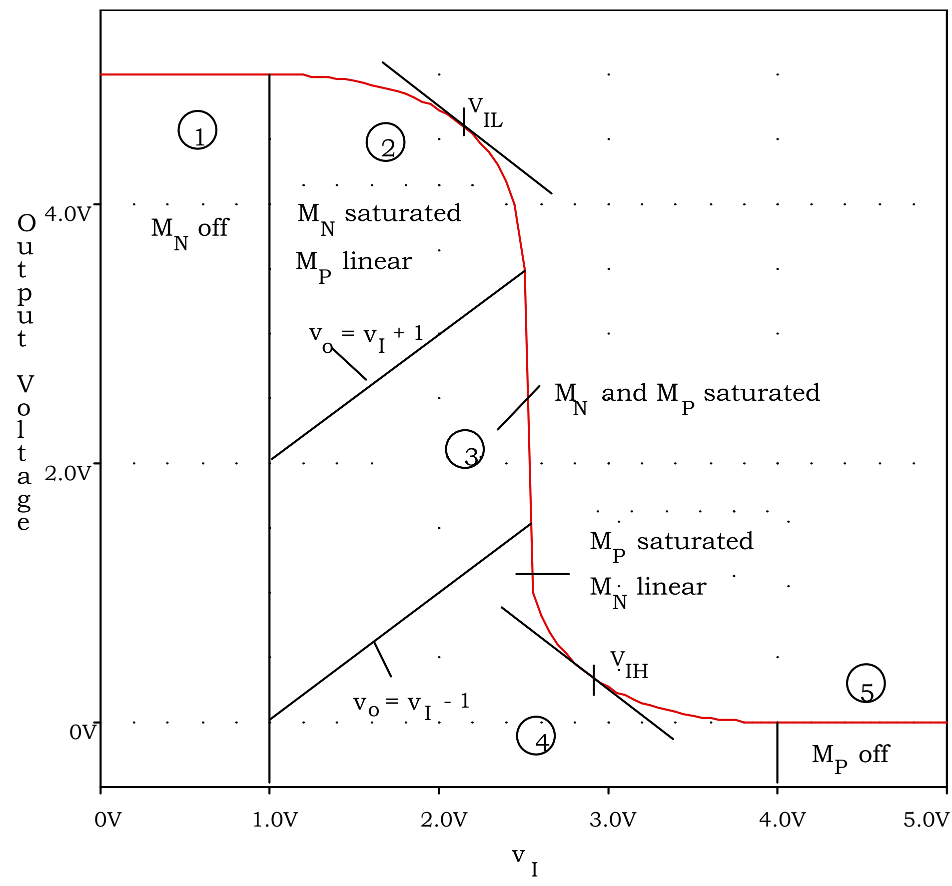


(a) CMOS inverter uses one NMOS and one PMOS transistor
(b) Simplified model for the CMOS logic gate

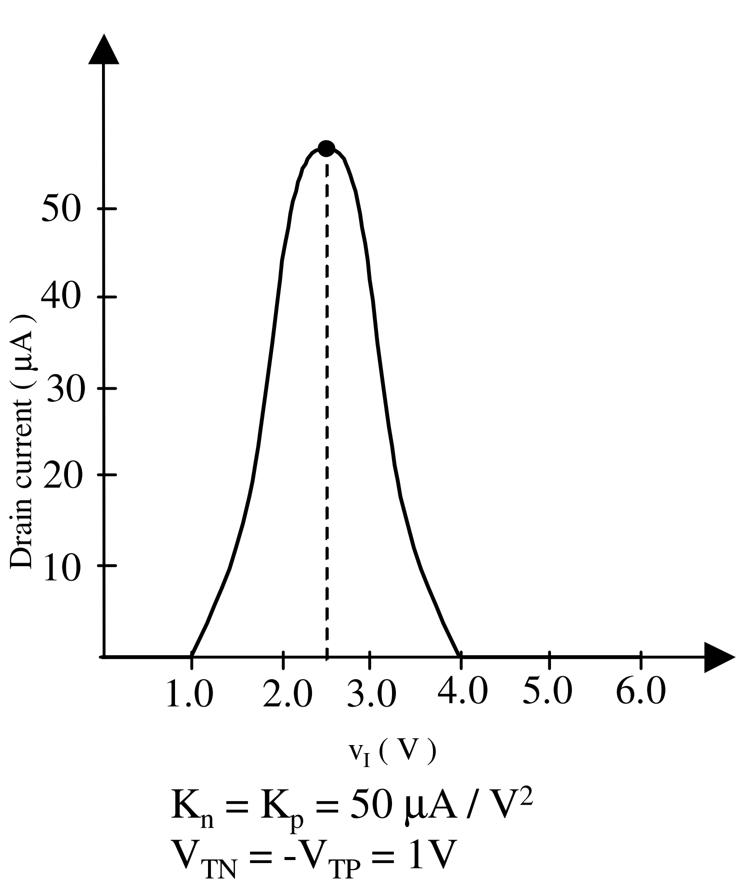
The CMOS Inverter-II



The CMOS inverter: VTC and dc current



CMOS voltage transfer characteristic may be broken down into the five regions outlined in table 8.2

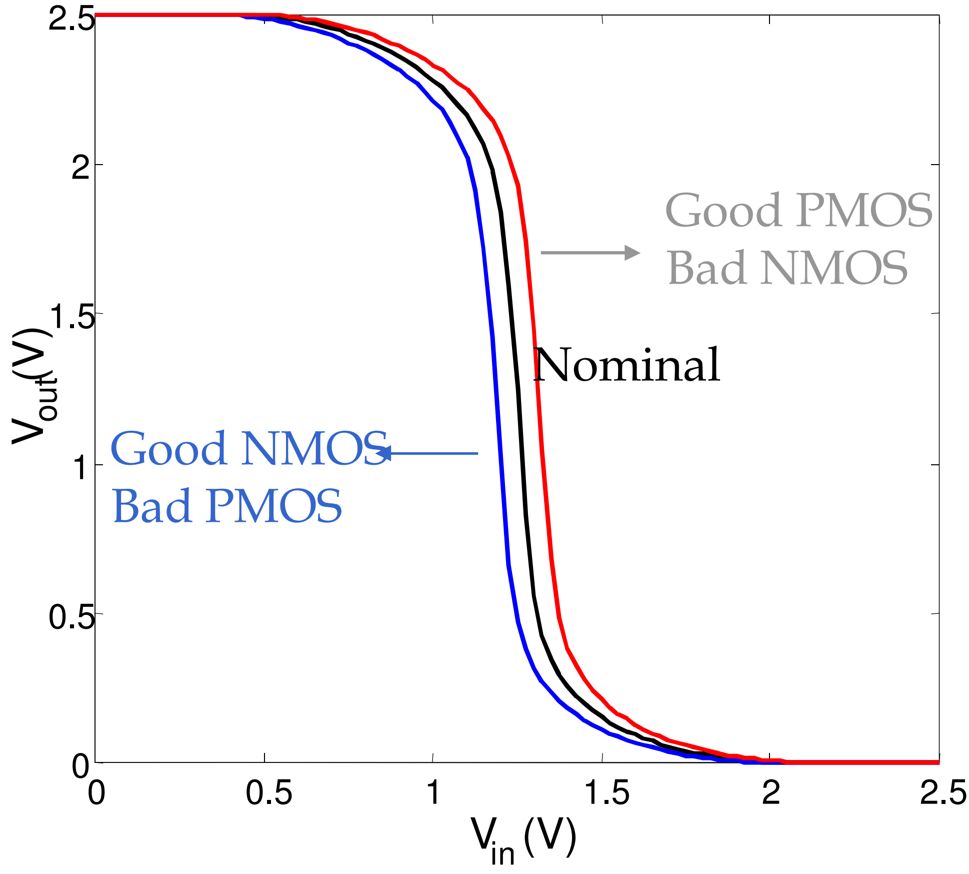


$K_n = K_p = 50\ \mu A / V^2$
$V_{TN} = -V_{TP} = 1V$

$$P_{static} = V_{DD}\ i_{leakage} + V_{DD} i_{sc}$$

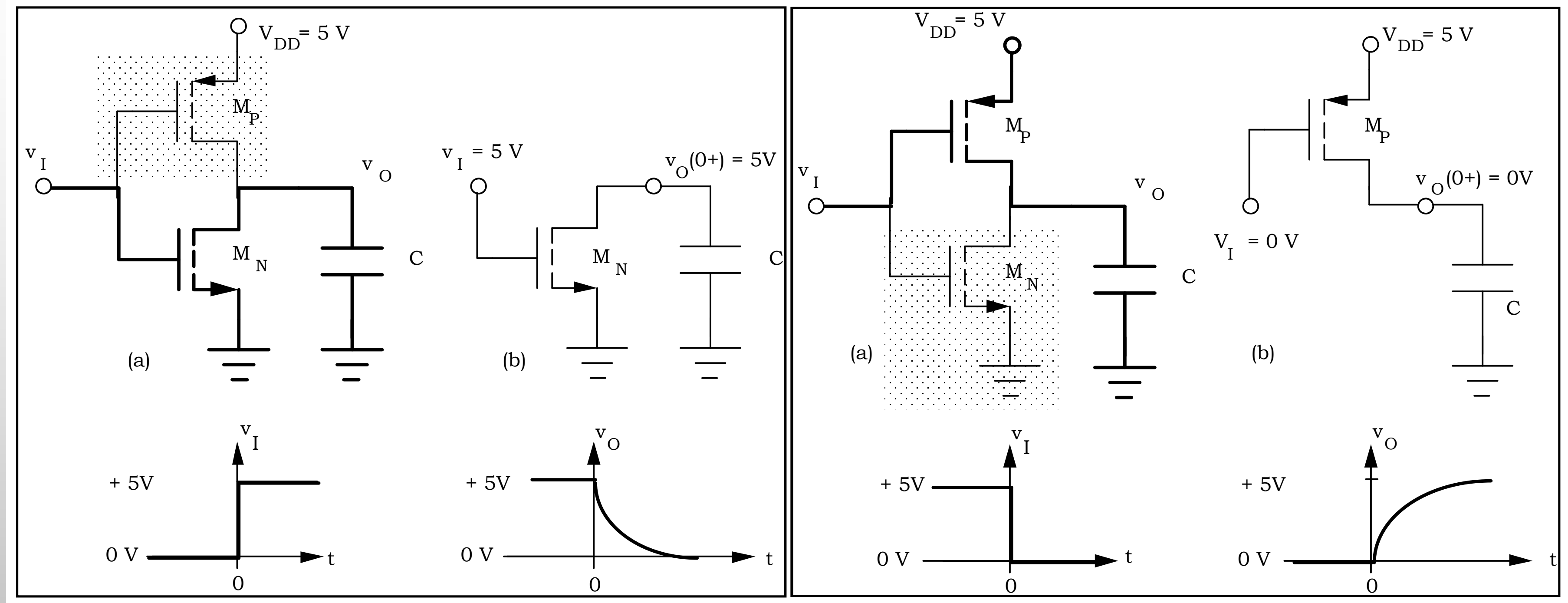
$$P_{short\text{-}circuit} = V_{DD} i_{sc}$$

Impact of Process Variations



Process variations are electrically modeled through variations of parameters (V_T, k_p, k_n, etc…)

• Dynamic Operation of the CMOS Inverter -1

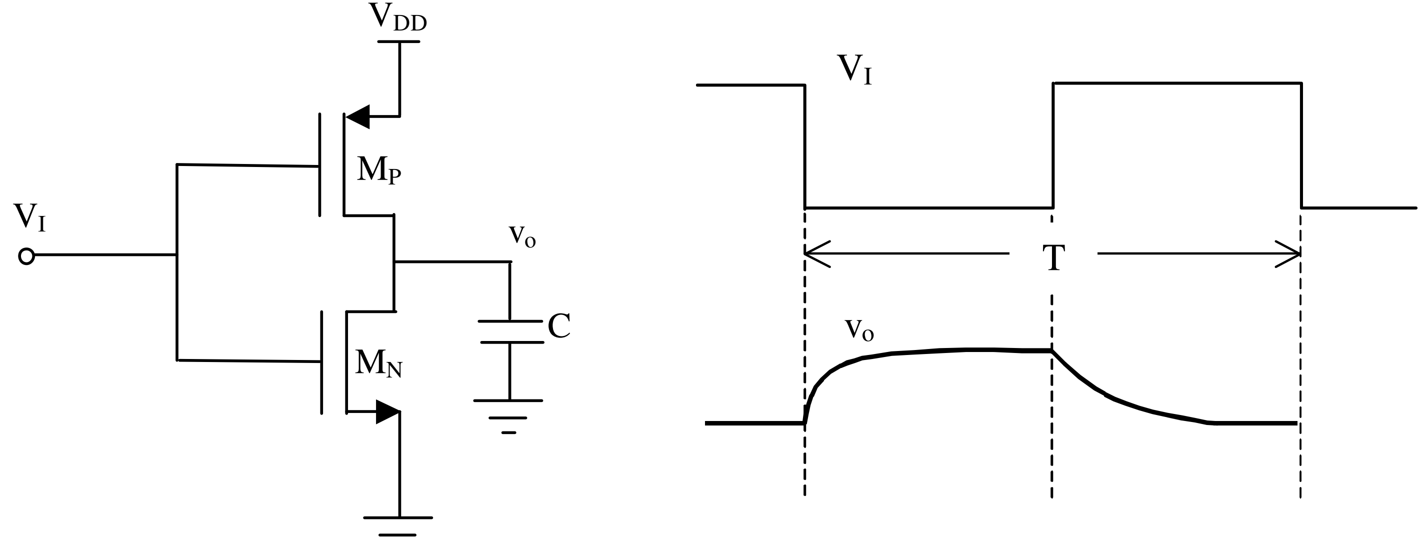


High-to-low output transition in a CMOS inverter

Low -to- high output transition in a CMOS inverter

C: load capacitance + interconnect capacitance + parasitic capacitance of the inverter

• Dynamic Power Dissipation in CMOS Gates - 1



What is the energy dissipation for changing v_o from 0 to V_{DD} and back to 0?

The energy dissipation in M_P when v_o changes from 0 to V_{DD} is

Assumptions: Step v_i, constant C

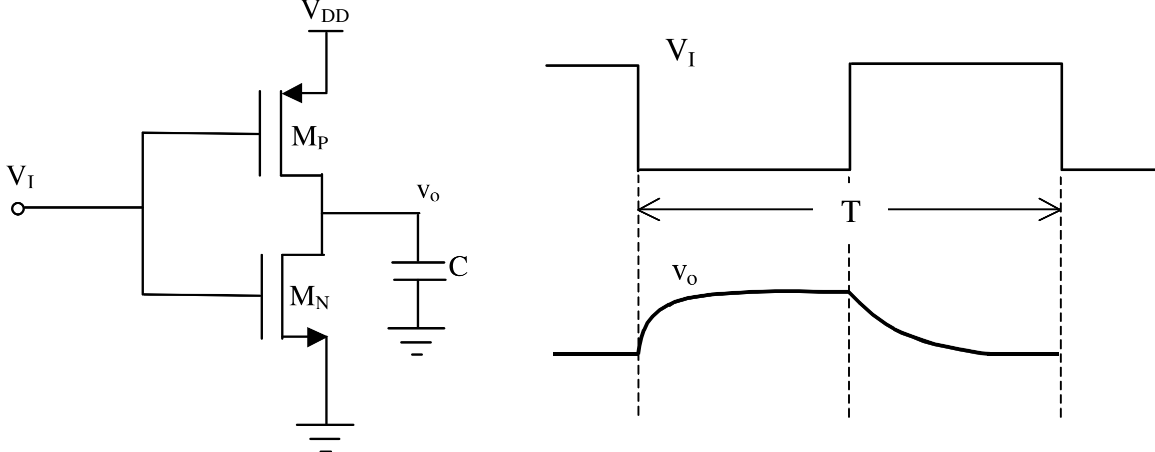
$$E\left(M_p\right) = \int v\left(M_p\right)\, i\left(M_p\right)\, dt = \int \left(V_{DD} - v_o\right)\, dq$$

$$E\left(M_p\right) == C \int_0^{V_{DD}} \left(V_{DD} - v_o\right)\, dv_o = C\, V_{DD}^{\ 2}/2$$

The energy stored in C when $v_o = V_{DD}$ is

$$E_C = C\, V_{DD}^{\ 2}/2$$

• Dynamic Power Dissipation in CMOS Gates - 2



The energy dissipation in M_N when v_o changes from V_{DD} to 0 equals the energy stored in the capacitor before discharging it

$$E\,(M_N) = \int v(M_N)\; i(M_N)\; dt = \int_{V_{DD}}^{0} -v_o C dv_o = \frac{CV_{DD}^{\,2}}{2} = E_C$$

When the operation of charging and discharging the capacitor is repeated each T seconds (or f times per second), the power dissipation is

$$P = \frac{C\,V_{DD}^{\,2}}{T}$$

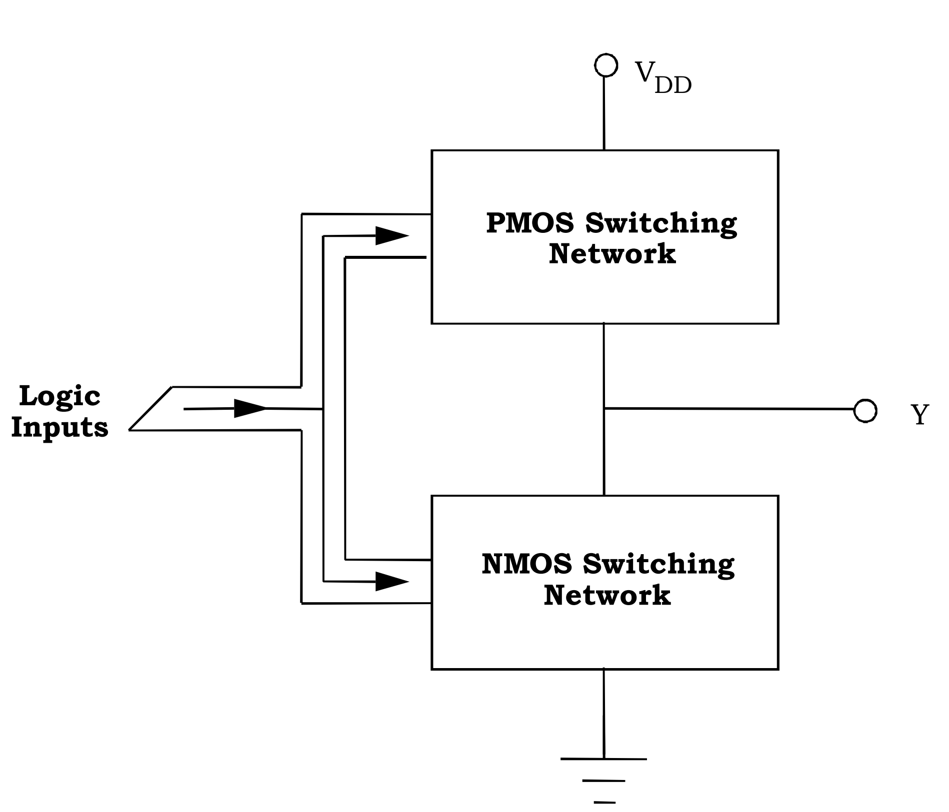
$$\boxed{P = f\;C\;V_{DD}^{\,2}}$$

In general, the average dynamic power dissipation is

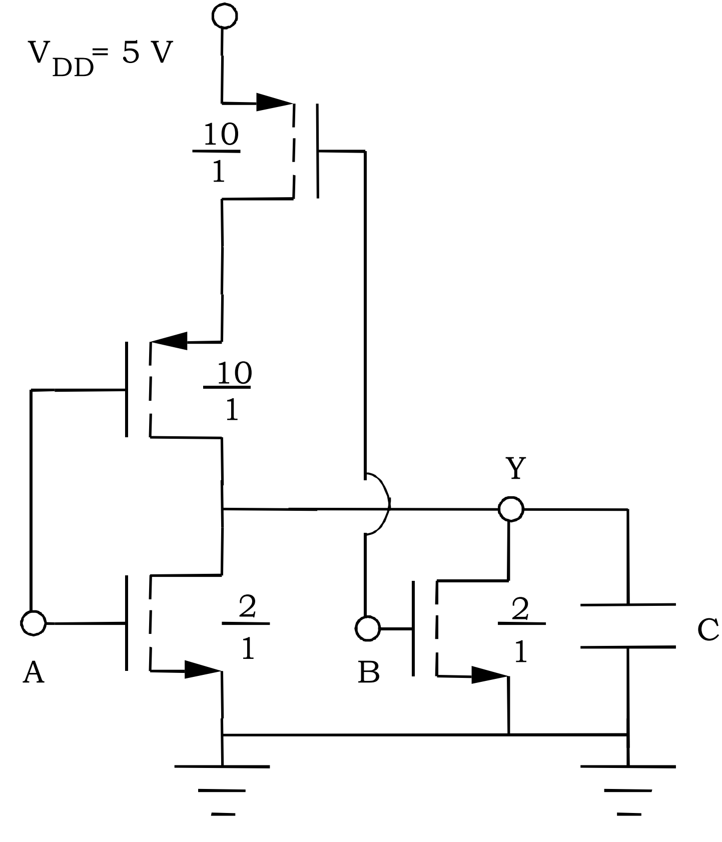
$$\boxed{P = a f\;C\;V_{DD}^{\,2}}$$

a **is the switching activity factor**

CMOS Gates (Static Logic)

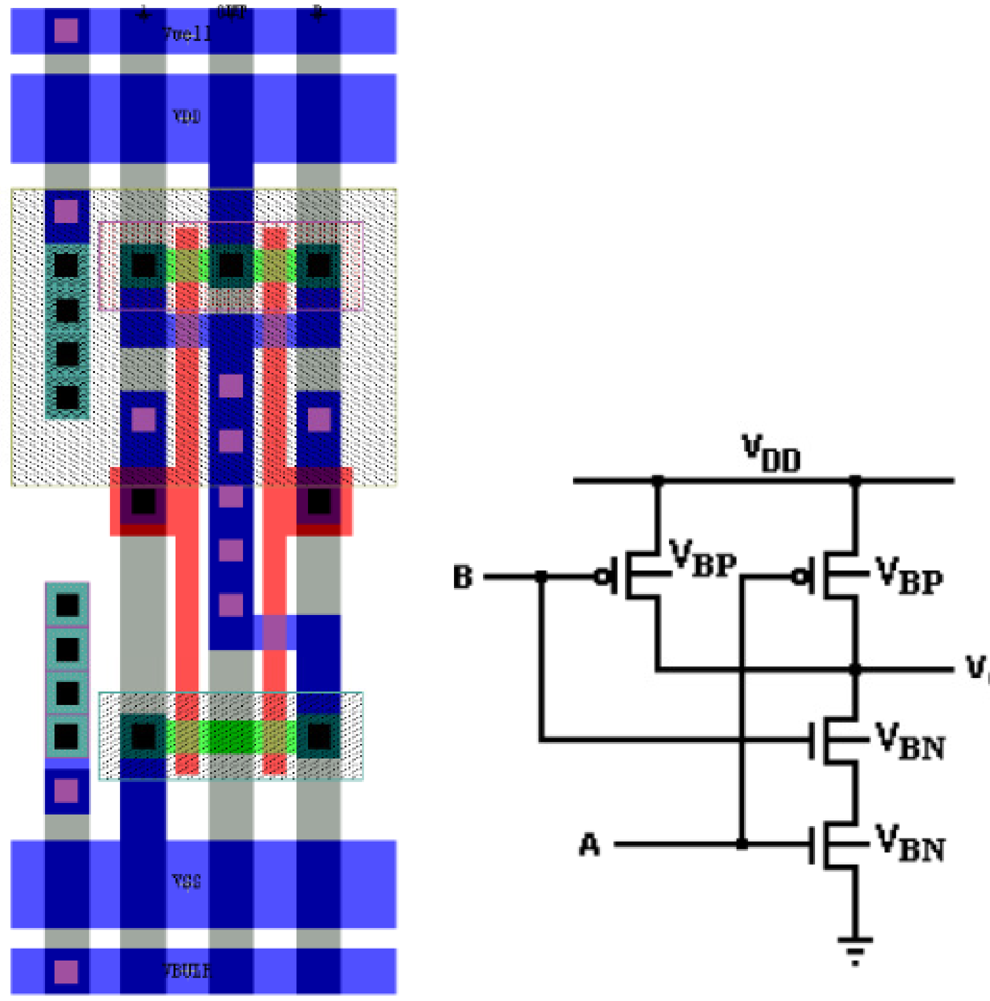


Basic CMOS logic gate structure

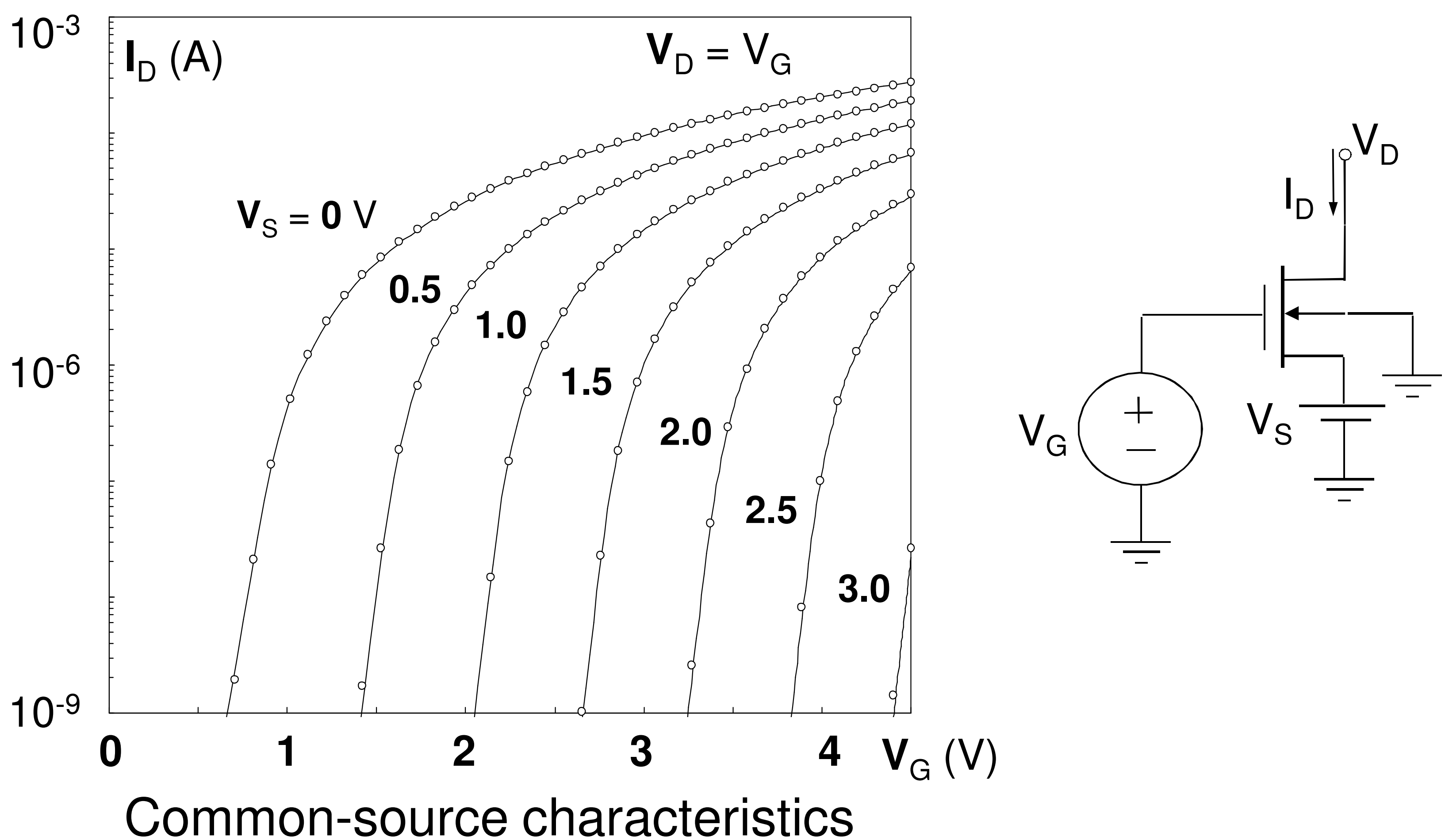


Two-input CMOS NOR gate

NAND de 2 entradas



The complete I-V relationship of the MOSFET (strong and weak inversion)

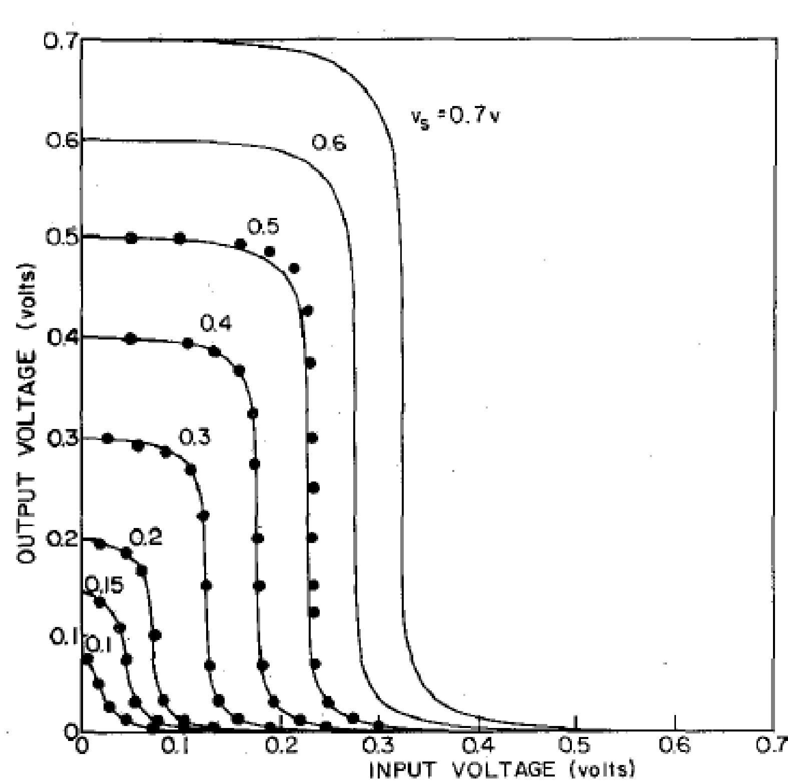


Common-source characteristics

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-7, NO. 2, APRIL 1972

Ion-Implanted Complementary MOS Transistors in Low-Voltage Circuits

RICHARD M. SWANSON, MEMBER, IEEE, AND JAMES D. MEINDL, FELLOW, IEEE



CMOS inverter transfer characteristics. ——experiment; ···· theory (12a).

Prof. James Meindl:
Theoretically, the minimum supply voltage for a CMOS inverter is
2 (ln2) (kT/q) = 36 mV
at room temperature (IEEE JSSC, 2000)

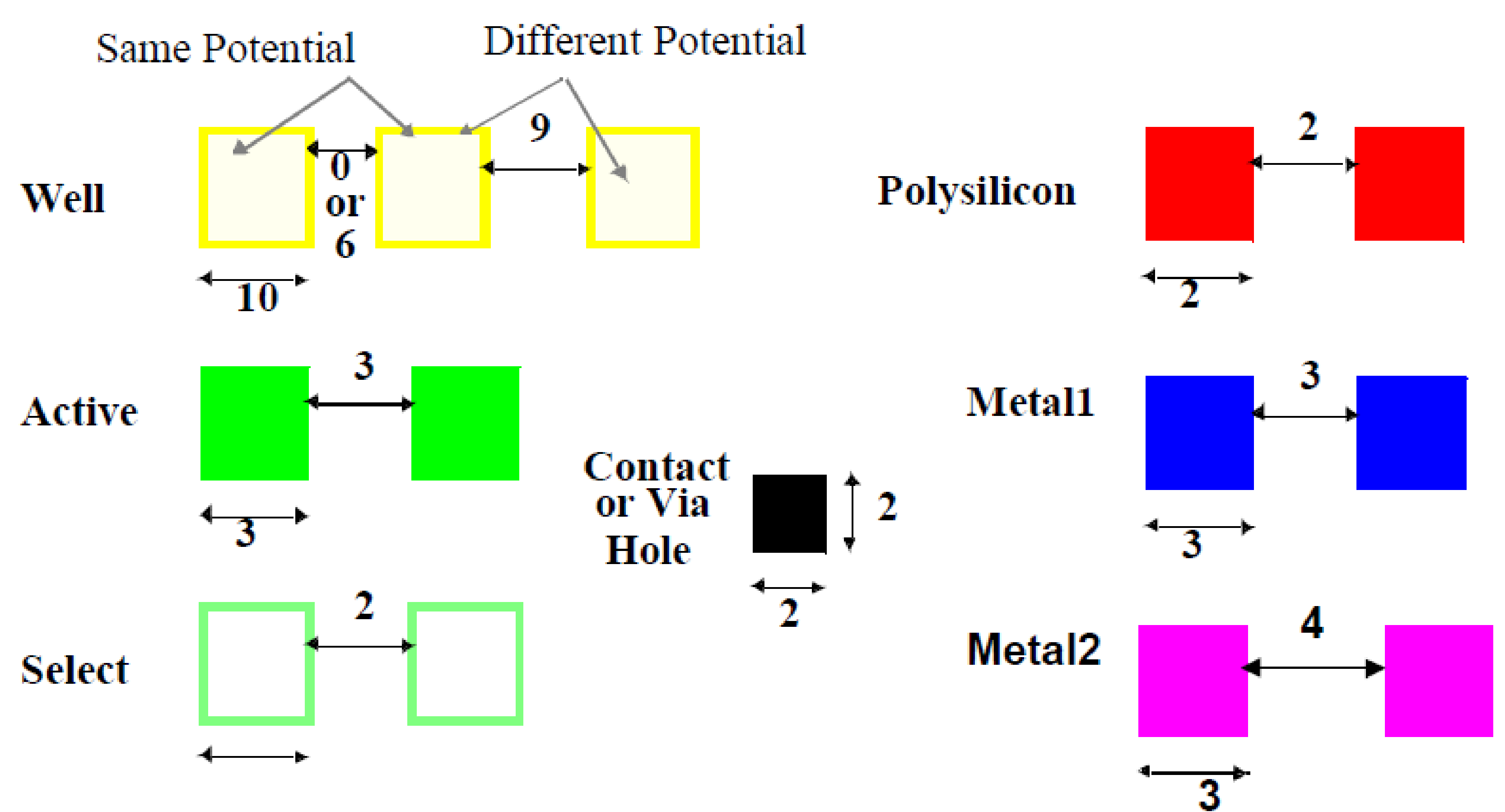
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - » scalable design rules: lambda parameter
  - » absolute dimensions (micron rules)

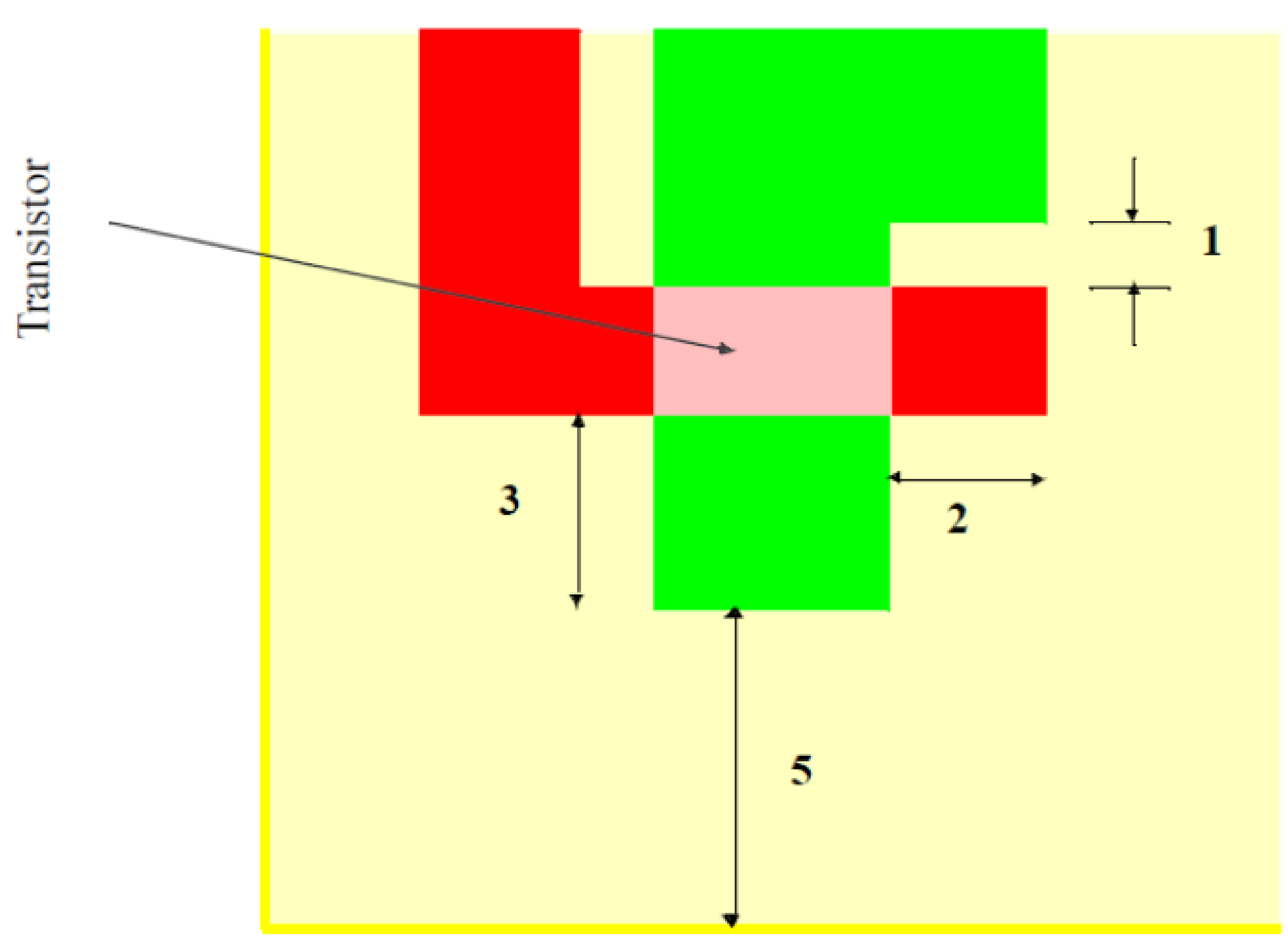
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

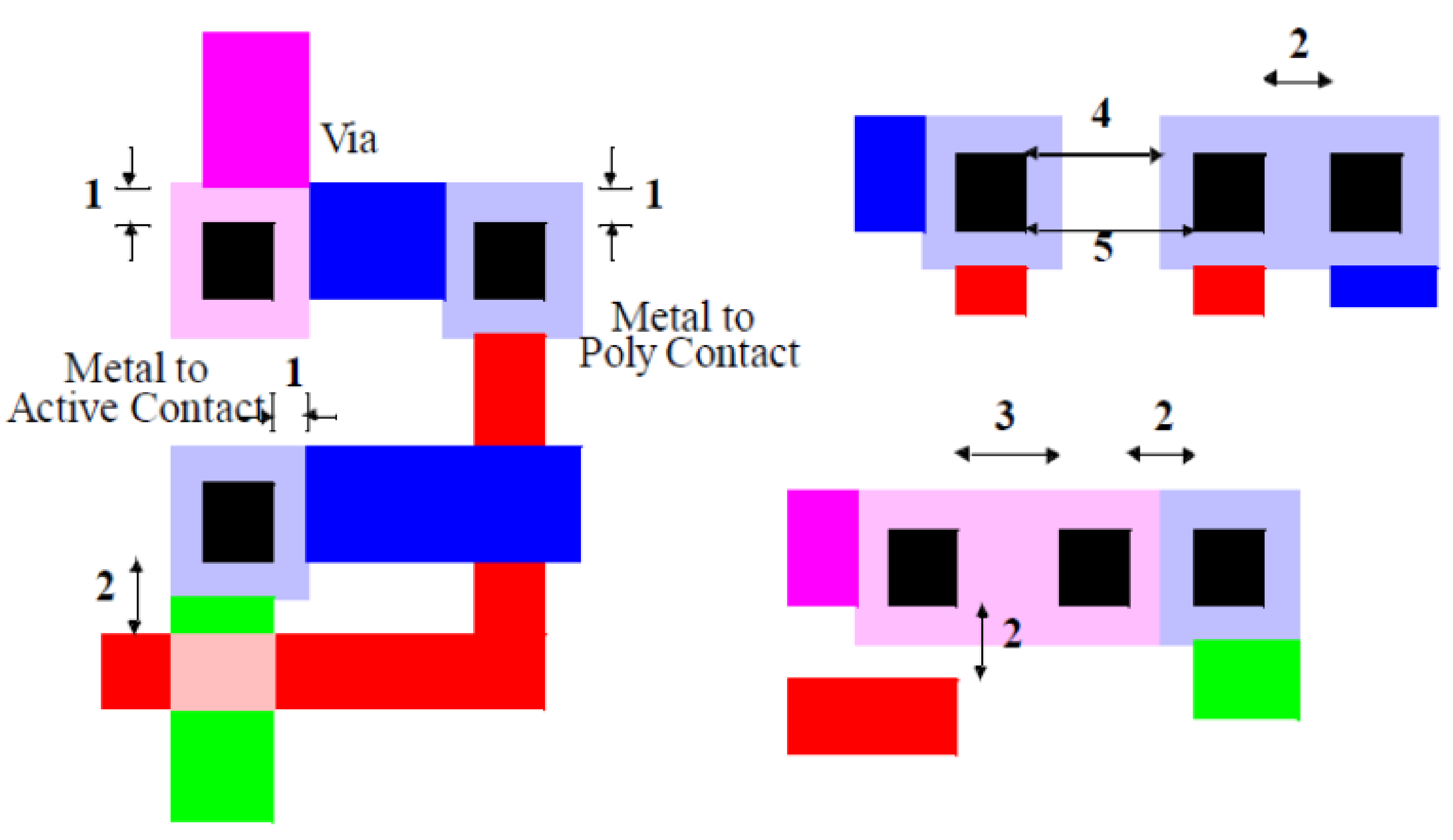
Intra-Layer Design Rules



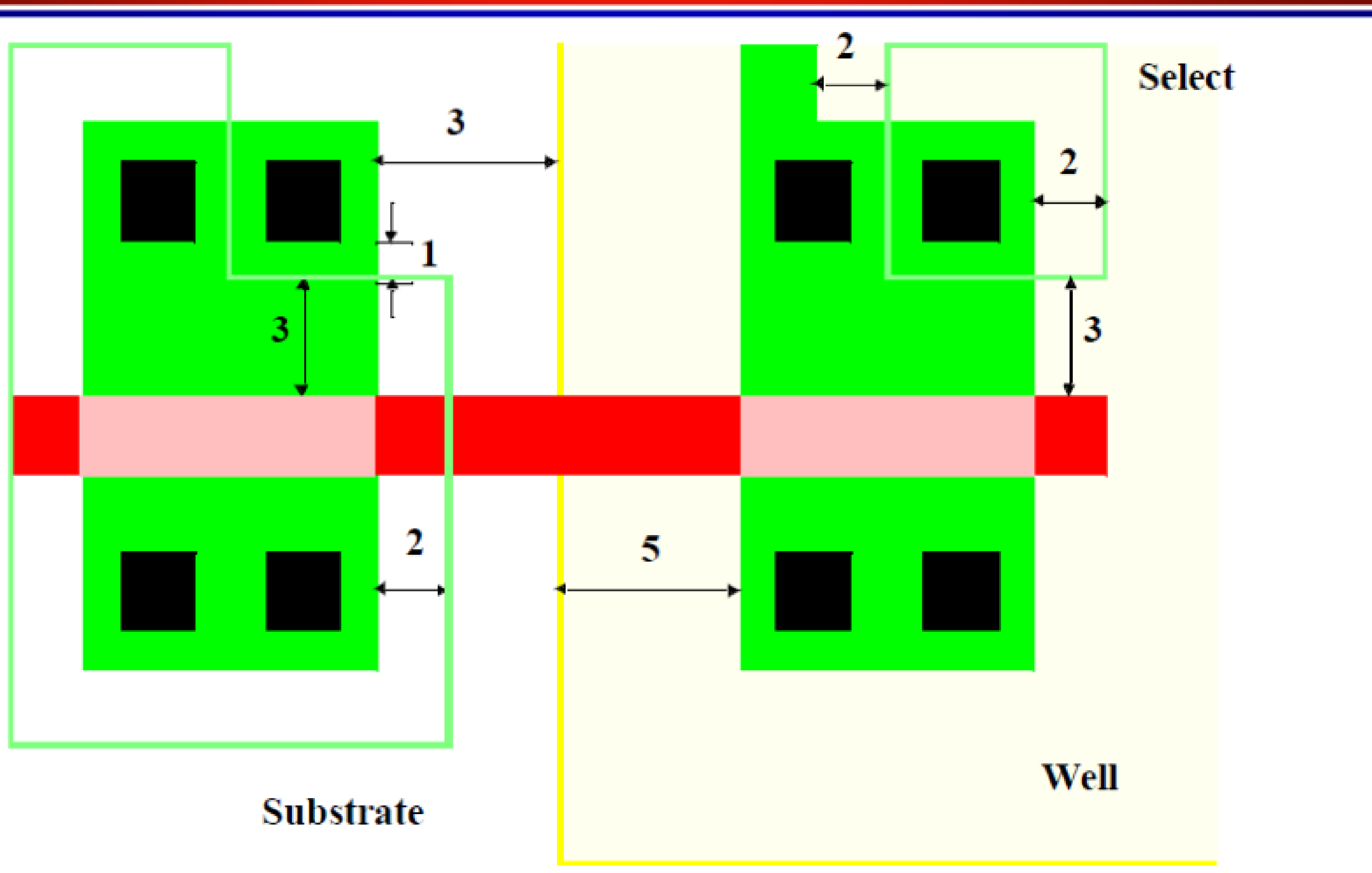
Transistor Layout



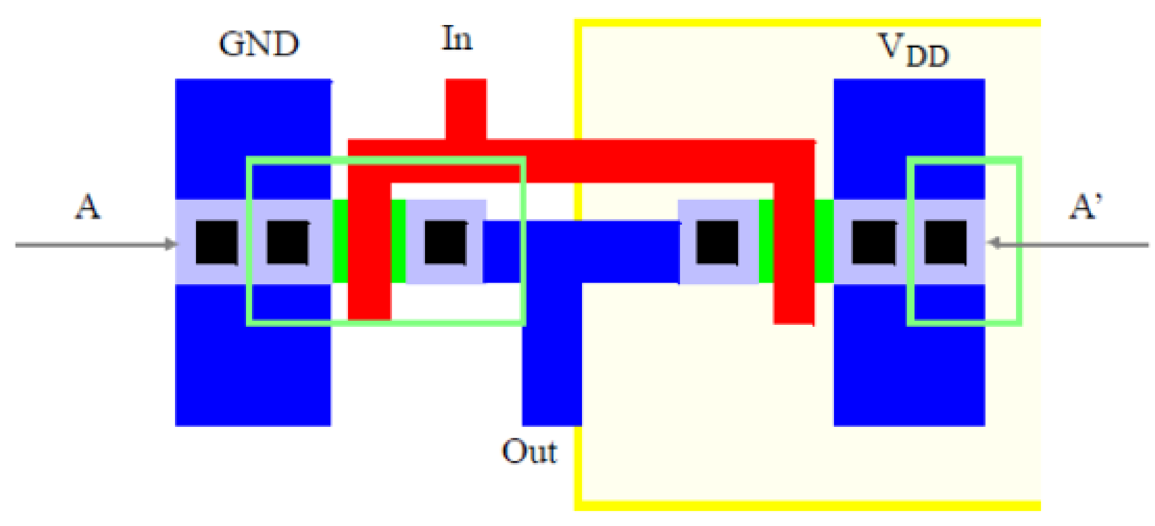
Via's and Contacts



Select Layer



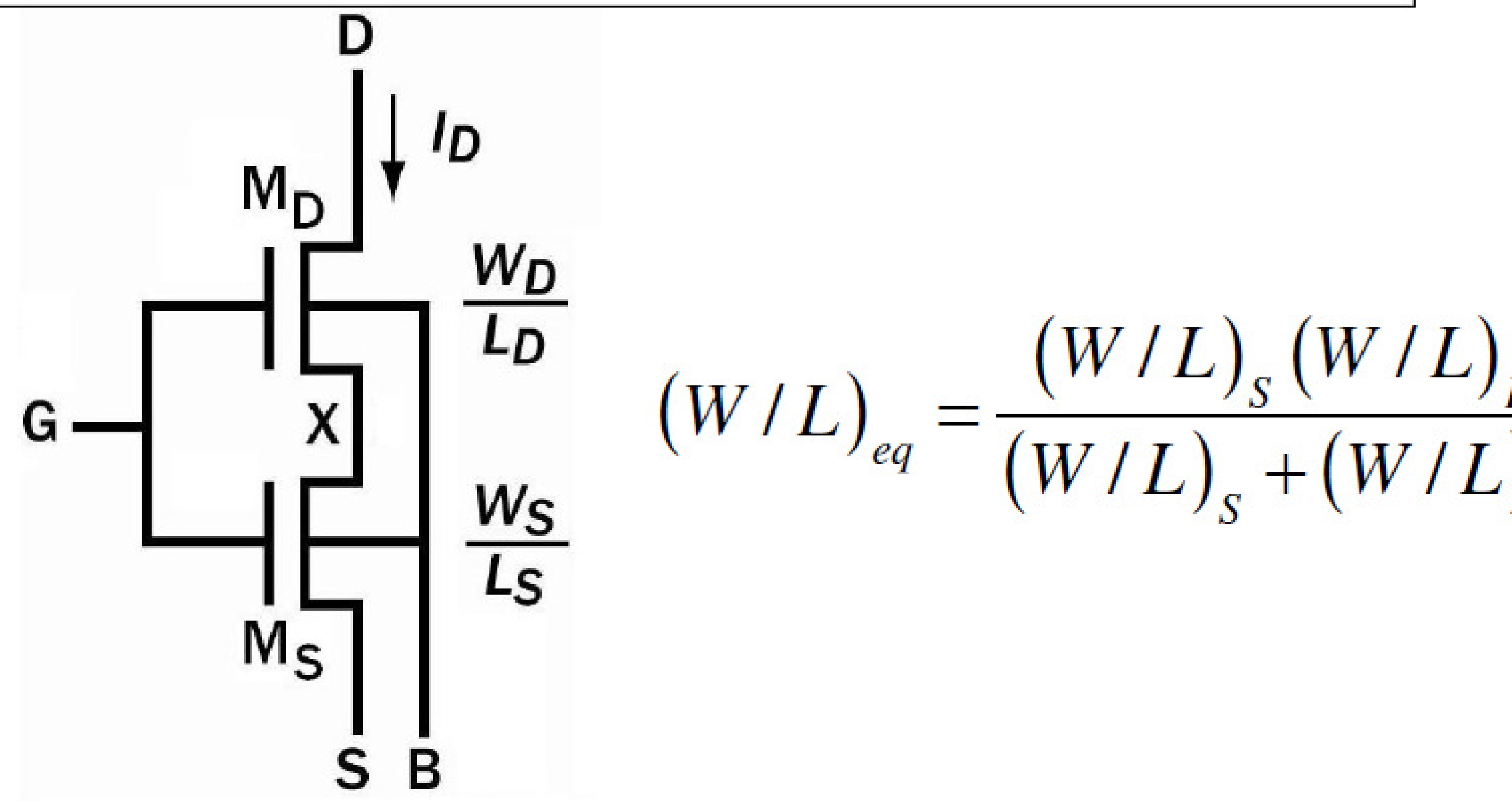
CMOS Inverter Layout



(a) Layout

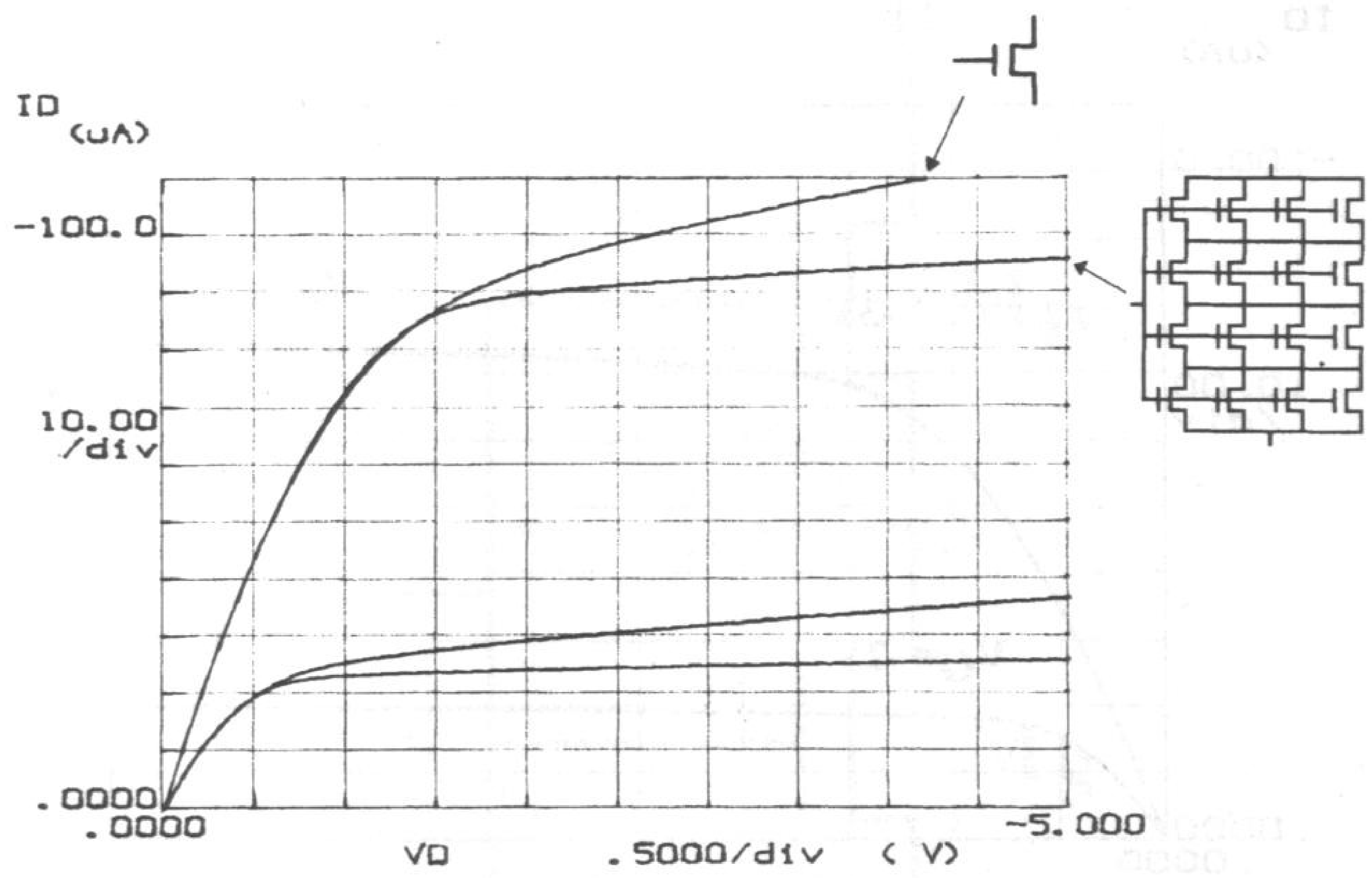
(b) Cross-Section along A-A'

Modeling the series association of MOSFETs

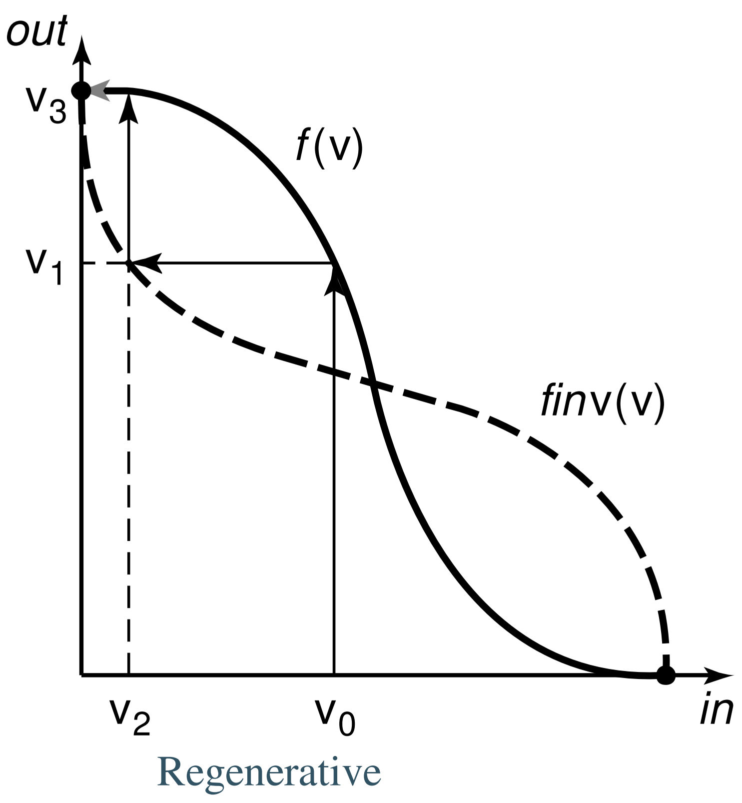


$$(W/L)_{eq} = \frac{(W/L)_S (W/L)_D}{(W/L)_S + (W/L)_D}$$

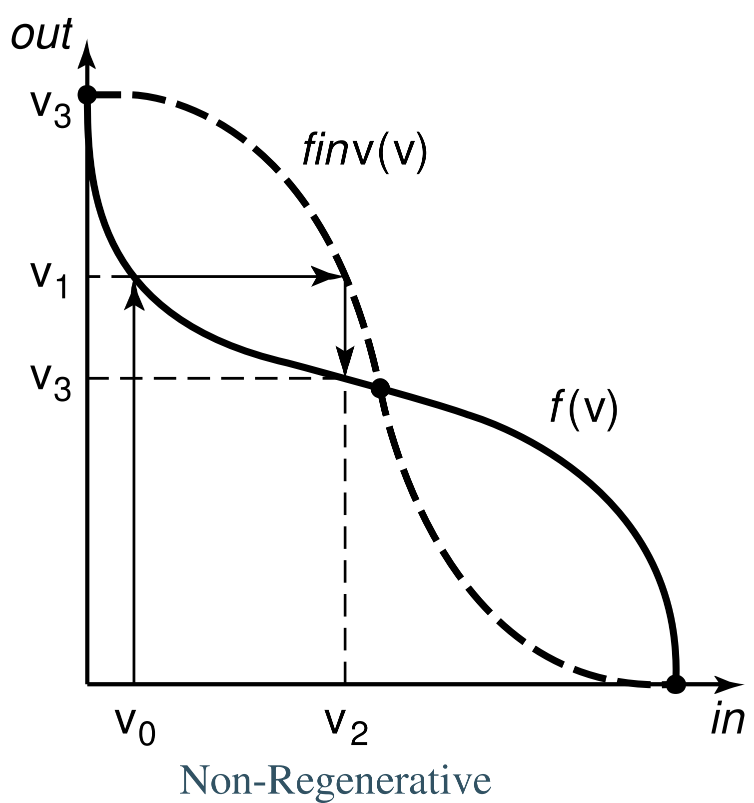
Series-parallel association of MOSFETs



Regenerative Property

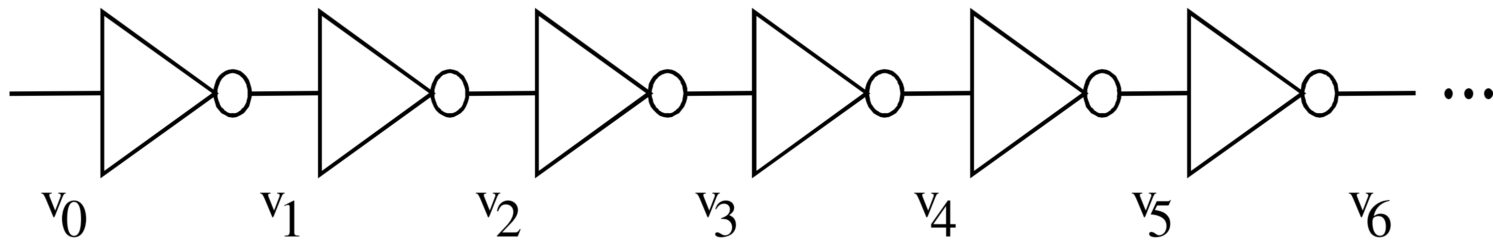


Regenerative

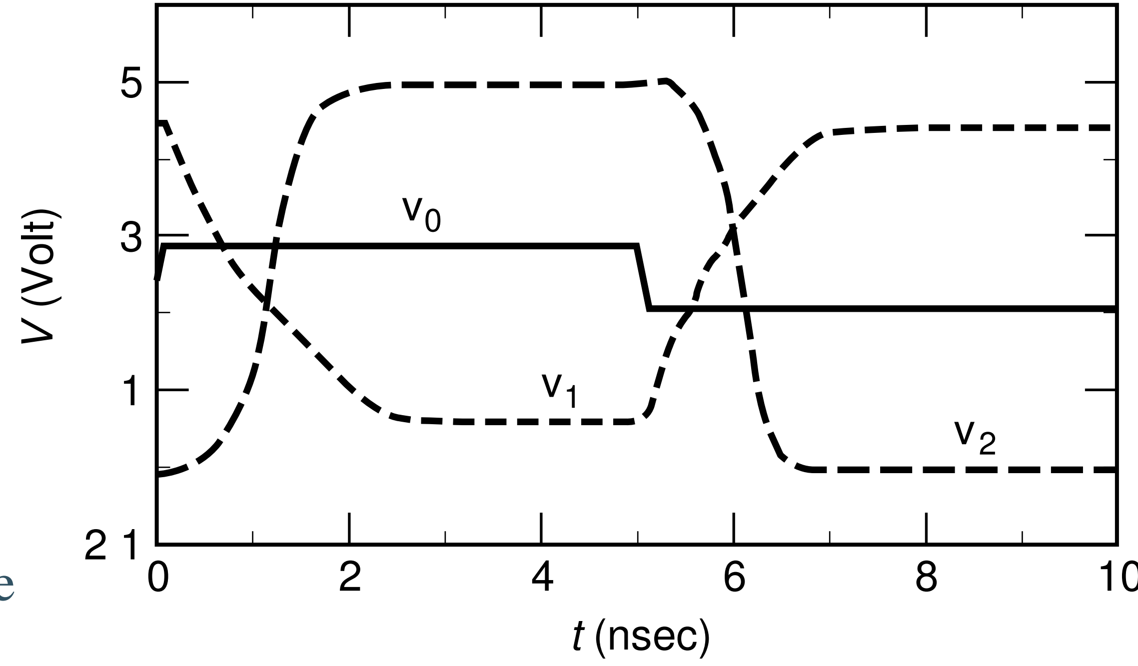


Non-Regenerative

Regenerative Property

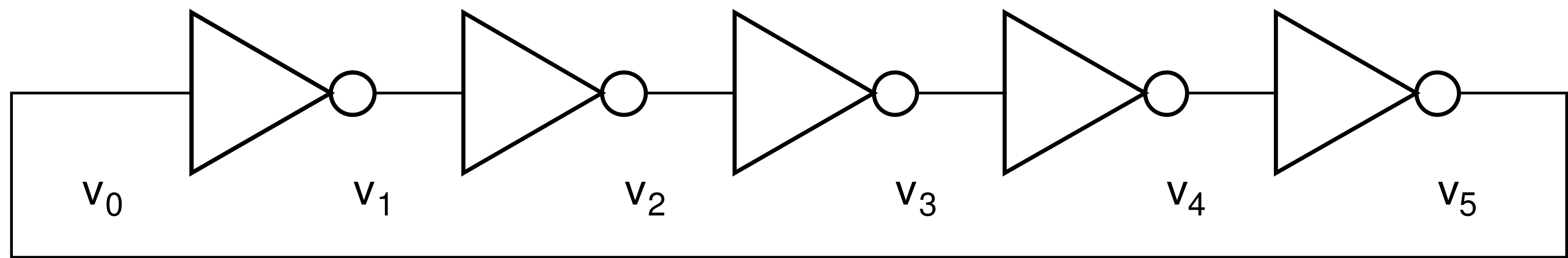


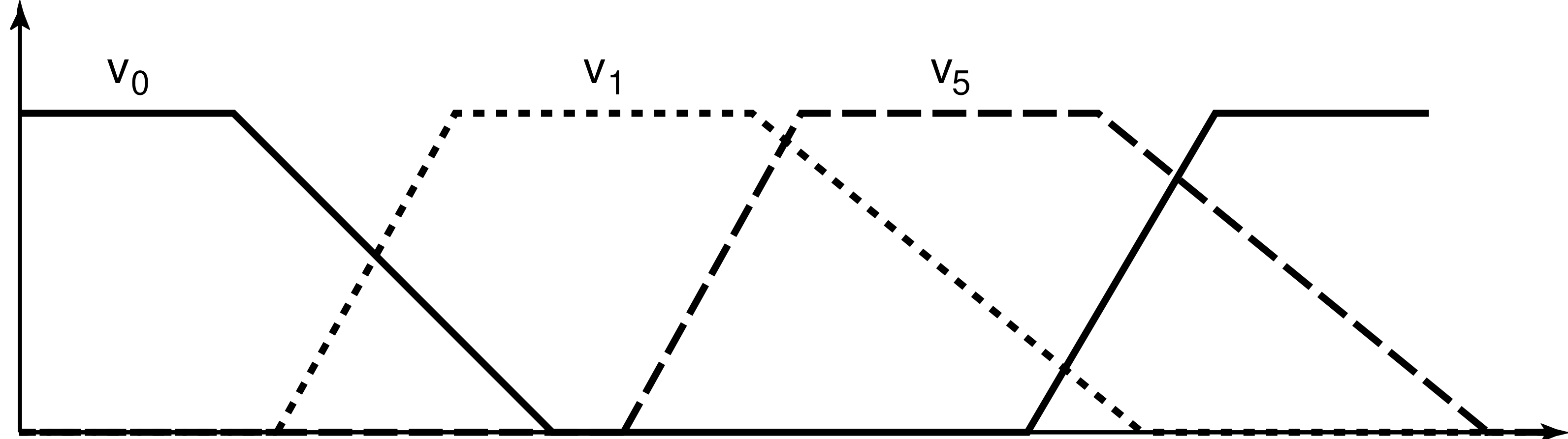
A chain of inverters



Simulated response

Ring Oscillator





$$T = 2\, t_p\, N$$

REFERENCES

- R. F. Pierret, *Field Effect devices*, 2nd ed., Addison-Wesley, 1990.
- Y. Tsividis, *Mixed Analog-Digital VLSI Devices and Tecnology*, World Scientific,1996.
- C. Galup-Montoro and M. C. Schneider, *MOSFET Modeling for Circuit Analysis and Design*, World Scientific, 2007.
- M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*, Cambridge, 2010.
- R. Howe, and C. Sodini. *Microelectronics: An Integrated Approach*. Prentice Hall, 1996.
- J. Rabaey, A. P. Chandrakasan, B. Nikolić, *Digital Integrated Circuits: A Design Perspective,* Pearson Education, 2003.
- L. A. Pasini Melek, *Operação de Circuitos Lógicos CMOS de (ultra)-baixo consumo*, Dissertação de mestrado, UFSC, 2004.

Example: oxide capacitance

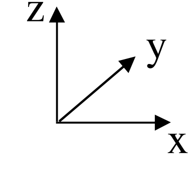
(a) Calculate the oxide capacitance per unit area for t_{ox}= 5 and 20 nm. The permittivity of silicon oxide is $\varepsilon_{ox} = 3.9\varepsilon_0$. $\varepsilon_0 = 8.85 \cdot 10^{-14}$ F/cm is the permittivity of free space.

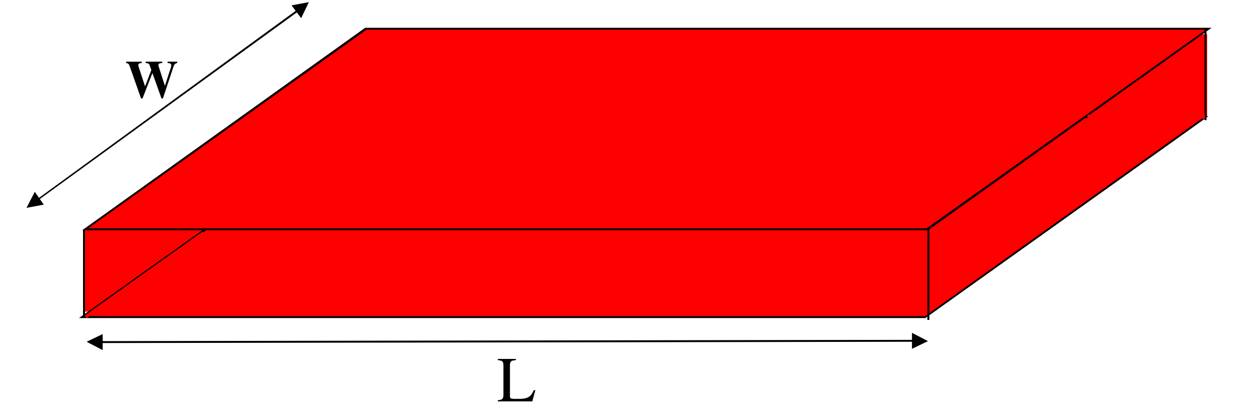
(b) Determine the area of a 1pF metal-oxide-metal capacitor for the two oxide thicknesses given in (a).

(c) Determine the gate charge/unit area in C/cm^2 and the number of elementary charges/ μm^2 of the 1 pF capacitor for $V_G - \phi_S = 1$ V

Answer: (a) C_{ox} = 690 nF/cm^2 = 6.9 fF/μm^2 for t_{ox}=5 nm and C_{ox} = 172 nF/cm^2= 1.7 fF/μm^2 for t_{ox}= 20 nm. (b)The capacitor areas are 145 and 580 μm^2 for oxide thicknesses of 5 and 20 nm, respectively. (c) $0.69 \cdot 10^{-6}$ and $0.43 \cdot 10^{5}$ /μm^2 for capacitor area of 145 μm^2 and $0.17 \cdot 10^{-6}$ and $0.11 \cdot 10^{5}$ /μm^2 for capacitor area of 580 μm^2.

Example: charge density





Assume that the electron concentration is $n = 10^{16}$ cm^{-3} , L=W=1 um, t=0.1 um

(a) Calculate the volumetric charge density

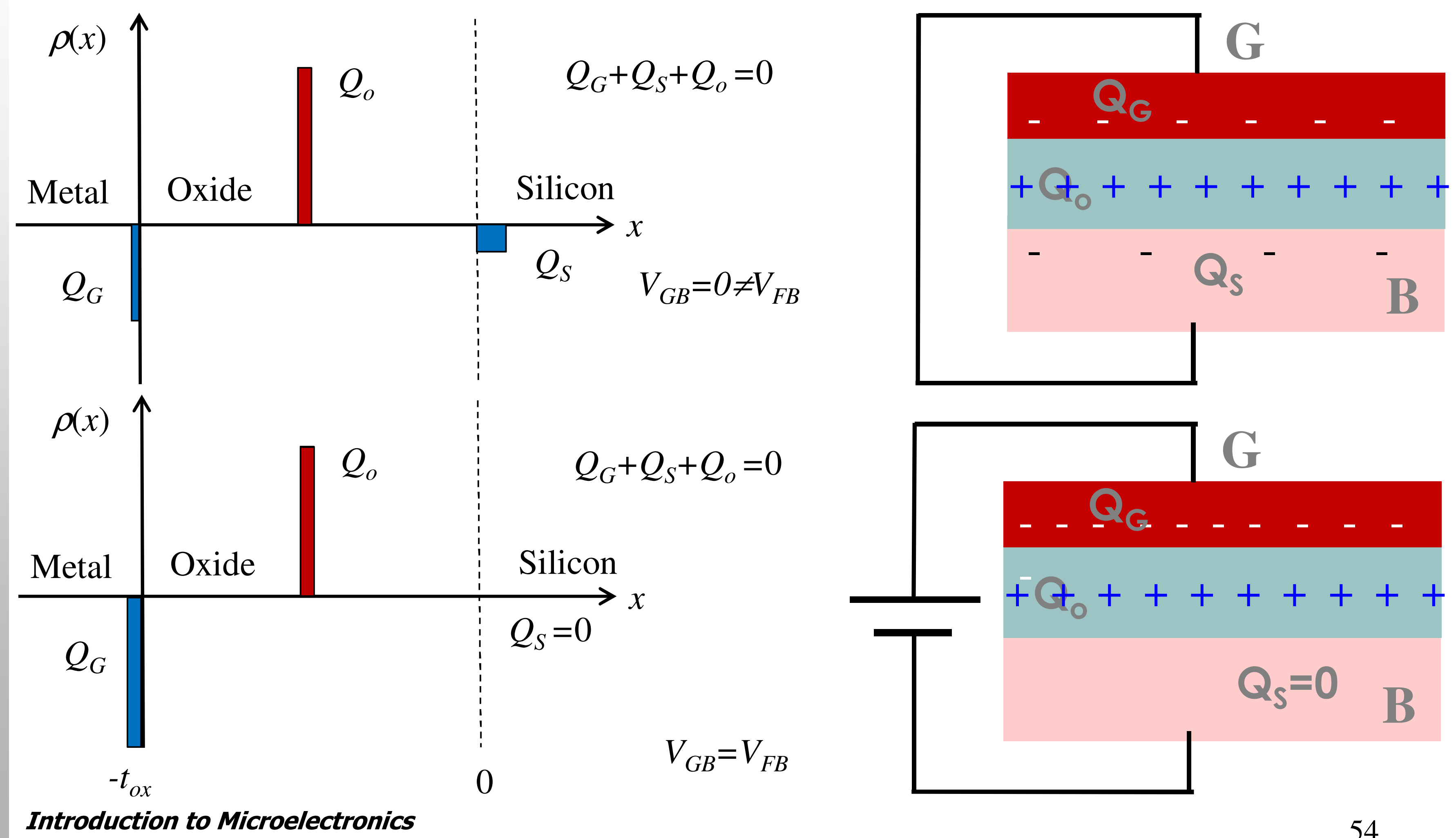
(b) Calculate the total number of electrons and the corresponding charge inside the volume

(c) Calculate the (areal) charge density seen from the z-direction

Answer: (a) ρ= -1.6 10^{-3} C/cm^3 (b) Number of electrons = 10^3, charge = -1.6 x 10^{-16} C (c) charge density Q_n= -1.6 x 10^{-8} C/cm^2 .

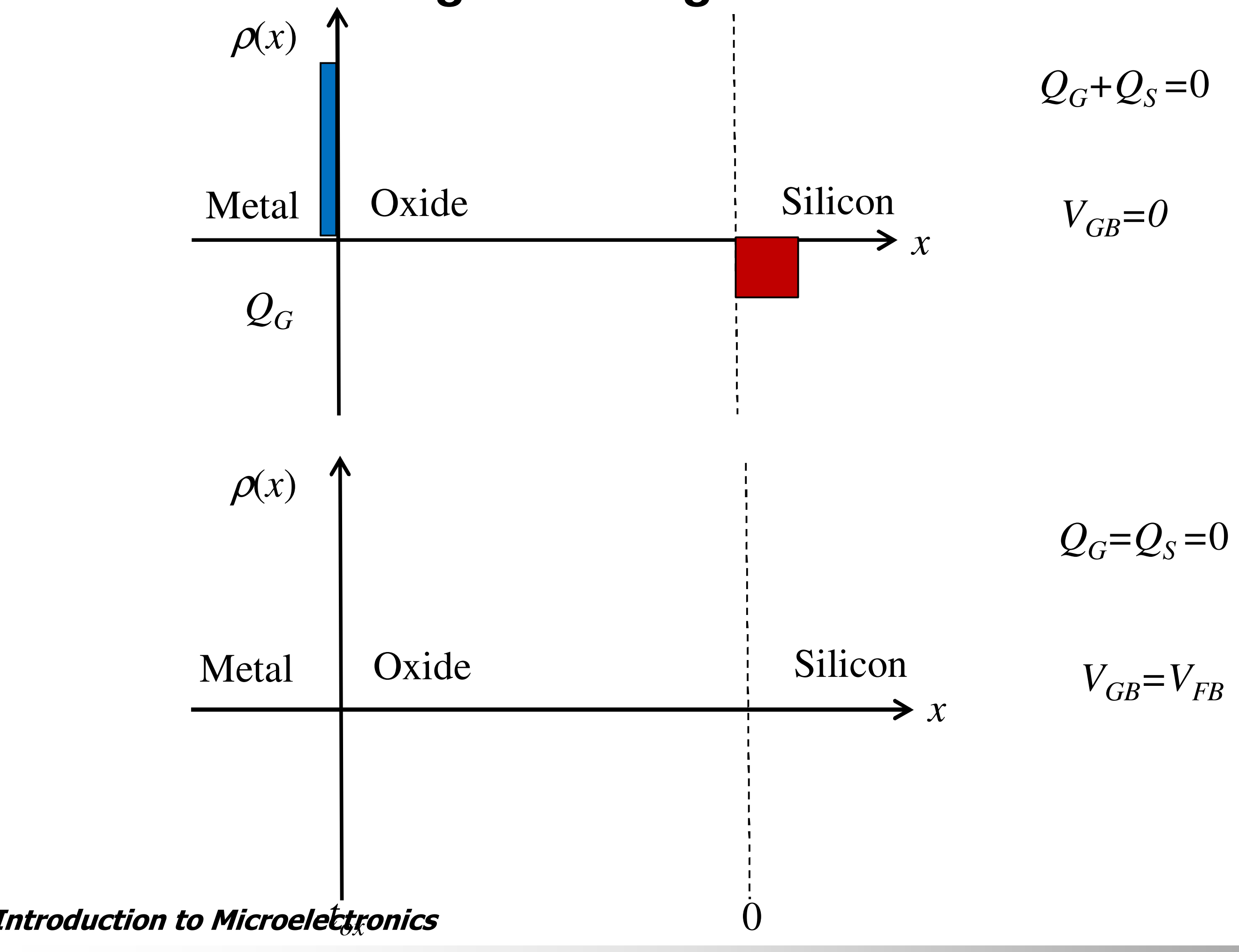
The flat-band voltage (V_{FB})

1. Charges inside the insulator and at the semiconductor-insulator interface induce a semiconductor charge at zero bias.



The flat-band voltage (V_{FB})

2. In equilibrium (with the two terminals shortened), the contact potential between the gate and the semiconductor substrate of the MOS induces charges in the gate and the semiconductor for V_{GB}=0.



$Q_G + Q_S = 0$

$V_{GB} = 0$

$Q_G = Q_S = 0$

$V_{GB} = V_{FB}$

Example: flat-band voltage

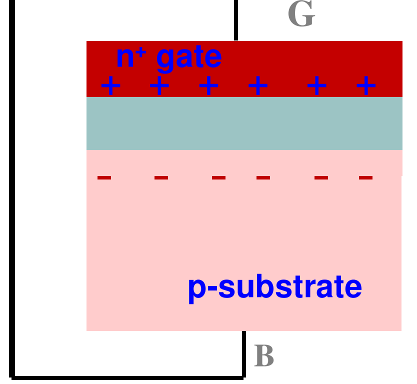
(a) Determine the expression for the flat-band voltage of n$^+$ polysilicon-gate on p-type silicon (b) Calculate the flat-band voltage for an n$^+$ polysilicon-gate on p-type silicon structure with $N_A = 10^{17}$ atoms/cm^3.

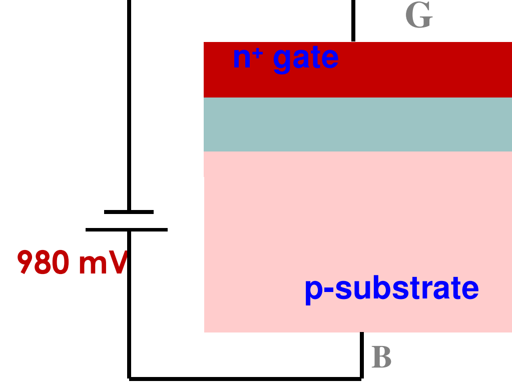
Answer: (a) In equilibrium, by analogy with an n$^+$ p junction, the potential of the n$^+$-region is positive with respect to that of the p-region. The flat-band condition is obtained by applying a negative potential to the n$^+$ gate with respect to the p-type semiconductor of value

(b)

$$V_{FB_n+p} = -\phi_{bi_n+p} = -0.56\text{ V} - \phi_t \ln\left(\frac{N_A}{n_i}\right)$$

$$V_{FB} = -0.56\text{ V} - \phi_t \ln\left(10^7\right) = -980\text{ mV}$$





Example: threshold voltage

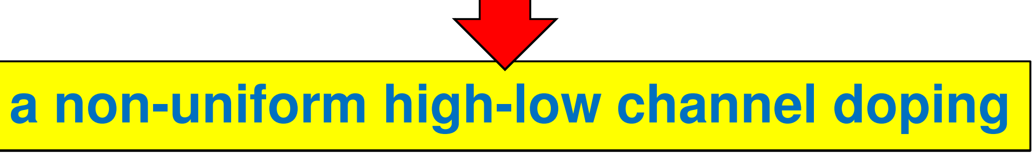
Estimate V_T for an n-channel transistor with n$^+$ polysilicon gate, N_A=10^{17} atoms/cm^3 and t_{ox}=5 nm.

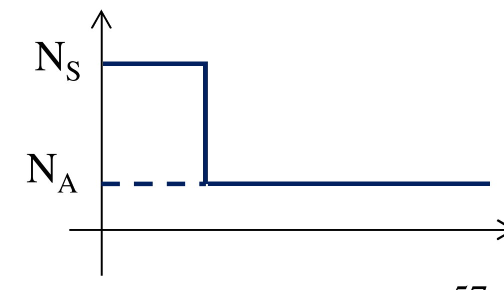
Answer: The flat-band voltage (slide 12) is -0.98 V; ϕ_F=0.419; C_{ox}= 690 nF/cm^2. The body-effect factor is $\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox} = 0.264\ \sqrt{\mathrm{V}}$

$$V_T \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} = -0.98 + 0.838 + 0.264\sqrt{0.838} = 0.1\mathrm{V}$$

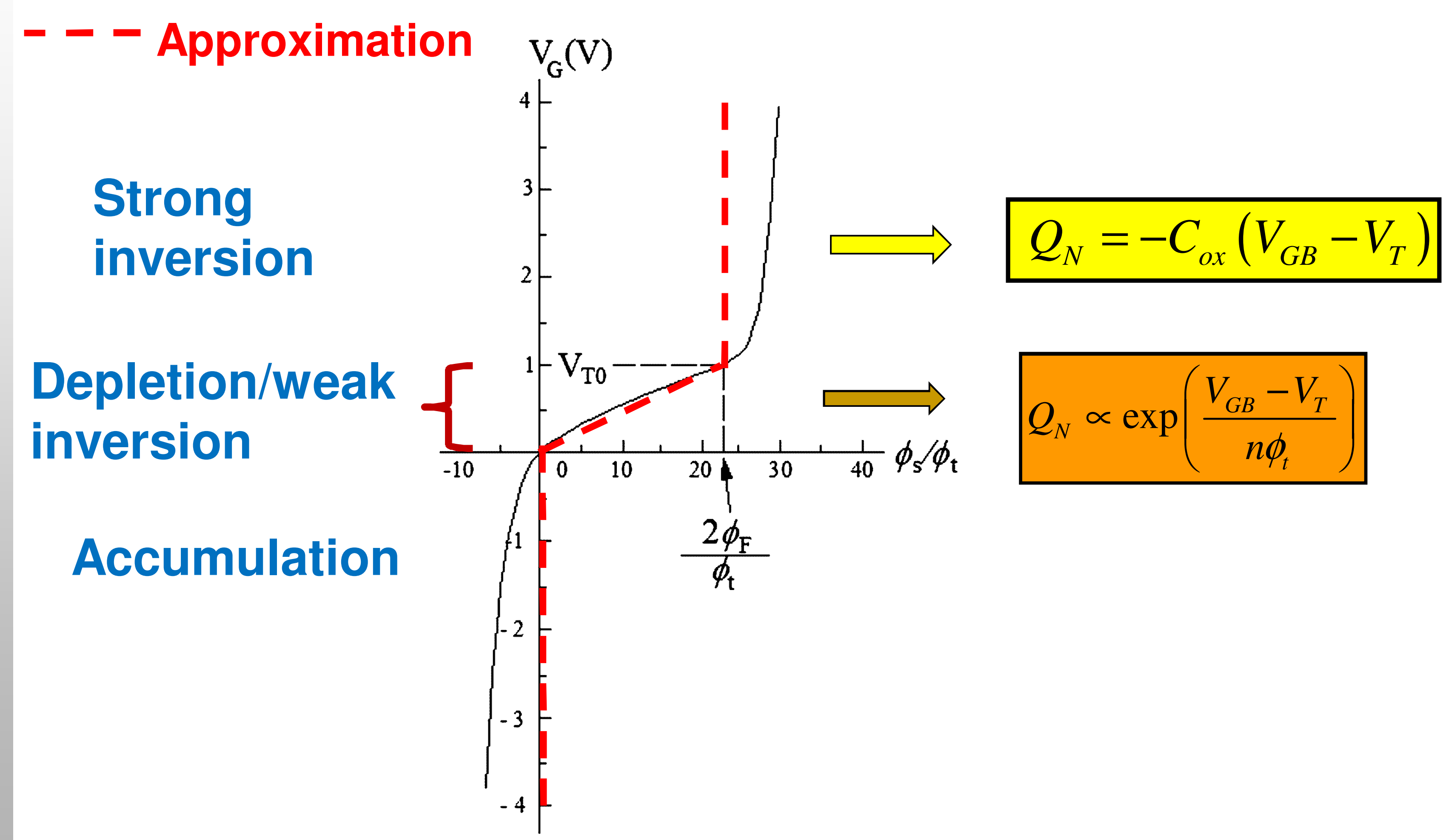
For this low value of the threshold voltage, the off-current (for V_{GS}=0) is too high for digital circuits (see subthreshold leakage).

Solution to control the magnitude of the threshold voltage





Exact relationship between surface potential and applied gate voltage V_G for the MOS capacitor



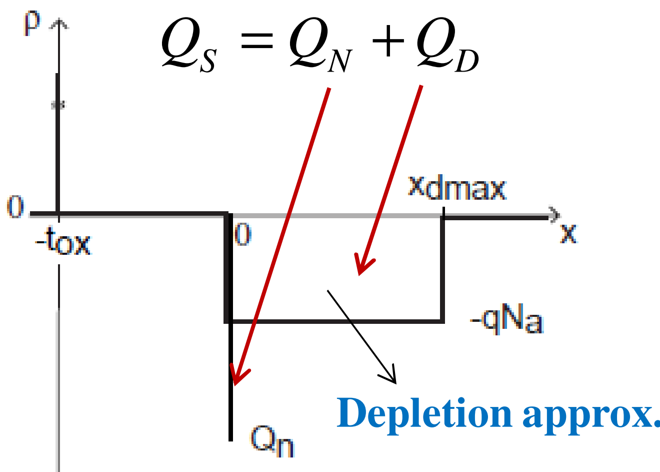
Threshold voltage V_T (for strong inversion)

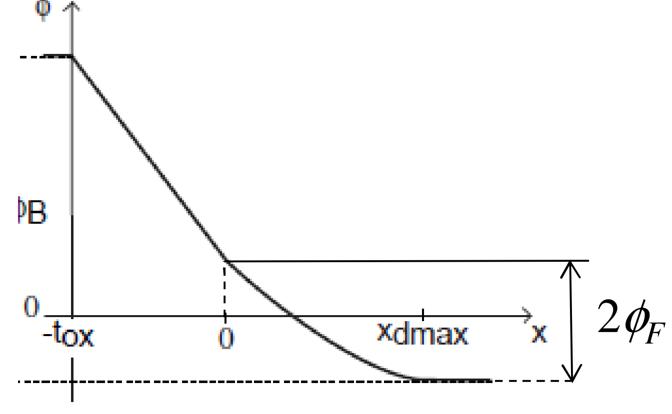
Gate voltage for which $\phi_s = 2\phi_F$

$Q_N \longrightarrow$ **Electron (carrier) charge**

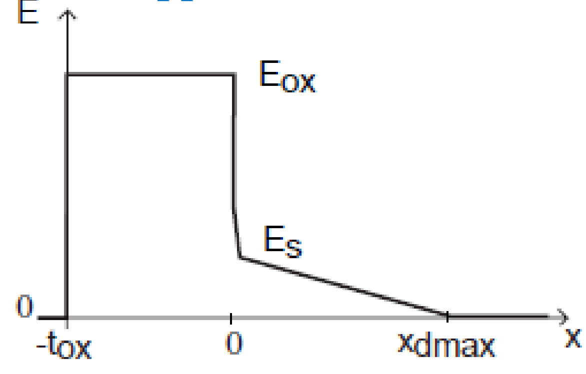
$Q_D \longrightarrow$ **Depletion (ion) charge**

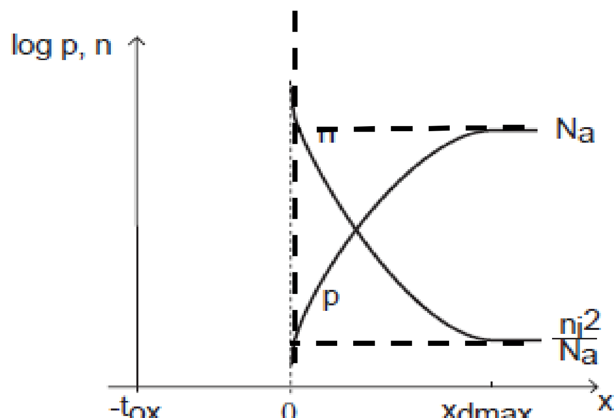
$$Q_S = Q_N + Q_D$$





Charge sheet approx.





Threshold voltage (for strong inversion)

$$\phi_s = 2\phi_F$$

At threshold we can neglect the inversion charge Q_N compared with the depletion charge Q_D

$$Q_S = Q_N + Q_D \cong Q_D$$

Recalling that

$$V_{GB} - V_{FB} = \phi_s - \frac{Q_S}{C_{ox}} \cong \phi_s - \frac{Q_D}{C_{ox}}$$

and solving for Q_D **(depletion approx.)**

$$\rho \cong -qN_A \; ; \; \frac{dE}{dx} = \frac{\rho}{\varepsilon_s} \text{ with } E(x_d) = 0 \rightarrow E = \frac{qN_A}{\varepsilon_s}(x_d - x)$$

$$E = -\frac{d\phi}{dx} \text{ with } \phi(x_d) = 0 \rightarrow \phi(x) = \frac{qN_A}{2\varepsilon_s}(x_d - x)^2 \Rightarrow \phi(x=0) = \phi_s = 2\phi_F \rightarrow 2\phi_F = \frac{qN_A}{2\varepsilon_s} x_d^2$$

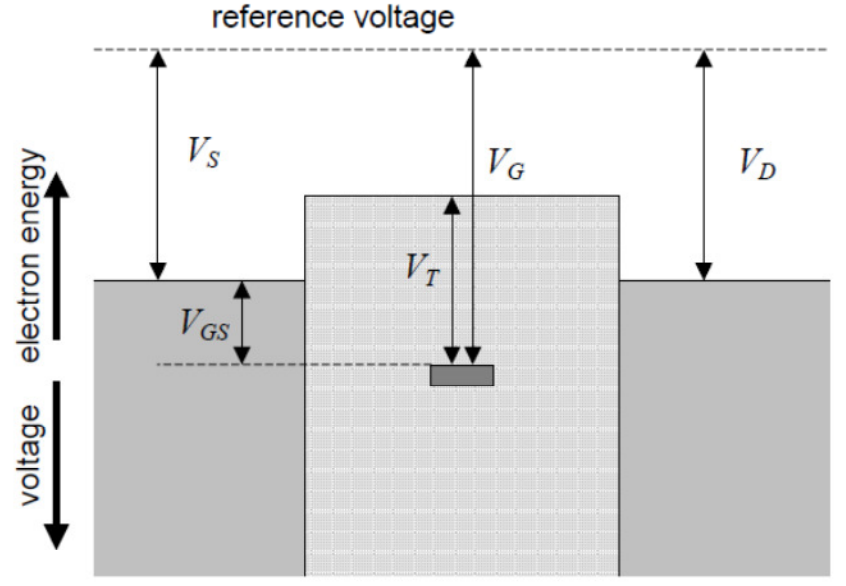
$$Q_D \cong -qN_A x_d = -\sqrt{2q\varepsilon_s N_A \phi_s} = -\gamma C_{ox}\sqrt{2\phi_F}$$

it follows that

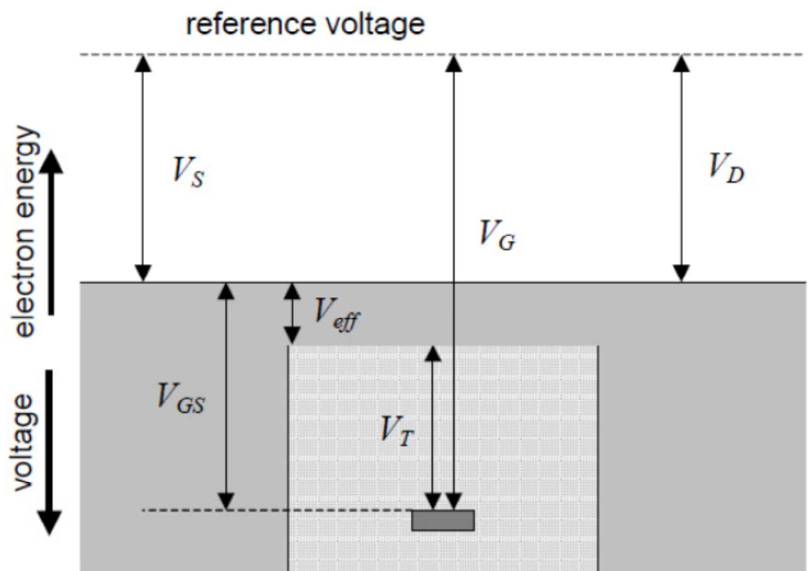
$$V_T = V_{GB}\Big|_{\phi_s = 2\phi_F} \cong V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F}$$

$$\gamma = \sqrt{2q\varepsilon_s N_A} / C_{ox} \longrightarrow$$ **Body effect factor**

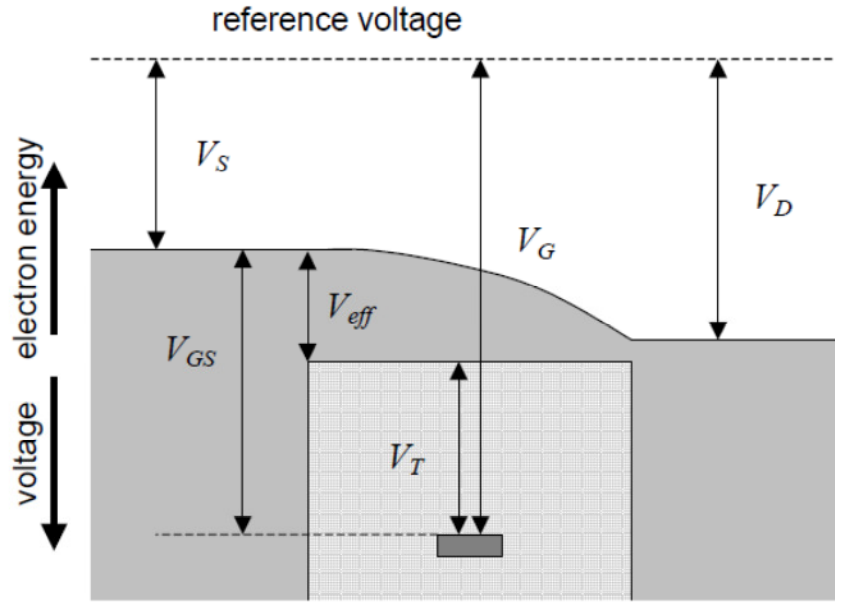
MOSFET in subthreshold ($V_{GS} < V_T$) and linear region (low V_{DS})



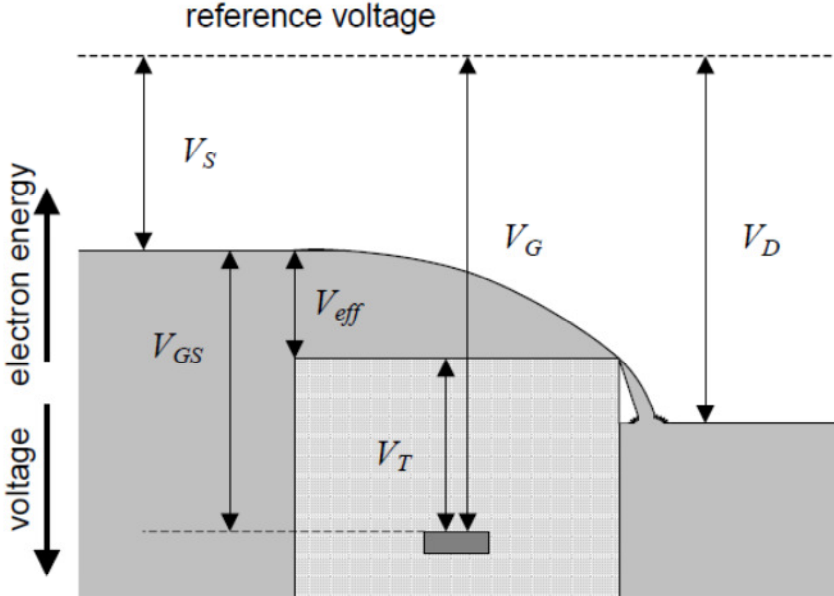
MOSFET in strong inversion ($V_{GS} > V_T$) and linear region (low V_{DS})



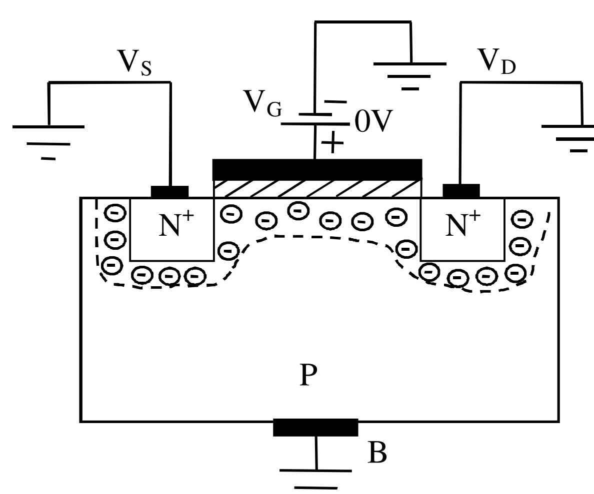
MOSFET for V_{GS}>V_T in the triode region



MOSFET for V_{GS}>V_T in the saturation region

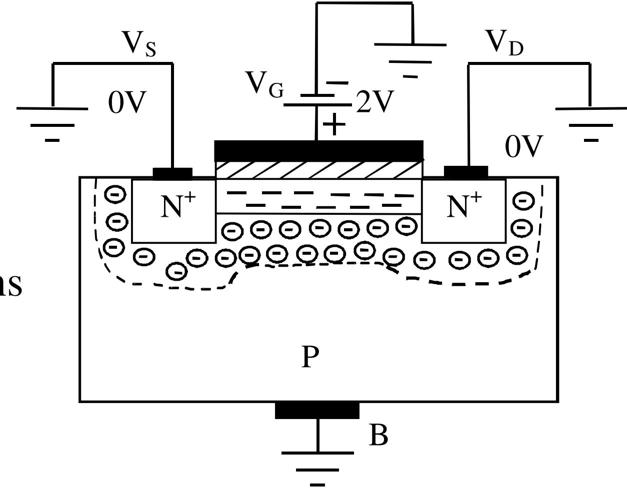


5.3 I-V Characteristics of Enhancement Mode MOSFETs

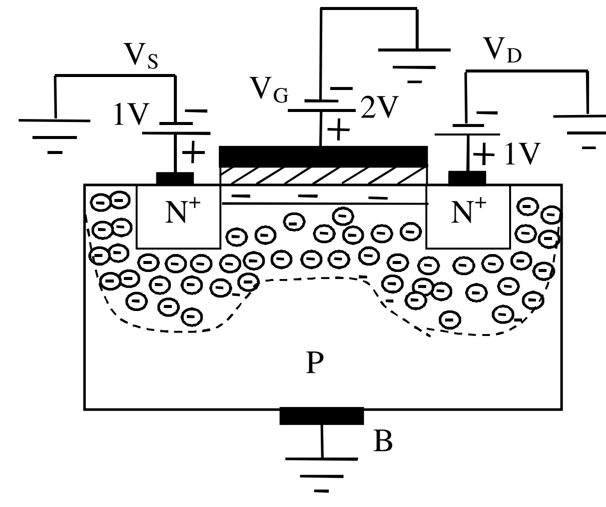


(a) $V_G = 0V$ $V_S = V_D = 0V$

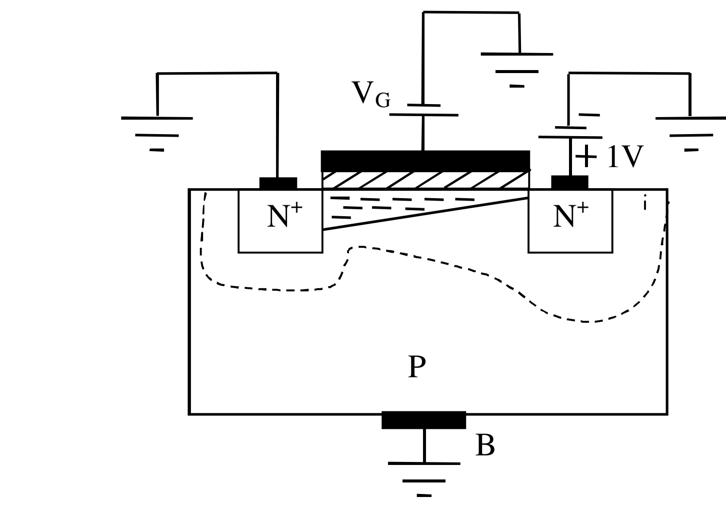
⊝ ions
– electrons



(b) $V_G = 2V$ $V_S = V_D = 0V$

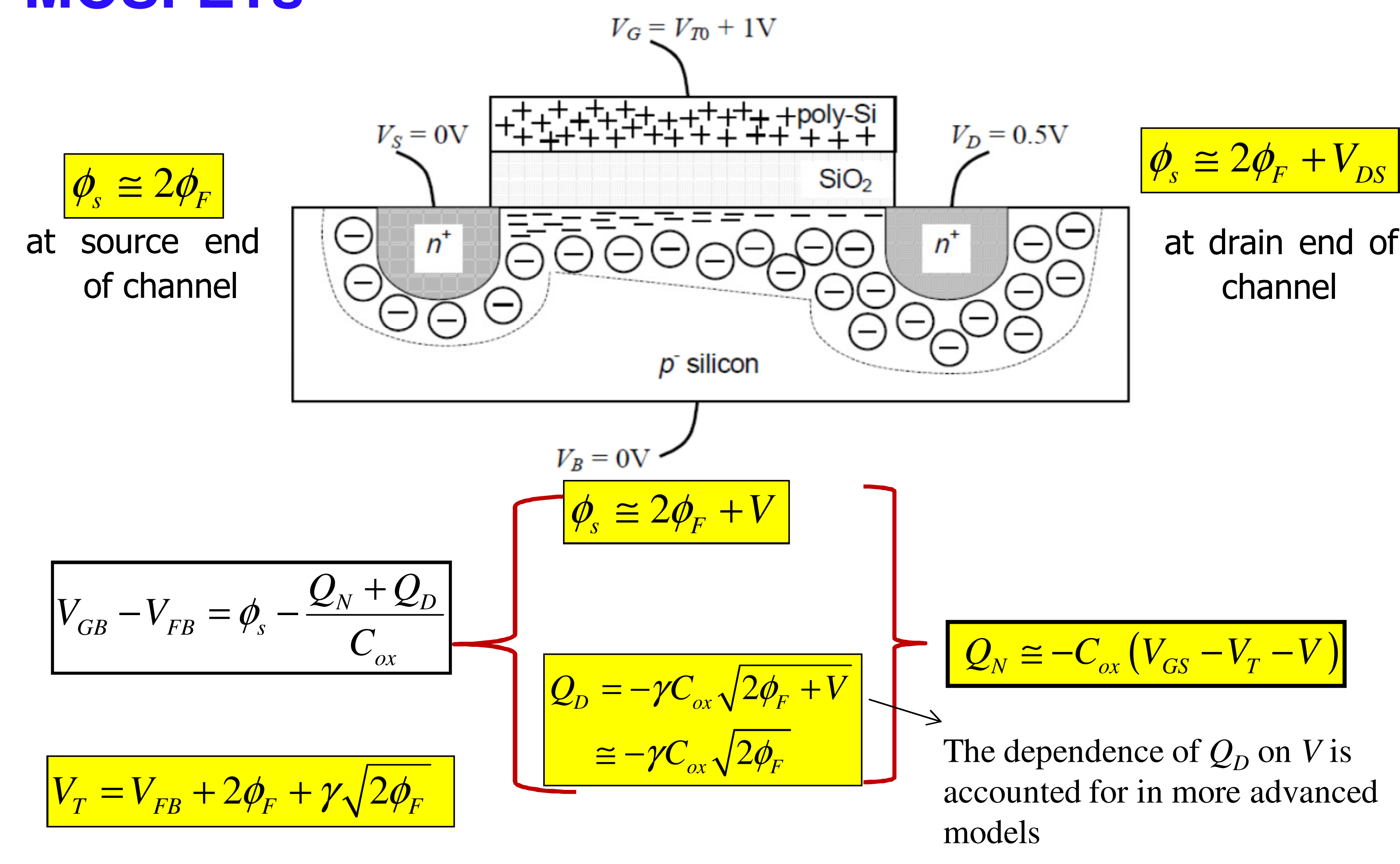


(c) $V_G = 2V$ $V_S = V_D = 1V$

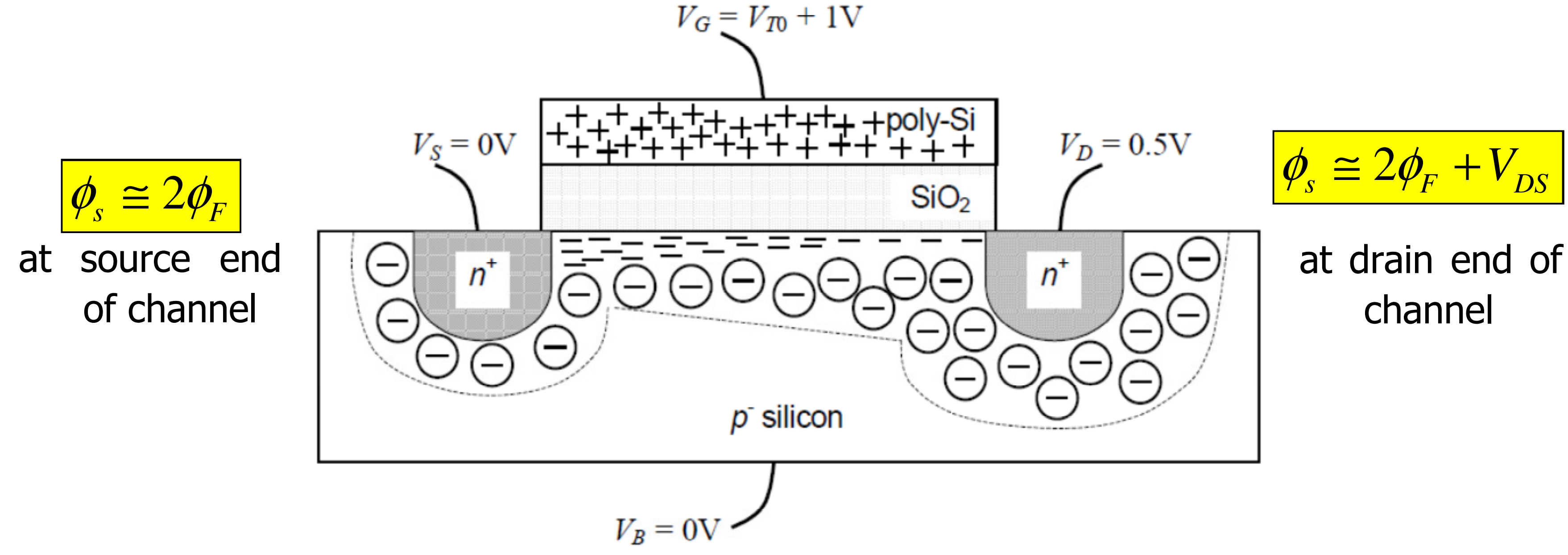


(d) $V_G = 2V$ $V_S = 0V$ $V_D = 1V$

5.3 I-V Characteristics of Enhancement Mode MOSFETs



5.3 I-V Characteristics of Enhancement Mode MOSFETs

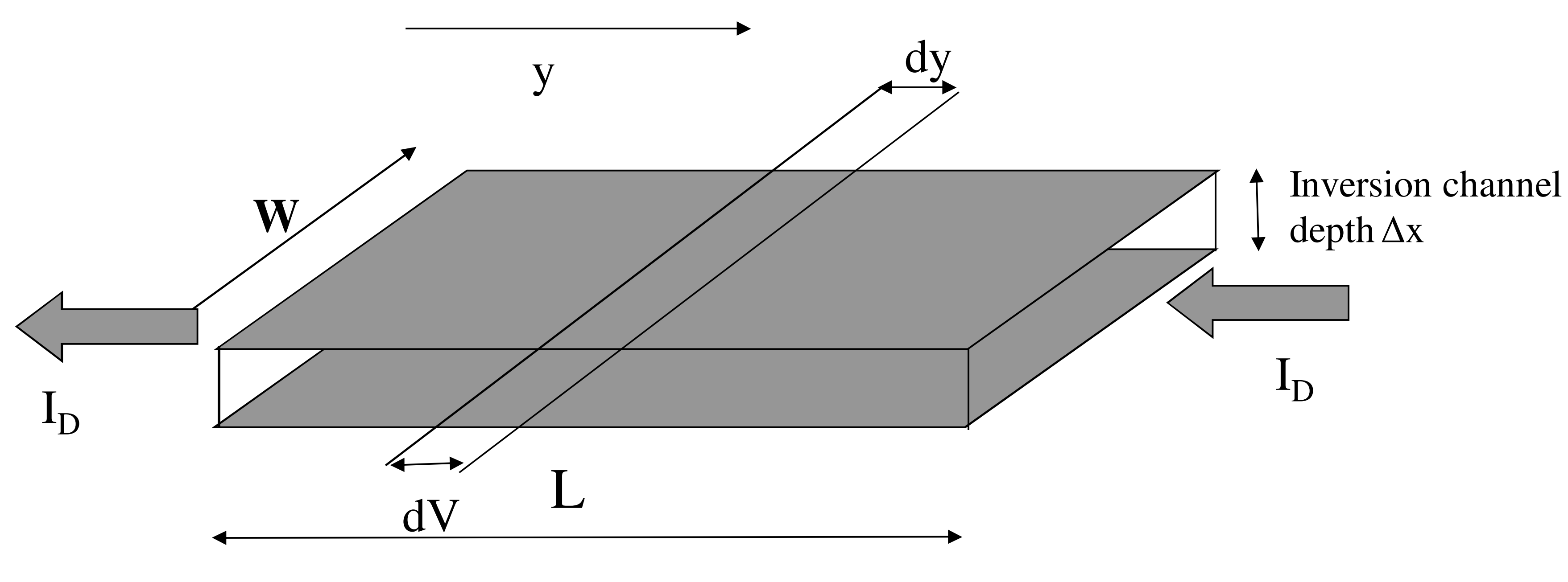


Strong inversion model: the electron (inversion) charge density along the channel is $Q_N = - C_{OX} (V_{GS} – V_T - V)$ with $0<V<V_{DS}$

and the current is due to drift (Ohm's law valid in each channel element)

MOSFET current law -I

- Resistance of channel element of length Δy



$$dR_{ch} = \frac{dy}{W\Delta x}\frac{1}{qn\mu} = -\frac{dy}{WQ_N\mu}$$

MOSFET current law -II

- Ohm's Law applied to the channel element of width W and length dy

$$dV = dR_{ch} I_D \qquad dR_{ch} = -\frac{dy}{W \mu Q_N}$$

$$I_D dy = -W \mu Q_N dV$$

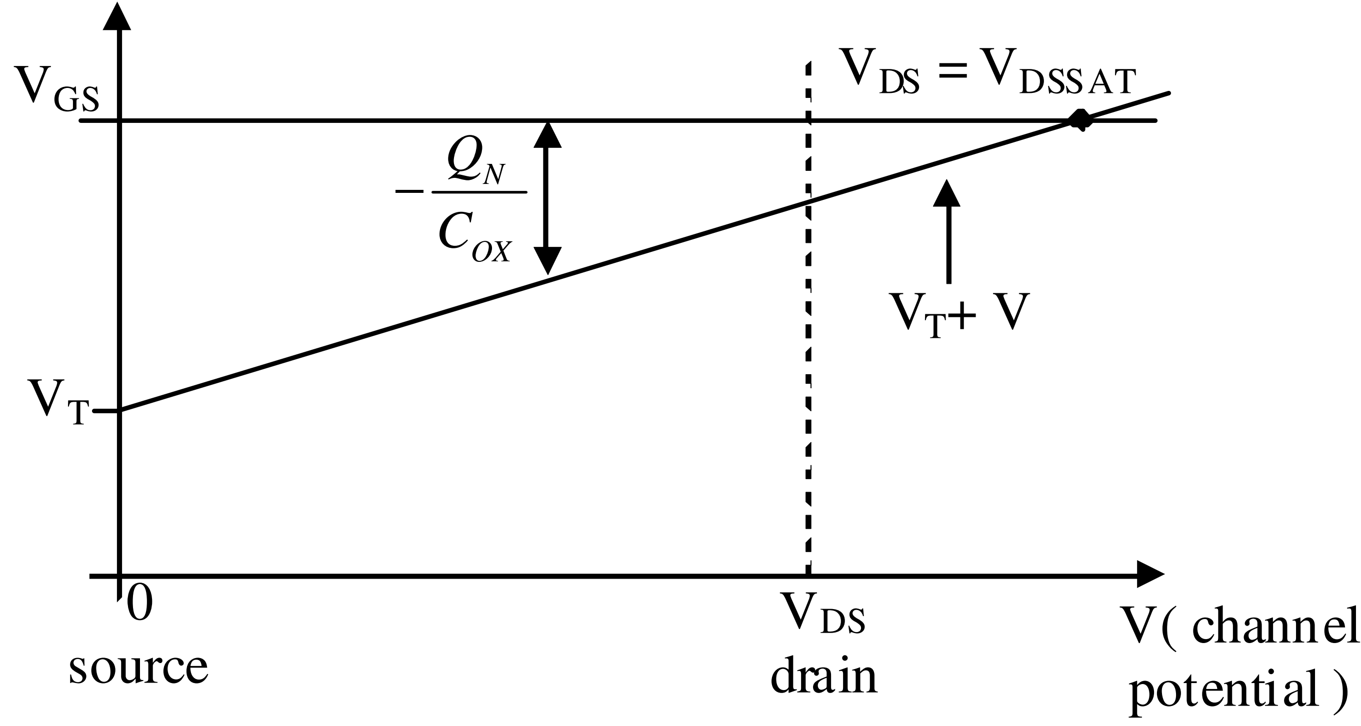
- Integrating the eq. above from source to drain

$$\int_0^L I_D dy = -\int_0^{V_{DS}} W \mu Q_N dV$$

$$I_D = -\frac{W}{L} \mu \int_0^{V_{DS}} Q_N dV$$

MOSFET current law -III

$$Q_N = -C_{ox}\left(V_{GS} - V_T - V\right)$$



MOSFET current law -IV

- Substituting the inversion charge density given by

  $Q_N = - C_{OX} (V_{GS} - V_T - V)$ in
  $$I_D = -\frac{W}{L}\mu \int_0^{V_{DS}} Q_N dV$$

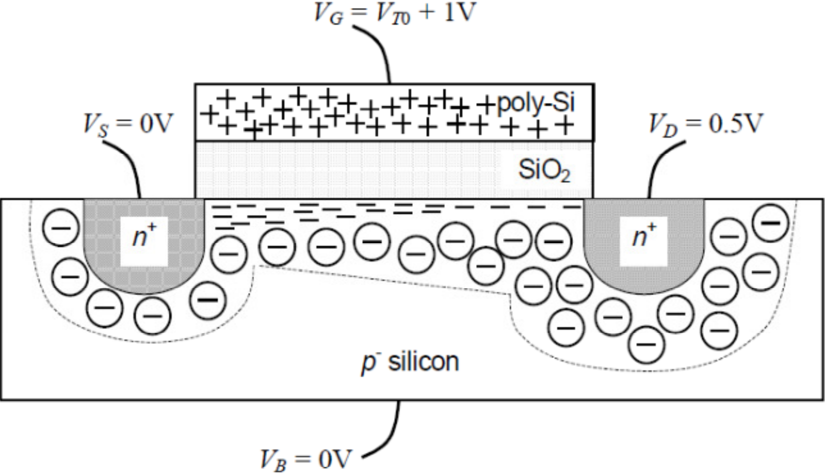
it follows that

$$I_D = \frac{W}{L}\mu \int_0^{V_{DS}} C_{ox}\left(V_{GS} - V_T - V\right) dV$$

$$I_D = \frac{W}{L}\mu C_{ox}\left[\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

Bulk effect

- We have neglected the variation of the depletion charge under the channel



- Including this effect reduces the drain current

$$I_D = \frac{W}{2Ln}\mu C_{ox}\left(V_{GS} - V_T\right)^2 \qquad \frac{C_{ox}}{C_{ox} + C_d} = \frac{1}{n}$$

Typical values of $n \sim 1.1$ to 1.5
n is a slight function of V_G

The output characteristics of the MOSFET in saturation

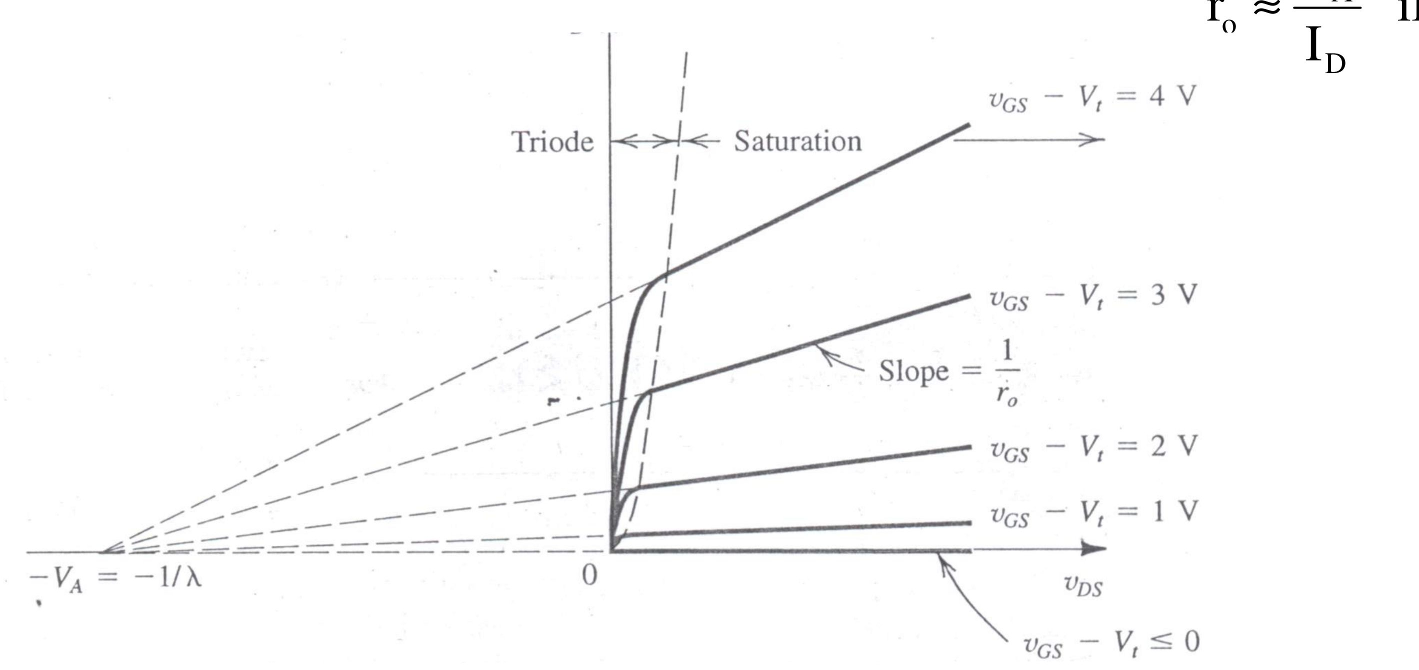
$$I_D = \frac{W}{2L}\mu C_{ox}\left(V_{GS} - V_T\right)^2\left(1 + \frac{V_{DS}}{V_A}\right)$$

if $V_{DS} \geq V_{DSSAT}$, $V_{GS} \geq V_T$

output resistance:

$$r_o = \left[\frac{\partial i_D}{\partial v_{DS}}\bigg|_Q\right]^{-1} = \frac{V_{DS} + V_A}{I_D}$$

$$r_o \approx \frac{V_A}{I_D} \quad \text{if} \quad V_{DS} << V_A$$



• Channel length modulation

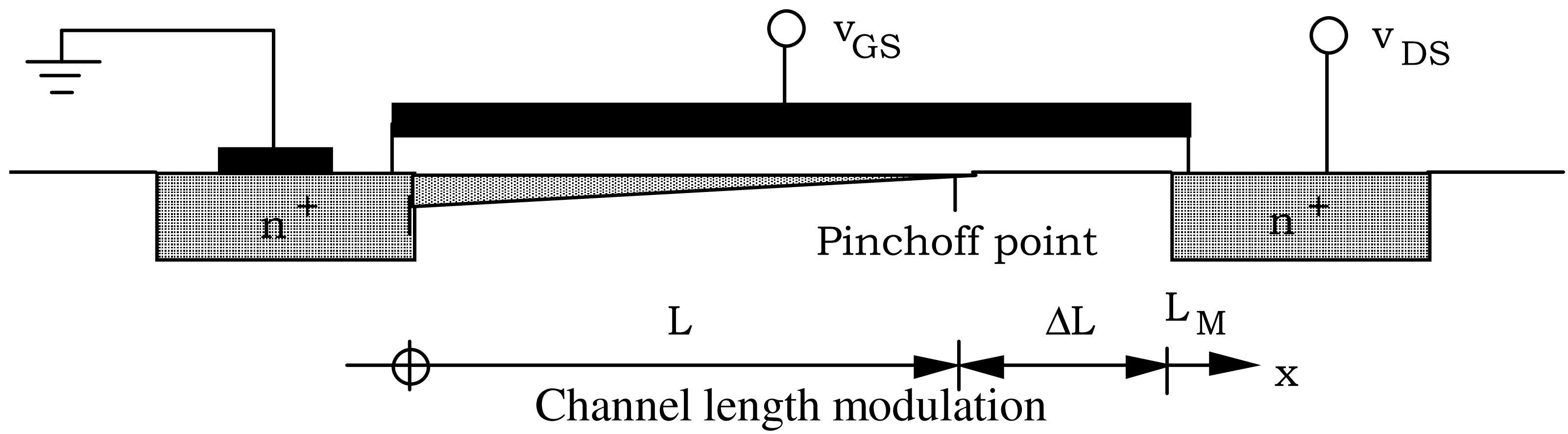
$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

$$L = L_M - \Delta L$$

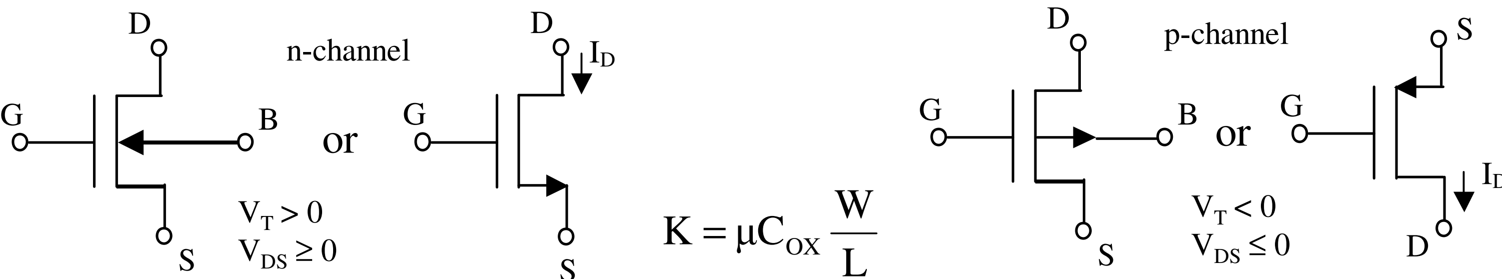
$$I_D = \frac{I_{DSAT}}{1 - \frac{\Delta L}{L_M}} \cong I_{DSAT}\left(1 + \frac{\Delta L}{L_M}\right)$$

$$\frac{\Delta L}{L_M} = \frac{V_{DS}}{V_A}$$

$$I_D = \frac{k_n}{2}(V_{GS} - V_T)^2\left(1 + \frac{V_{DS}}{V_A}\right)$$



Summary of DC equations for the MOSFET

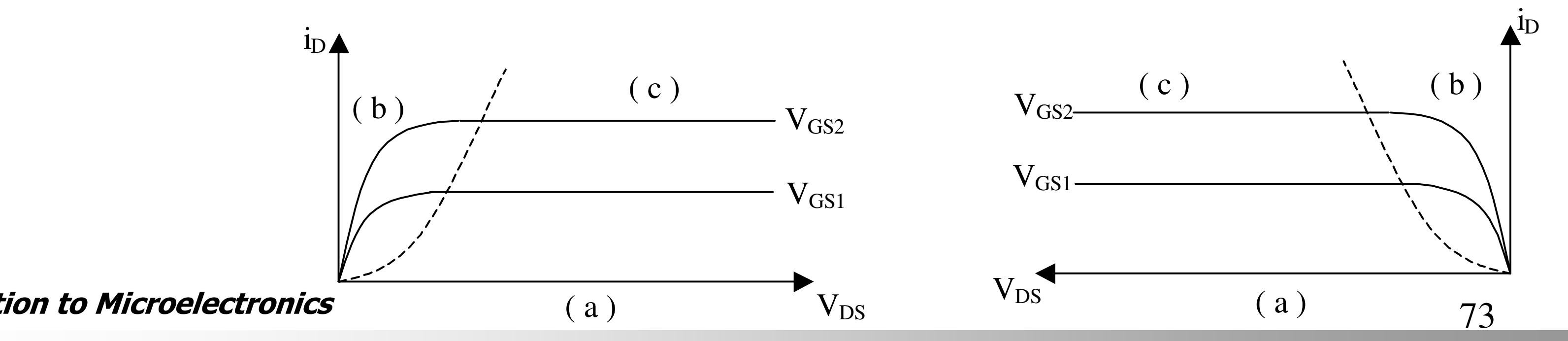


$$K = \mu C_{OX} \frac{W}{L}$$

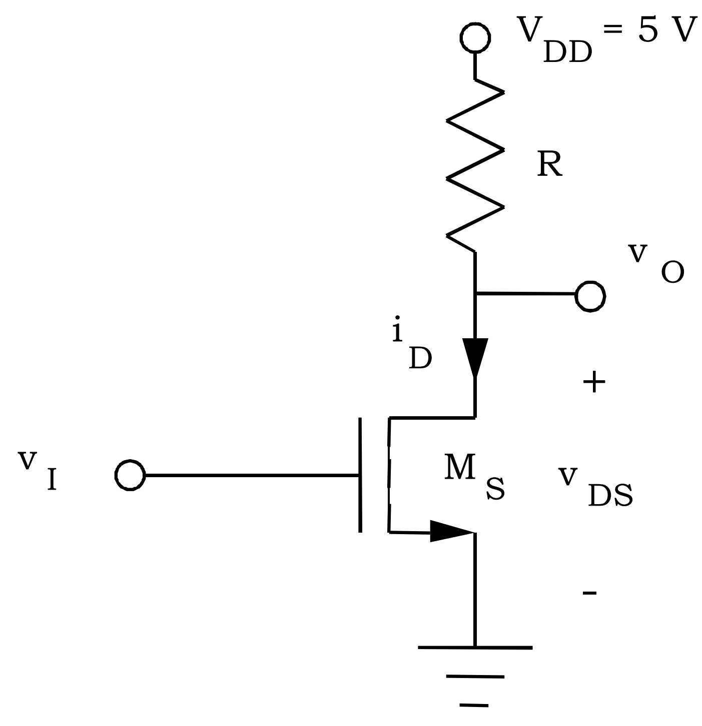
(a) $v_{GS} < V_T$	Cutoff region, $i_D \approx 0$	$v_{GS} \geq V_T$

(b) $v_{GS} \geq V_T$	Triode region	$v_{GS} \leq V_T$
$(v_{GD} \geq V_T)$ $v_{DS} \leq v_{GS} - V_T$	$I_D = \frac{W}{L}\mu C_{ox}\left[(V_{GS}-V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$	$v_{DS} \geq v_{GS} - V_T$ $(v_{GD} \leq V_T)$

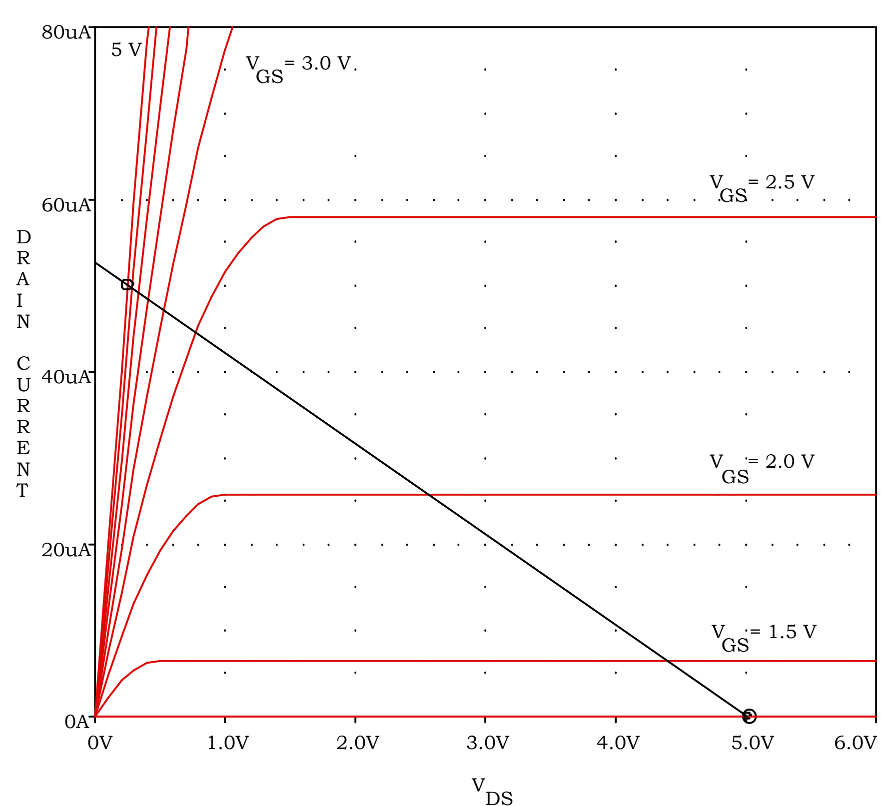
(b) $v_{GS} \geq V_T$	Saturation region	$v_{GS} \leq V_T$
$(v_{GD} \leq V_T)$ $v_{DS} \geq v_{GS} - V_T$	$I_D = \frac{W}{2L}\mu C_{ox}(V_{GS}-V_T)^2$	$v_{DS} \leq v_{GS} - V_T$ $(v_{GD} \geq V_T)$



nMOS Inverter Circuit-I



NMOS inverter with resistive load

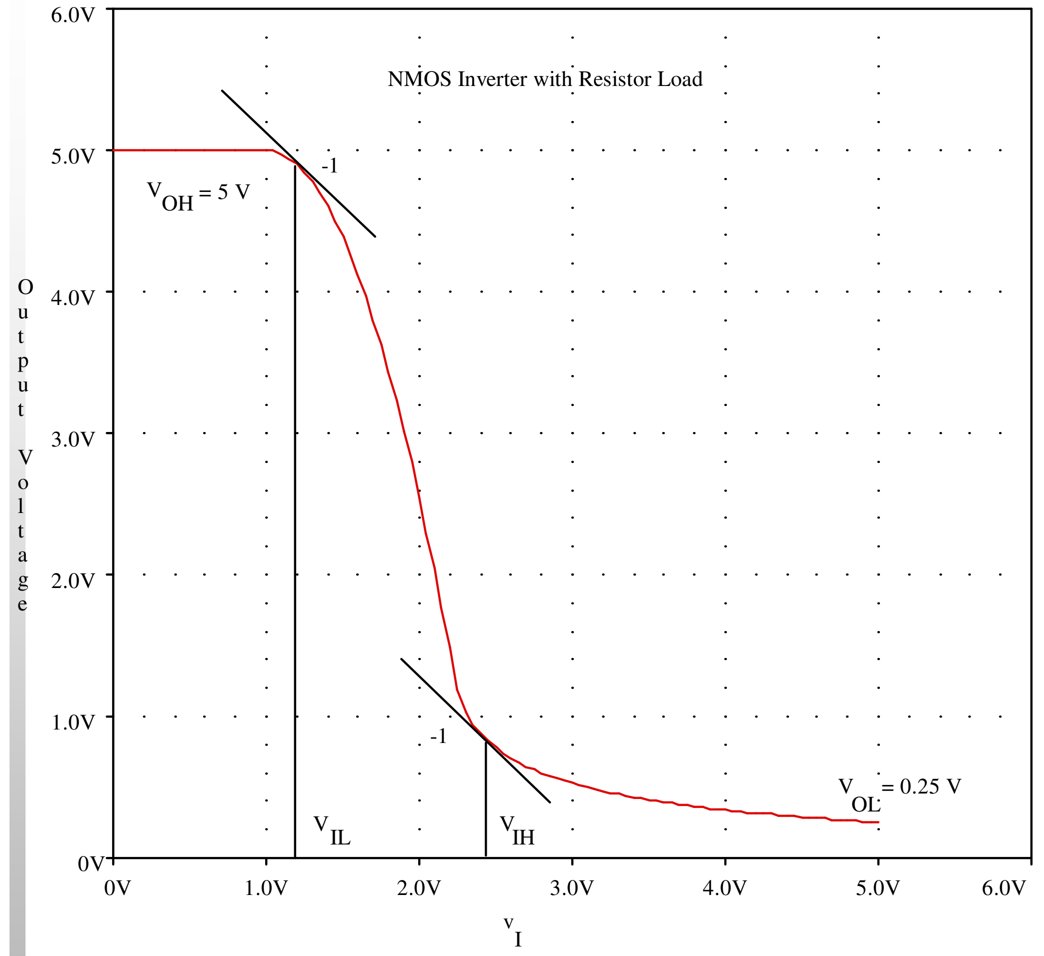


MOSFET output characteristics and load line

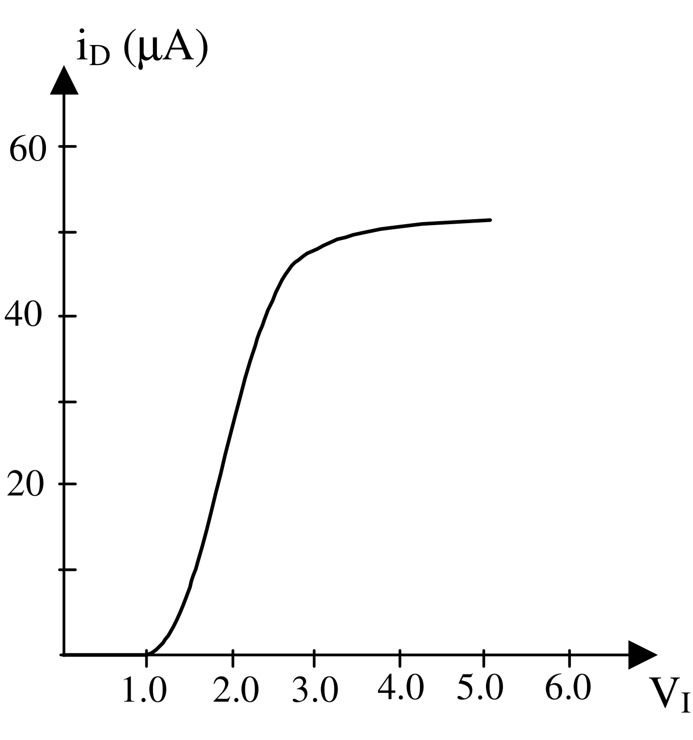
$V_{DD} = 5$ V
$R = 95$ kΩ

Load line: $$i_D = \frac{V_{DD} - v_{DS}}{R}$$

nMOS Inverter Circuit-II



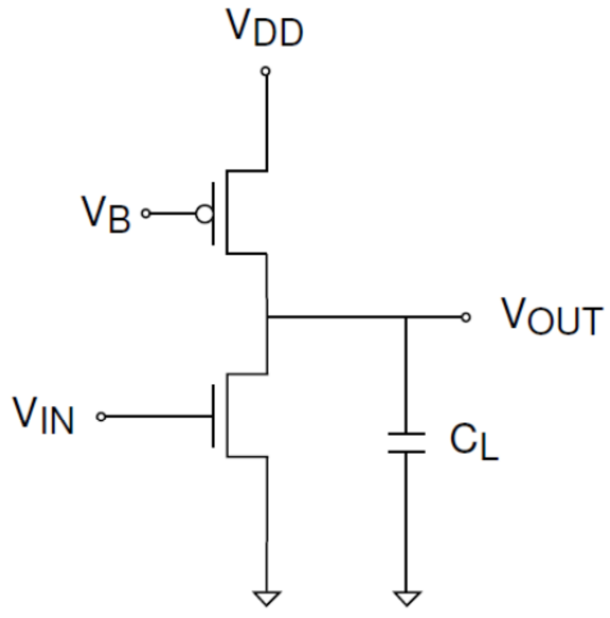
Simulated transfer characteristic of an NMOS logic gate with resistive load

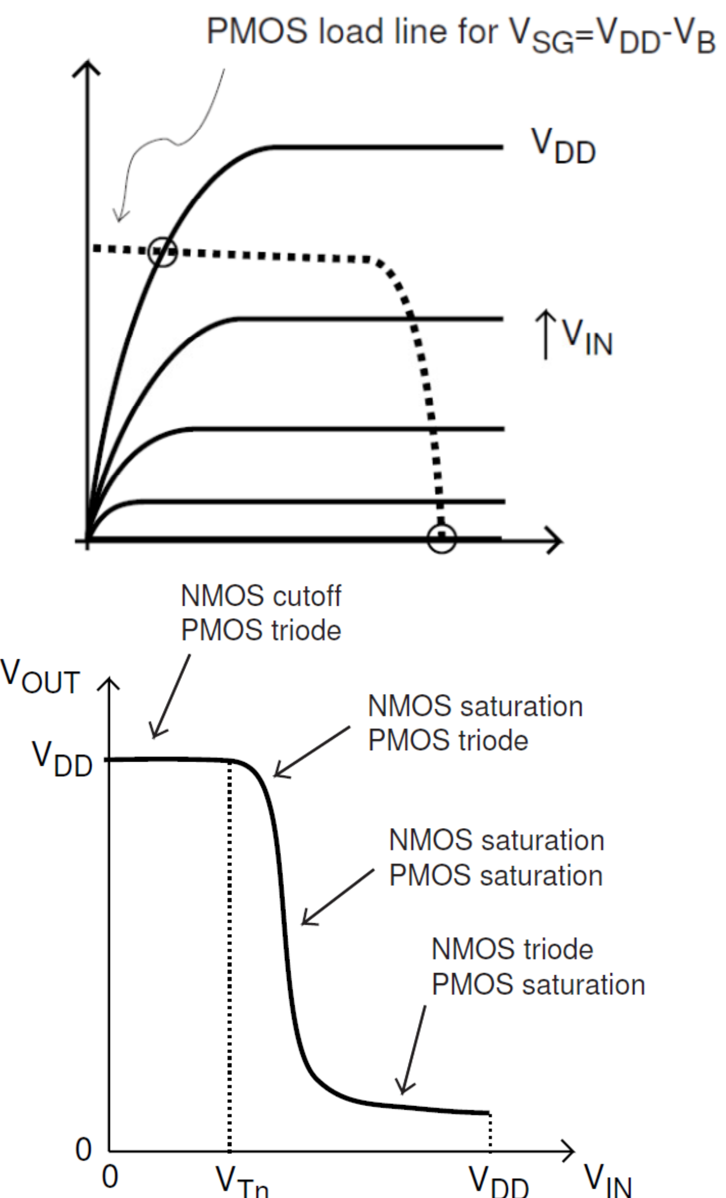


Drain current vs. input voltage

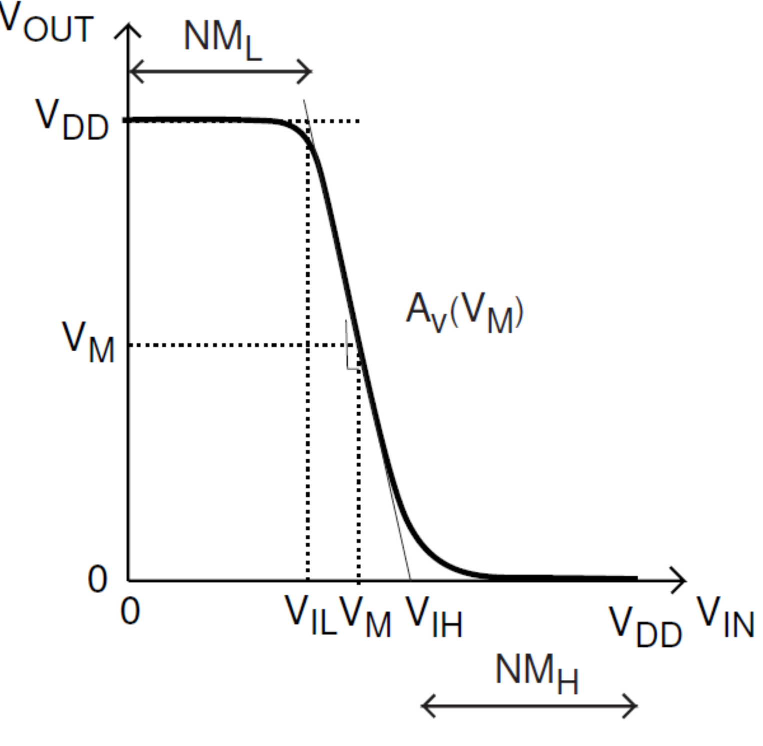
Drawback: current consumption ≈ 50 μA if the input is high

Inverter circuit – PMOS transistor load





CMOS INVERTER LOGIC THRESHOLD-I



At V_M both transistors are saturated

$$I_{Dn} = \frac{W_n}{2L_n}\mu_n C_{ox}\left(V_M - V_{Tn}\right)^2$$

$$I_{Dp} = \frac{W_p}{2L_p}\mu_p C_{ox}\left(V_{DD} - V_M + V_{Tp}\right)^2$$

CMOS INVERTER LOGIC THRESHOLD-II

Define $k_n = \frac{W_n}{L_n} \mu_n C_{ox}$ $k_P = \frac{W_p}{L_p} \mu_p C_{ox}$

Since $I_{Dn} = I_{Dp}$

Then

$$\frac{k_n}{2}\left(V_M - V_{Tn}\right)^2 = \frac{k_p}{2}\left(V_{DD} - V_M + V_{Tp}\right)^2$$

Solve for V_M

$$V_M = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}\left(V_{DD} + V_{Tp}\right)}{1 + \sqrt{\frac{k_p}{k_n}}}$$

CMOS INVERTER LOGIC THRESHOLD-III

Symmetric case $V_{Tp} = -V_{Tn} \quad k_p = k_n \qquad V_M = \dfrac{V_{DD}}{2}$

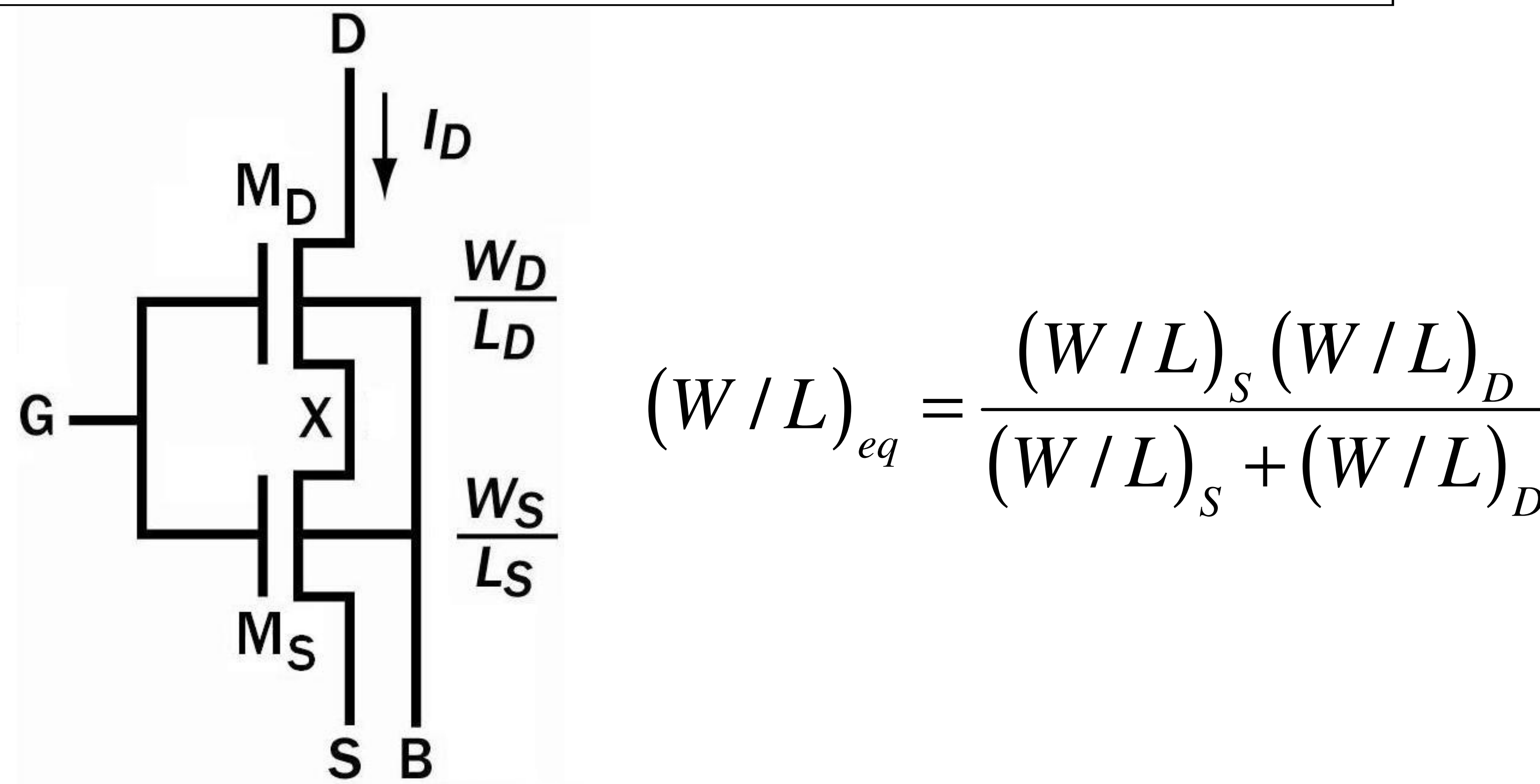
This implies $\dfrac{W_p}{L_p} \cong 2\dfrac{W_n}{L_n}$

Asymmetric cases

$$k_n >> k_p \quad \Rightarrow \quad V_M \cong V_{Tn}$$

$$k_n << k_p \quad \Rightarrow \quad V_M \cong V_{DD} + V_{Tp}$$

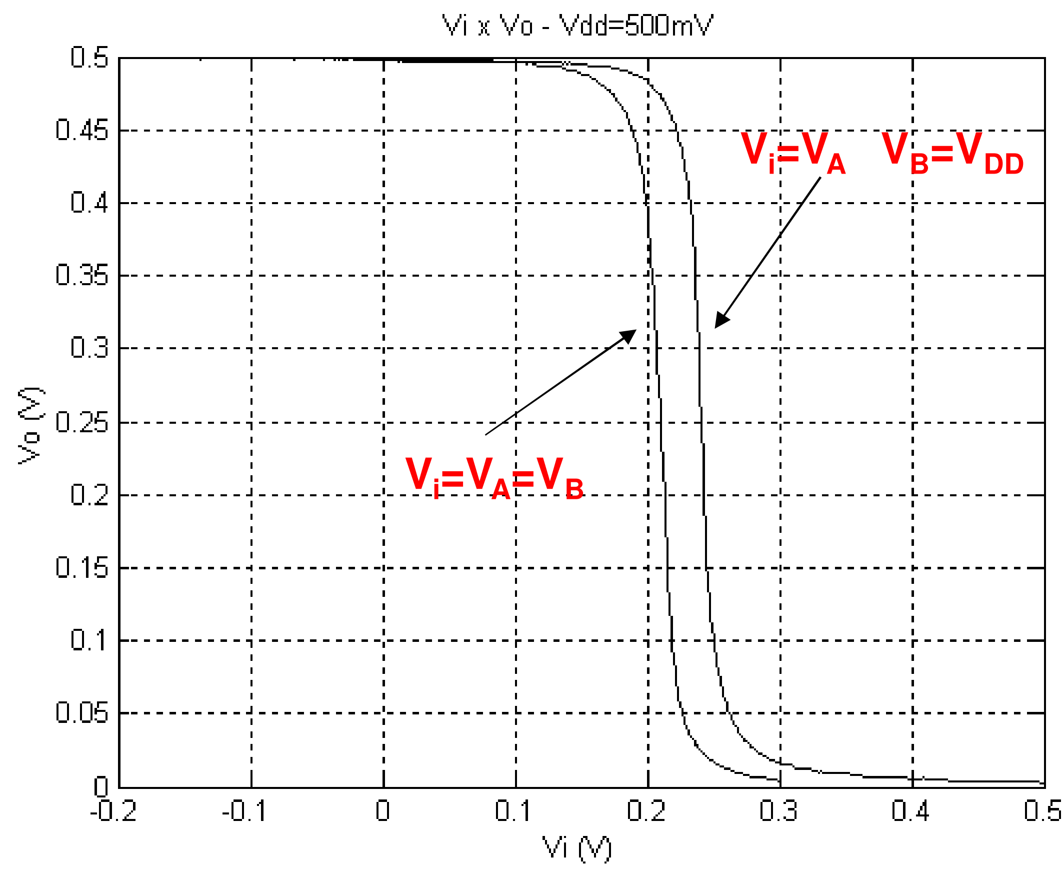
Modeling the series association of MOSFETs



Experimental Results NAND-2

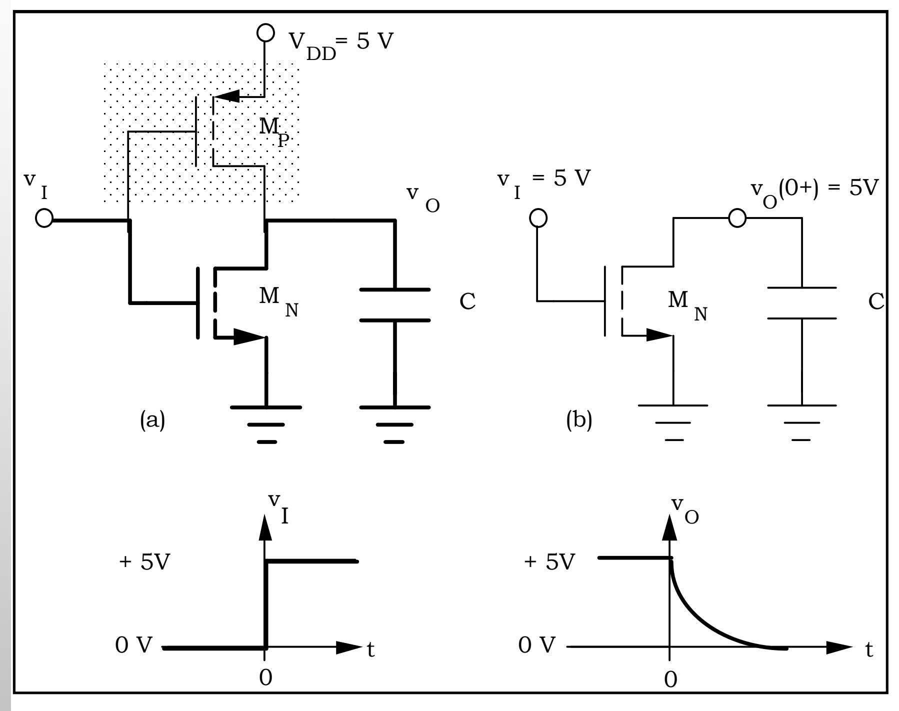
DC Transfer Curve

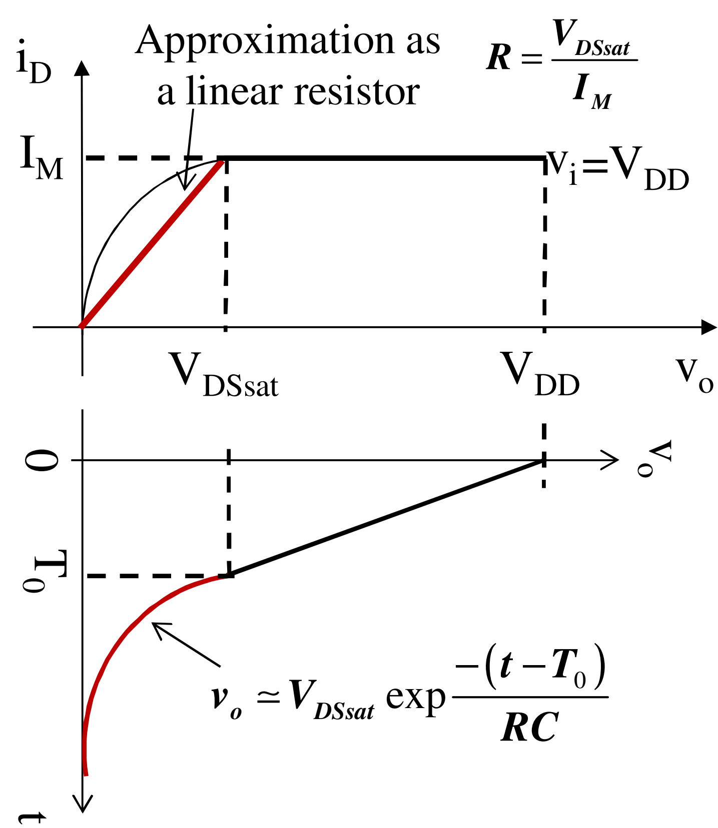
TSMC 0.35µm Technology



• Dynamic Operation of the CMOS Inverter - 2

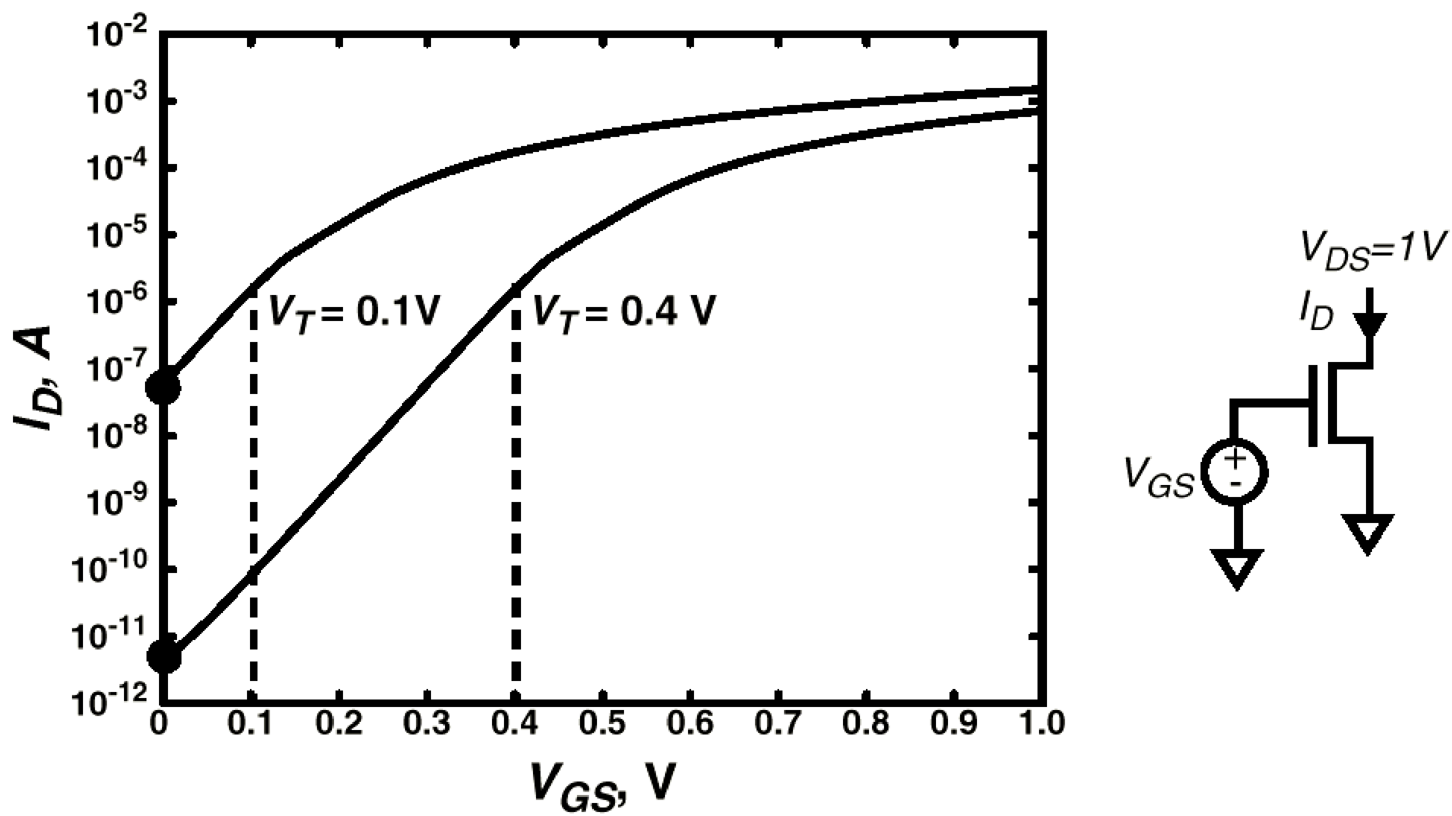
High-to-low output transition in a CMOS inverter





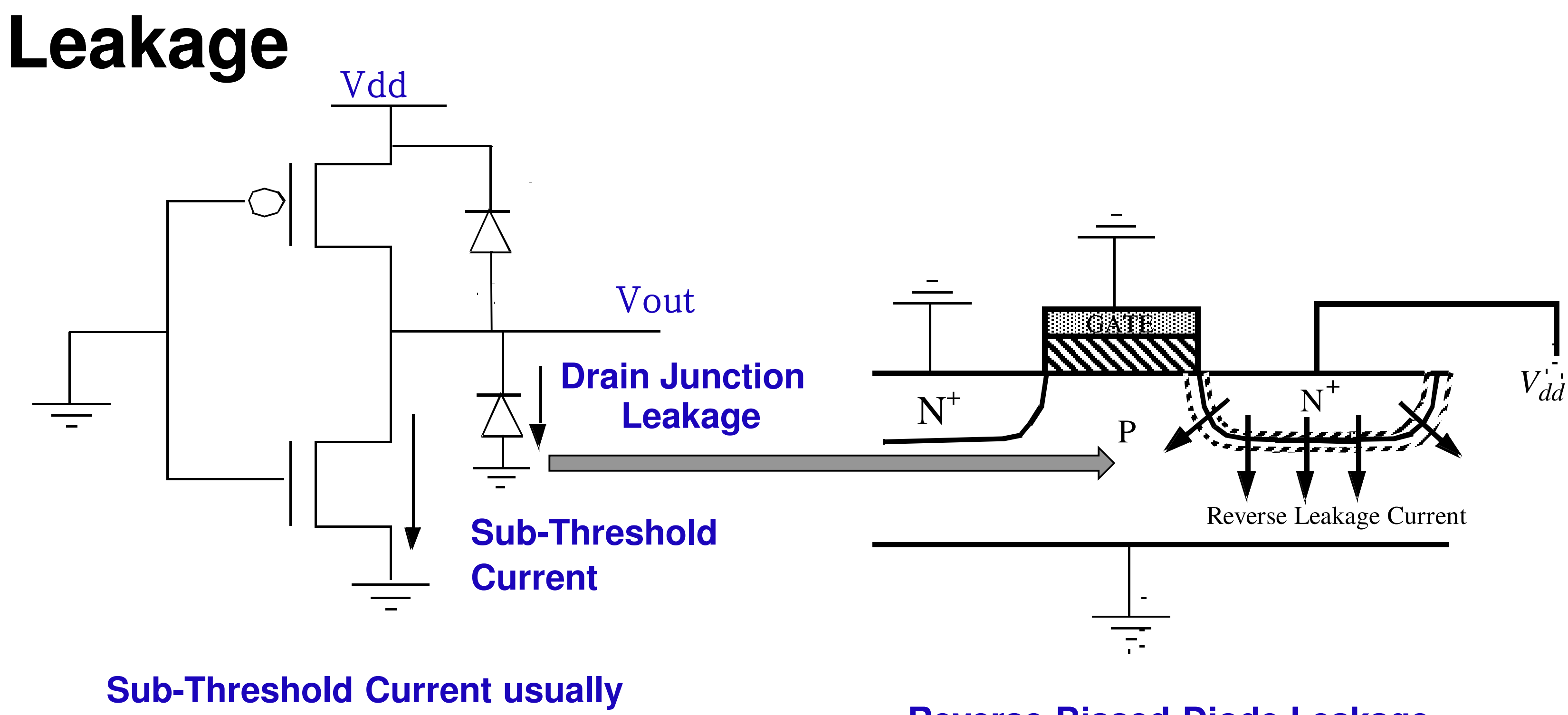
$$T_0 = C\frac{V_{DD} - V_{DSsat}}{I_M}$$

Subthreshold Leakage Component



- Leakage control is critical for low-voltage operation

Leakage

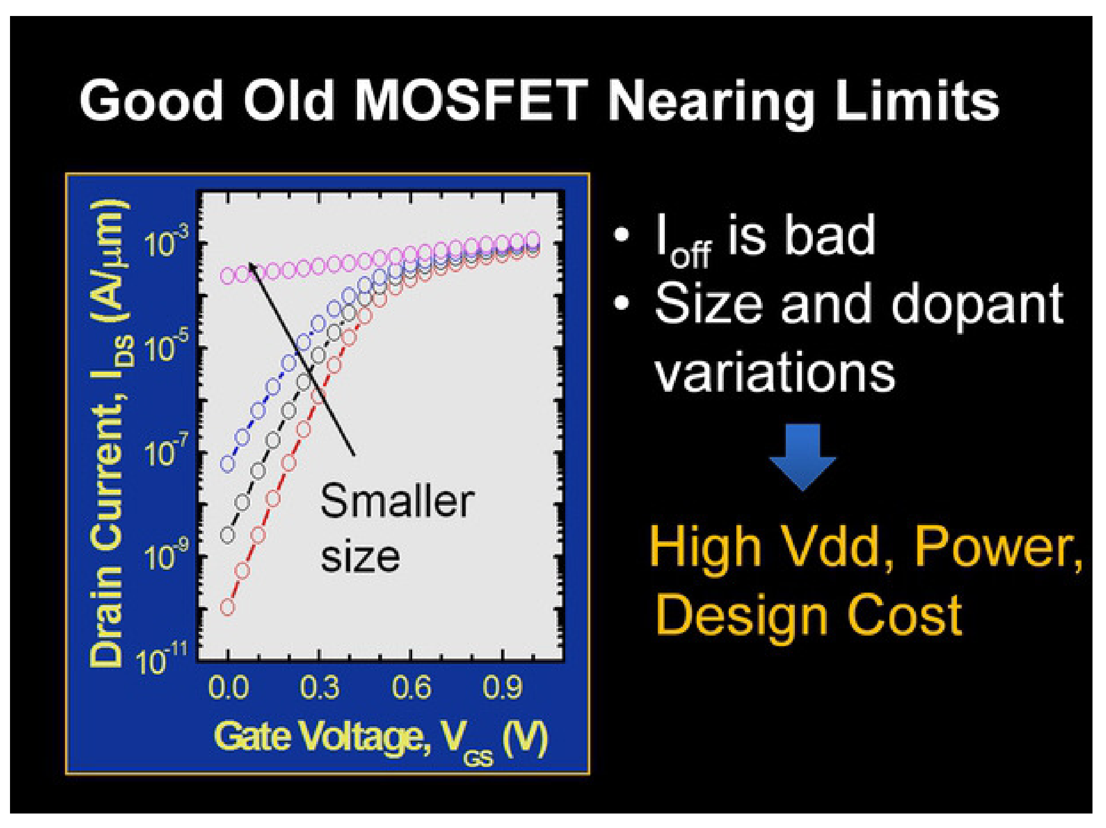


Sub-Threshold Current usually Dominant Factor

Reverse-Biased Diode Leakage

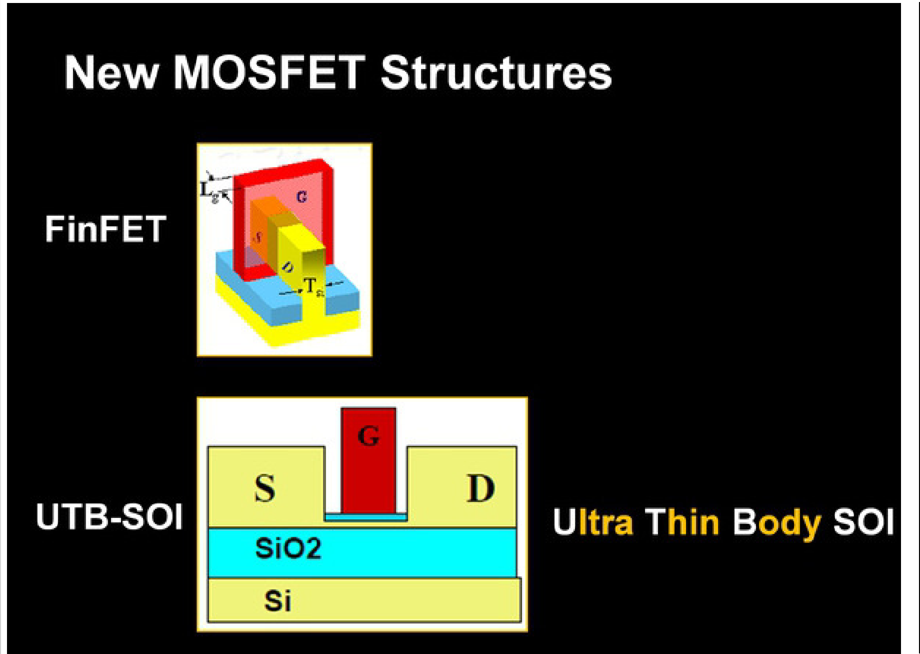
Principles for Power Reduction

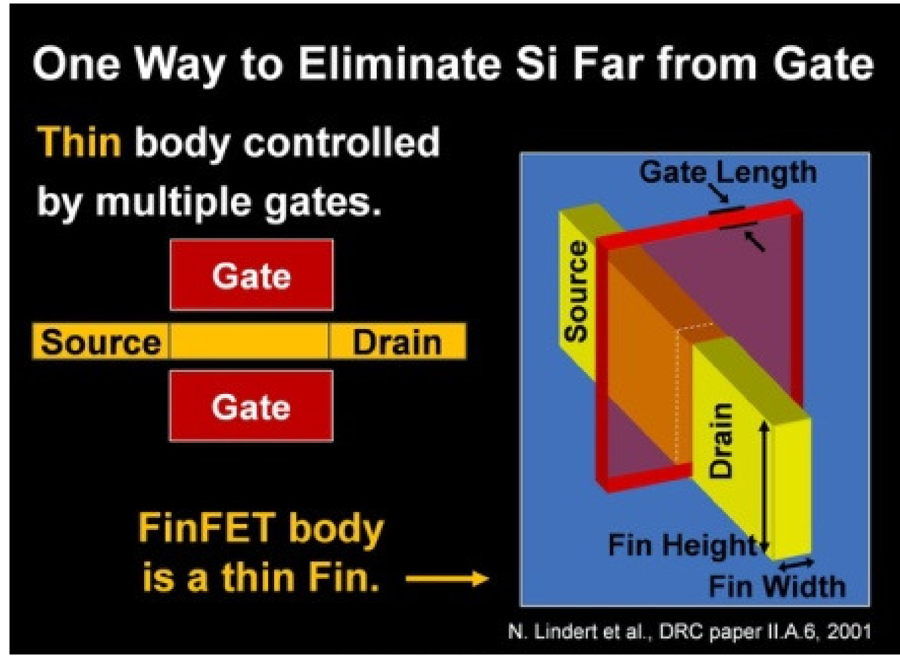
- Prime choice: Reduce voltage!
  - Recent years have seen an acceleration in supply voltage reduction
  - Design at very low voltages still open question (0.9…. 0.6… 0.1? V)
- Reduce switching activity
- Reduce physical capacitance



3D FinFET
New Structure Rejuvenates Transistor!
Dr. Chenming Hu
University of California Berkeley
http://www.eecs.berkeley.edu/~hu/

http://www.synopsys.com/Community/SNUG/Silicon%20Valley/Pages/snug-2012-keynote-3d-finfet.aspx





http://www.synopsys.com/Community/SNUG/Silicon%20Valley/Pages/snug-2012-keynote-3d-finfet.aspx