Chapter

7

DC-to-AC Conversions

Although most of this book has been dedicated to the modeling and simulation of DC-to-DC converters, there are applications such as uninterruptible power supplies (UPS) that convert a DC input voltage to a sinusoidal AC output voltage. The basis of the conversion is very similar to that of the conversion of a DC input voltage to a DC output voltage.

One of the more difficult aspects of DC-to-AC conversion is obtaining a regulated, low-distortion sine-wave reference. Several example circuits that demonstrate different techniques for generating sine-wave references are contained in this chapter.

Using SPICE to Generate a Sine ROM

The following example demonstrates an unusual task for SPICE. This example is the result of an actual design for a three-phase sine-wave reference (only one phase is shown). The circuit simulates a single-bit pulse code representation of a sine wave. The implementation is accomplished using a microprocessor that generates a 4-bit word. One bit is used for each of the three-phase references, while the fourth bit is used to generate a synchronization pulse that is required by other circuits. The microprocessor functions as a crystal oscillator and counter. This implementation allows the microprocessor to support functions such as programmable frequency, which are used to support 50-, 60-, and 400-Hz outputs. Much of the protection circuitry is also realized by the microprocessor.

The fundamental problem is the generation of a bit pattern for the sine-wave reference. The circuit in Fig. 7.1 shows a novel approach for generating the bit pattern for a single phase. The same circuit is easily extended to three phases (or any other number of phases).

The pulse generator, V1, is used as the clock. Because we will generate 256 values in the table, this clock is 256 times greater than the output frequency. Flip-flop X1 was created using logic expressions. It latches the data between clock pulses. V2 is a sine wave that is used as a reference in the circuit. R1, R5, C1, and C2 filter the pulse-coded waveform and reconstruct the sine wave. EB1 is a simple comparator that sets the output bit high if the sine-wave output is lower than the sine-wave reference value or sets the output bit low if the sine-wave output is higher than the sine-wave reference value. EB2 shifts the level of the bit values to a zero-one format (if V(3) is greater than 1, then V(9) is set to 1 V; otherwise, V(9) is set to 0 V).

The SPICE .FOUR analysis is performed on the sine-wave output in order to place the total harmonic distortion in the output table. The circuit is simulated several times, with different amplitude values for V2. The lowest distortion occurs with the values listed in Fig. 7.1. As we look at the output data, we can see the bit patterns and the sine-wave output at each filter stage. Note that more sophisticated filters could produce lower distortion, as could more values in the data table. Figure 7.2 shows the sine-wave output waveform and the one-zero bit pattern produced by EB2.

Note that the circuit starts with zero initial voltage. For this reason, two cycles are simulated and the data for the Fourier analysis are extracted only from the second cycle so that the transient residues are eliminated.

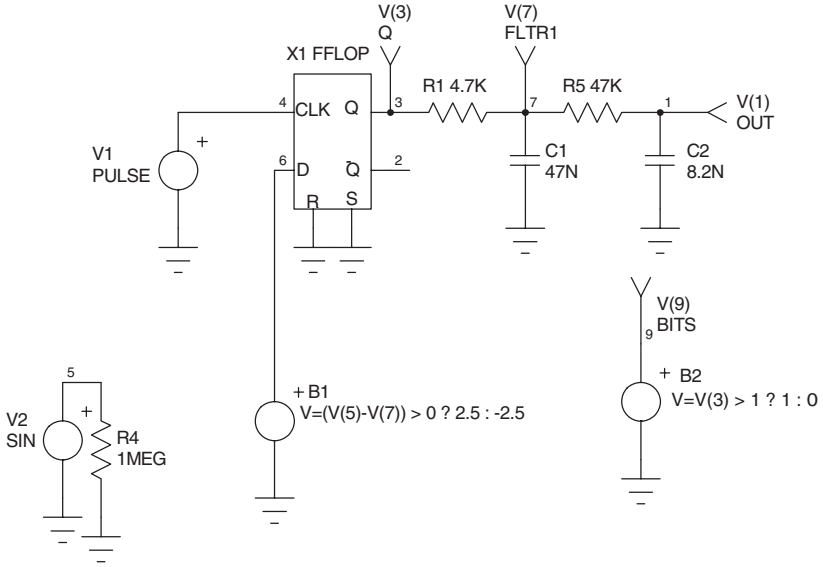


Figure 7.1 Schematic and netlist showing a novel approach for generating a bit pattern.

```
SINE: BIT PATTERN GENERATOR
.TRAN 9.766U 9M 0 1U UIC
.FOUR 400HZ V(1)
.PROBE
* V(1)=OUT
*V(3)=Q
*V(9)=BITS
*V(7)=FLTR1
.PRINT TRAN V(1) V(3) V(9) V(7)
R1 3 7 4.7K
C1 7 0 47N IC=0
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
V2 5 0 SIN 0 1.5 400
R4 5 0 1MEG
R5 7 1 47K
C2 1 0 8.2N IC=0
EB1 6 0 Value={ IF ( (V(5)-V(7)) > 0 , 2.5 , -2.5 ) }
EB2 9 0 Value={ IF ( V(3) > 1 , 1 , 0 ) }
X1 4 6 0 0 2 3 FFLOPZero

.SUBCKT FFLOPZero 1 2 11 12 5 6
* CLK D R S QB Q
X1 7 4 2 8 NAND3Z_0
X2 8 3 10 9 NAND3Z_0
X3 1 8 10 7 NAND3Z_1
X4 4 9 1 10 NAND3Z_0
X5 4 7 6 5 NAND3Z_1
X6 5 10 3 6 NAND3Z_0
X7 11 4 INVZ
X8 12 3 INVZ
.ENDS FFLOPZero
*
.SUBCKT NAND3Z_0 1 2 3 4
E1 5 0 VALUE = { IF ( (V(1)>0) & (V(2)>0) & (V(3)>0), -2.5, 2.5 ) }
R1 5 4 400
C1 4 0 20P IC=0
.ENDS NAND3Z_0
*
.SUBCKT NAND3Z_1 1 2 3 4
E1 5 0 VALUE = { IF ( (V(1)>0) & (V(2)>0) & (V(3)>0), -2.5, 2.5 ) }
R1 5 4 400
C1 4 0 20P IC=5
.ENDS NAND3Z_1
*
.SUBCKT INVZ 1 2
E1 3 0 VALUE = { IF ( V(1)>0, -2.5, 5 ) }
R1 3 2 100
C1 2 0 10P IC=5
.ENDS INVZ

.END
```

Figure 7.1 (*Continued*)

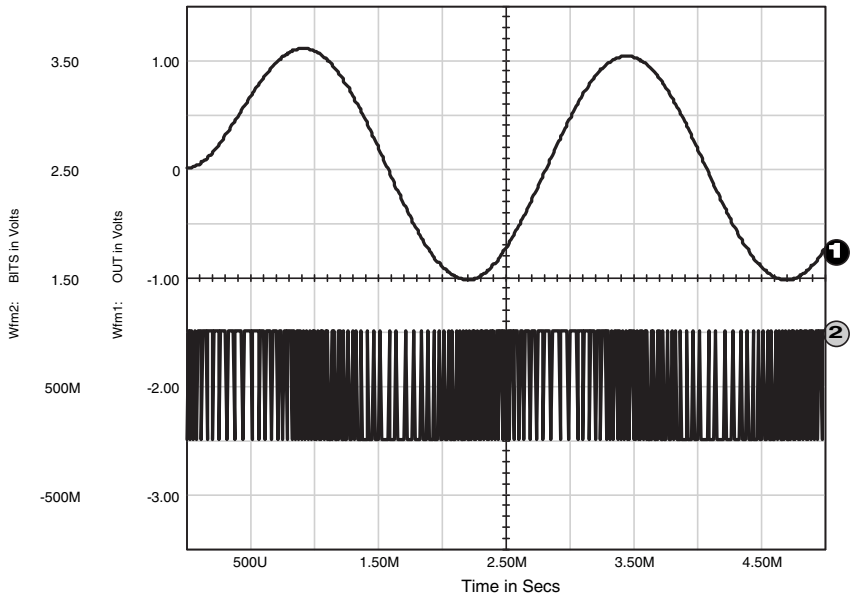


Figure 7.2 Sine-wave output and bit pattern produced by the circuit in Fig. 7.1.

Although this demonstrates the circuit operation, it does not produce the data in a desirable format. A section of the output listing is shown in Fig. 7.3.

The distortion analysis results are displayed along with the output data in the output file. To obtain the table in the desired format, we will resimulate a modified version of the circuit. The .OPTIONS Numdgt=1 setting causes the output to be displayed in the output file using no decimal places. Only one column of data will appear in the output file. The column is the bit pattern. The numbers are displayed in the exponential format. Via the search and replace command found in most text editors, we can clean up the two values that are present. Replace 1e+000 with 1, and replace 0e+000 with 0. The result will be a bit pattern, as shown in the partial output file in Fig. 7.4.

The left column is our bit pattern (which has 256 values) and the right column is the index (think of the index as an address ranging from 0 to 255).

This bit pattern can now be coded into ROM. To achieve a three-phase bit pattern, the circuit can be copied three times and the sine-wave reference can be replaced by a three-phase reference. The result will be three columns of bit data and an index column.

State Machine Modeling in XSPICE

Some SPICE simulators have the ability to model digital functions by using a state machine model (see chap. 8). State machine models allow

```
**** 04/22/05 11:14:34 ******* PSpice 10.0.0 (Jan 2003) *******
 SINE: BIT PATTERN GENERATOR
****     FOURIER  ANALYSIS                TEMPERATURE =   27.000 DEG C
 ************************************************************
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(1)
DC COMPONENT = 7.470631E-04
```

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	4.000E+02	1.035E+00	1.000E+00	1.704E+02	0.000E+00
2	8.000E+02	1.618E-03	1.564E-03	5.586E+01	-2.850E+02
3	1.200E+03	9.813E-04	9.482E-04	1.264E+02	-3.849E+02
4	1.600E+03	6.173E-04	5.965E-04	1.679E+02	-5.139E+02
5	2.000E+03	1.506E-03	1.456E-03	6.730E+01	-7.849E+02
6	2.400E+03	3.724E-04	3.599E-04	-1.354E+02	-1.158E+03
7	2.800E+03	5.308E-04	5.129E-04	-1.345E+02	-1.328E+03
8	3.200E+03	2.945E-04	2.846E-04	-7.875E+01	-1.442E+03
9	3.600E+03	2.342E-04	2.263E-04	1.356E+02	-1.398E+03

```
   TOTAL HARMONIC DISTORTION =   2.518698E-01 PERCENT

**** 04/22/05 11:14:34 ******* PSpice 10.0.0 (Jan 2003) *******
 SINE: BIT PATTERN GENERATOR

 ****     TRANSIENT ANALYSIS               TEMPERATURE =   27.000 DEG C

************************************************************

  TIME       V(1)       V(3)       V(9)       V(7)

  0.000E+00   1.601E-15  -1.383E-04   0.000E+00   4.617E-09
  9.766E-06   1.248E-03   2.312E+00   1.000E+00   9.912E-02
```

Figure 7.3 Partial SPICE Transient data (below) and Fourier results (above) for the simulation in Fig. 7.2.

very fast simulation of large digital systems. The state machine model in Fig. 7.5 ran in 0.48 s, compared with 3.0 s for Fig. 7.1! The results are shown in figure 7.6 for comparison. This same circuit took 79 s in the first edition of this book!

Although this is a very simple circuit, it does illustrate the power and speed improvements that can be attained. In general, the greater the complexity of the digital circuit, the greater the benefit provided by the state machine model. The example in Fig. 7.5 uses the output data from the previous example to create a state machine model for an 8-bit counter with a 256×1 bit ROM.

Referring to the netlist, the state machine model is described by .MODEL STATEA20. Various delays are shown along with a pointer (state_file=sin.txt) to the file containing the state definition table. The

```
SINE: BIT PATTERN GENERATOR
.TRAN 9.766U 4.99M 2.5M 1U UIC
.FOUR 400HZ V(1)
.PROBE
.OPTION NUMDGT=1
* V(1)=OUT
* V(3)=Q
* V(9)=BITS
* V(7)=FLTR1
.PRINT TRAN  V(9)  ; V(3)  V(1)  V(7)
R1 3 7 4.7K
C1 7 0 47N IC=0
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
V2 5 0 SIN 0 1.5 400
R4 5 0 1MEG
R5 7 1 47K
C2 1 0 8.2N IC=0
EB1 6 0 Value={ IF ( (V(5)-V(7)) > 0 , 2.5 , -2.5 ) }
EB2 9 0 Value={ IF ( V(3) > 1 , 1 , 0 ) }
X1 4 6 0 0 2 3 FFLOPZero

TIME  V(9)        INDEX

      0               0
      1               1
      1               2
      0               3
      1               4
      1               5
      0               6
      1               7
      1               8
      1               9
      0               10
```

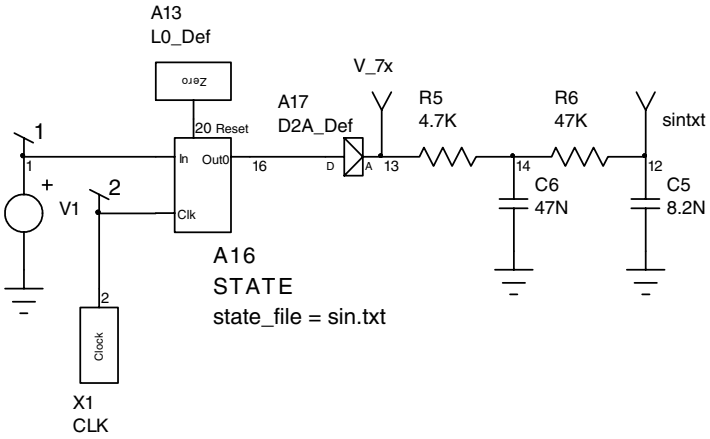
Figure 7.4 Partial output file listing after the transient data have been manipulated. Index column is shown for clarity.

state file model parameter is actually like any other SPICE model parameter, except that instead of being a number its value is that of a file name. The "A" elements describe either digital elements or "bridges." The bridges act like translation devices. These "SPICE" extensions, included in some SPICE simulators, were taken from XSPICE, a public domain version of SPICE 3 that includes a digital logic simulator extension [36]. They convert signals between the various analog (SPICE elements) and pure digital elements (elements used by the logic simulator embedded in XSPICE).

Using the Sine Reference to Drive a Power Stage

The sine reference is useful for generating a reference signal for applications such as a UPS, but it is also capable of directly driving a power stage. The circuit in Fig. 7.7 demonstrates the use of the bit code pattern to directly drive a push-pull converter stage.

Note the distorted waveform and the "spike" at 3.15 ms (see Fig. 7.8), which was generated by the step load. A second simulation was




```
NEWSIN.cir
.TRAN 9.766u 10m 0 UIC
.FOUR 400 v(12)
.PRINT TRAN V_7x .PRINT TRAN sintxt
X1 2 CLK Params: FREQ=102.4K DUTY=50
V1 1 0 DC=0
C5 12 0 8.2N
R5 13 14 4.7K
R6 14 12 47K
A13 20 L0_DefA5
.MODEL L0_DefA5 D_pulldown( load=1.0P)
A17 [ 16 ] [ 13 ] D2A_DefA8
in_high=3.00 rise_delay=1N fall_delay=1N)
.MODEL D2A_DefA8 dac_bridge( out_low=-2.5 out_high=2.5
+ out_undef=0.0E+000 t_rise=1.0N t_fall=1.0N
+ input_load=1.0P)
C6 14 0 47N
A16 [ 1_Din ] 2 20 [ 16 ] STATEA20
.MODEL STATEA20 d_state( clk_delay=1n reset_delay=1n
+ state_file=sin.txt reset_state=0 input_load=1p clk_load=1p
+ reset_load=1p)
A16_Din_1 [ 1] [ 1_Din] A2D
.MODEL A2D adc_bridge( in_low=0.600
.END
```

Figure 7.5 Schematic and associated XSPICE netlist for the sine-wave generator using a state machine model.

performed using an identical circuit, but the input voltage was 28 V, as opposed to 24 V in the first simulation. The output voltages of both simulations are shown in the graph of Fig. 7.9. These two simulations show two major drawbacks of this simple circuit. The first is the relatively high output impedance that results from the output filter. The second is the inability to regulate the output voltage against input voltage

Selected from Output File

Fourier analysis for v(12):

No. Harmonics: 10, THD: 0.264578 %, Gridsize: 200, Interpolation Degree: 1

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	4.00E+02	1.06E+00	-4.37E+01	1.00E+00	0.00E+00
2	8.00E+02	1.77E-03	-1.94E+01	1.67E-03	2.43E+01
3	1.20E+03	9.58E-04	-1.60E+02	9.03E-04	-1.17E+02
4	1.60E+03	6.71E-04	2.45E+01	6.33E-04	6.82E+01
5	2.00E+03	1.65E-03	6.69E+01	1.56E-03	1.11E+02
6	2.40E+03	4.15E-04	1.29E+01	3.91E-04	5.66E+01
7	2.80E+03	5.52E-04	1.53E+02	5.21E-04	1.96E+02
8	3.20E+03	3.43E-04	-6.41E-02	3.23E-04	4.36E+01
9	3.60E+03	2.49E-04	-7.86E+00	2.35E-04	3.58E+01

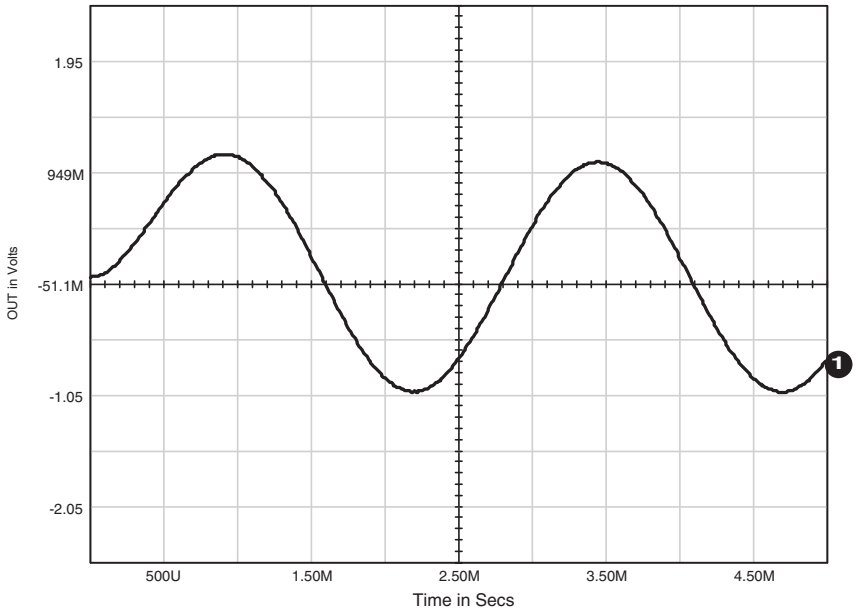


Figure 7.6 Fourier analysis text output (top) and transient response (bottom) of the sine ROM circuit in Fig. 7.5.

changes. The circuit is still useful; however, it should be restricted to applications where the input voltage is stabilized (or the regulation of the output is not a concern) and the load is relatively static. Such applications may include ballasts, motors, and lamps.

Improving the sine-wave power circuit

Both of the weaknesses of the simple circuit shown in Fig. 7.7 can be easily overcome. The circuit in Fig. 7.10 uses a sine reference voltage, V(5),

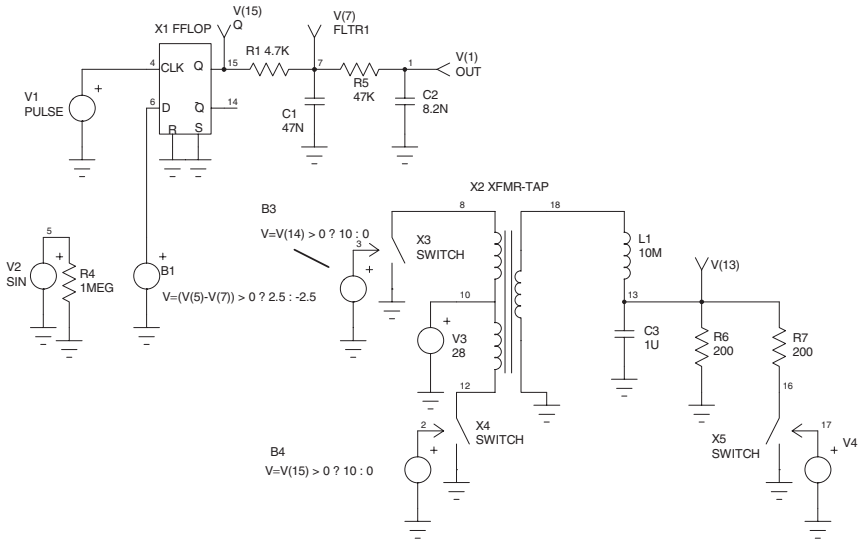


Figure 7.7 A push-pull converter driven by the state machine based sine ROM.

```
UPS:
.PROBE
.TRAN 9.766U 10M UIC
.FOUR 400HZ V(13)
* V(1)=OUT
* V(15)=Q
* V(7)=FLTR1
.PRINT TRAN V(1) V(15) V(7) V(13)
V4 17 0 PWL 0 10 3.125M 10 3.15M 0
EB1 6 0 Value={ IF ( (V(5)-V(7)) > 0 , 2.5 , -2.5 ) }
C2 1 0 8.2N IC=0
C3 13 0 1U
R1 15 7 4.7K
EB3 12 0 Value={ IF ( V(14) > 0 , 10 , 0 ) }
EB4 2 0 Value={ IF ( V(15) > 0 , 10 , 0 ) }
R4 5 0 1MEG
R5 7 1 47K
R6 13 0 200
R7 13 16 200
L1 18 13 10M
X1 4 6 0 0 14 15 FFLOPZero
X2 18 0 8 11 10 XFMR-TAP Params: RATIO=.1
X3 8 0 12 SWITCH
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
X4 10 0 2 SWITCH
V2 5 0 SIN 0 1.5 400
X5 16 0 17 SWITCH
V3 11 0 DC=28
C1 7 0 47N IC=0
.END
```

Figure 7.8 Output of the push-pull converter of Fig. 7.7.

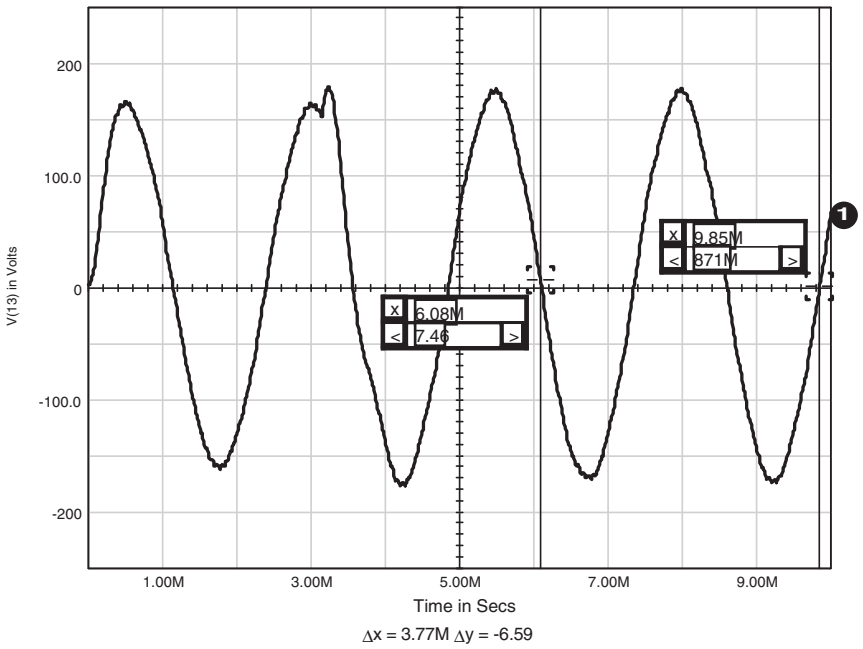


Figure 7.8 (*Continued*)

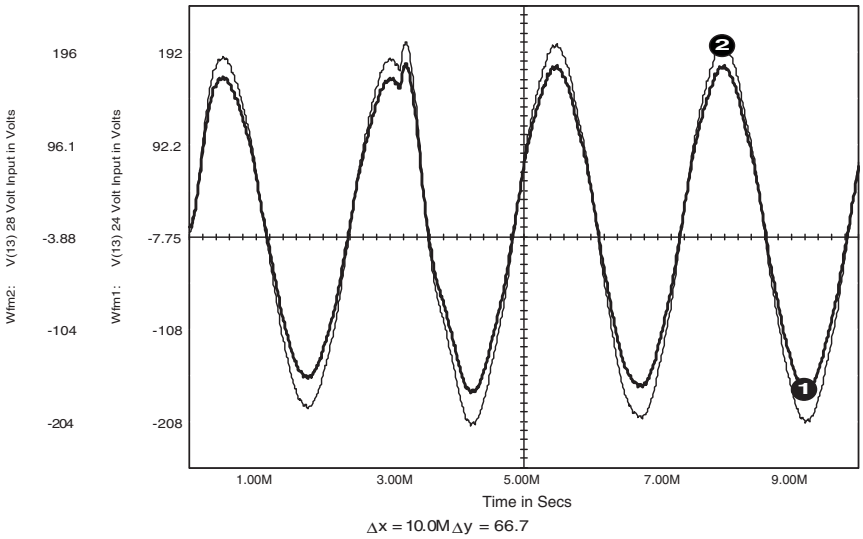
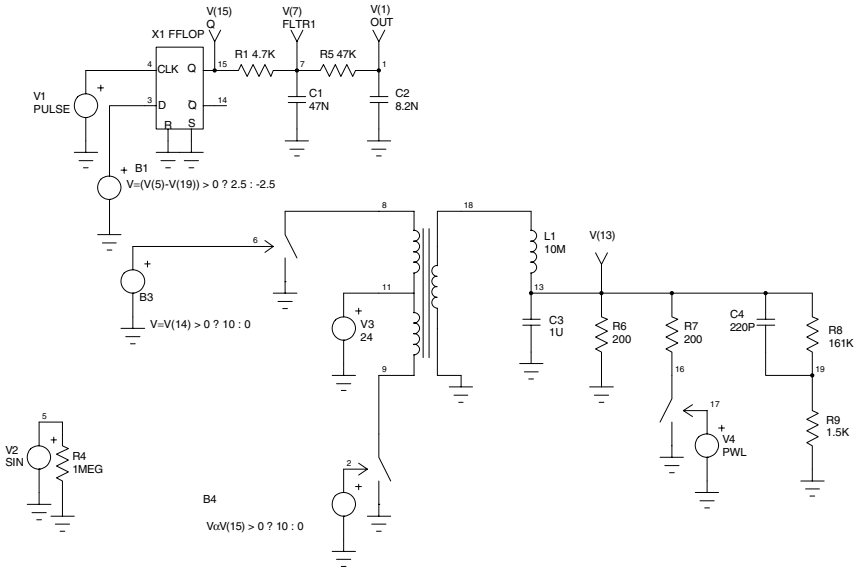


Figure 7.9 Output of the push-pull converter using 24- and 28-V inputs.




```
UPS2: USE THE SINE REFERENCE AND COMPARE IT WITH VOUT
.PROBE
.TRAN 9.766U 10M UIC
.FOUR 400HZ V(13)
* V(1)=OUT
* V(15)=Q
* V(7)=FLTR1
.PRINT TRAN V(1) V(15) V(7) V(13)
R1 15 7 4.7K
C1 7 0 47N IC=0
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
V2 5 0 SIN 0 1.5 400
R4 5 0 1MEG
R5 7 1 47K
C2 1 0 8.2N IC=0
EB1 6 0 Value={ IF ( (V(5)-V(19)) > 0 , 2.5 , -2.5 ) }
X2 18 0 8 11 10 XFMR-TAP Params: RATIO=.1
X4 10 0 2 SWITCH
V3 11 0 24
L1 18 13 10M
C3 13 0 1U
R6 13 0 200
X3 8 0 12 SWITCH
EB3 12 0 Value={ IF ( V(14) > 0 , 10 , 0 ) }
EB4 2 0 Value={ IF ( V(15) > 0 , 10 , 0 ) }
R7 13 16 200
X5 16 0 17 SWITCH
V4 17 0 PWL 0 10 3.125M 10 3.15M 0
R8 13 19 161K
R9 19 0 1.5K
C4 13 19 220P
X1 4 6 0 0 14 15 FFLOPZero
.END
```

Figure 7.10 Schematic and netlist for the push-pull converter with improved regulation. B1 compares the sine-wave reference with the output voltage.

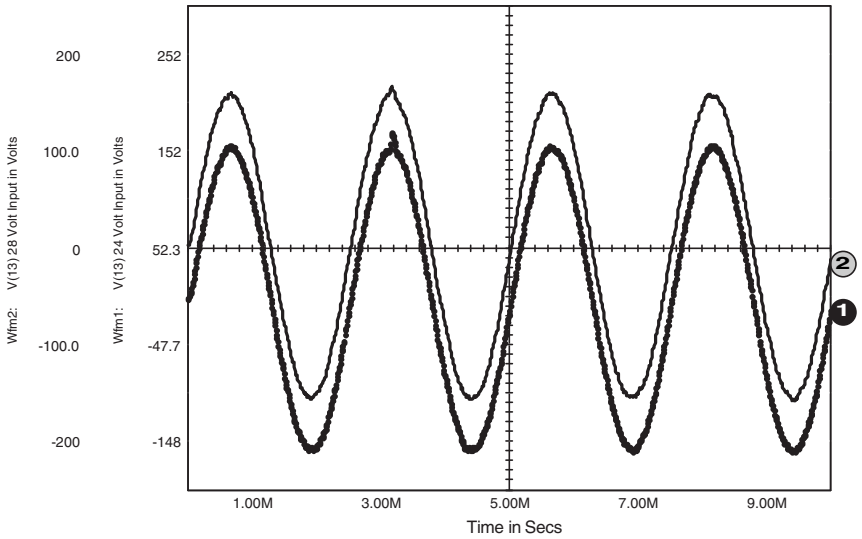


Figure 7.11 Output of the improved push-pull converter.

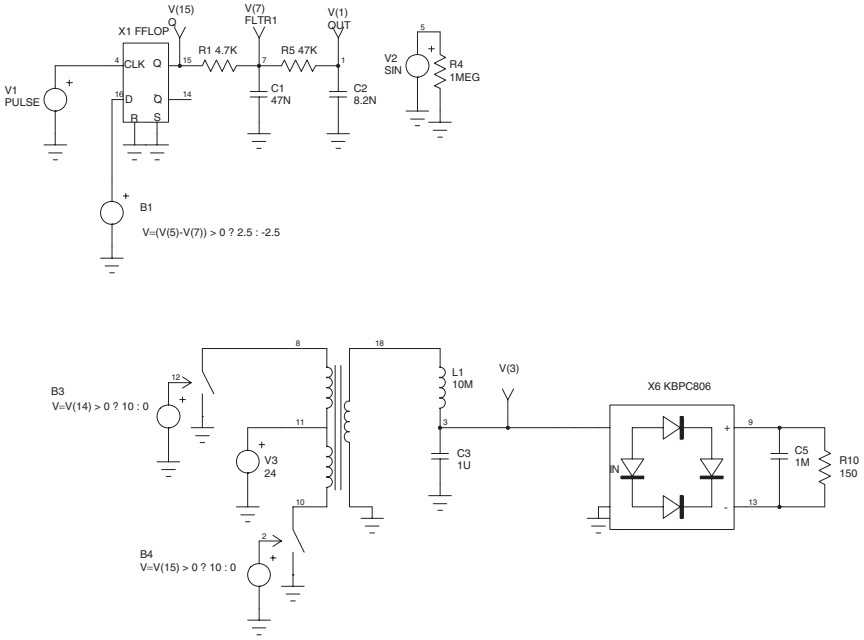
and compares it with the actual output voltage, V(19). This approach uses the same algorithm that we used to create the reference which stabilized the output voltage. The result is greatly improved regulation with respect to both line and load changes.

The output voltage is now sensed by R8, R9, and C4. The purpose of C4 is to cancel one of the two poles of the output filter. The comparator, EB1, now compares the sine-wave reference to the output of the power stage rather than the output of the flip-flop (V(7)), as in Fig. 7.7. The results are shown in Fig. 7.11.

Note the drastic improvement in the dynamic transient response. The waveform is no longer highly distorted as a result of the transient. Also note that the spike that was created by the load switching is much smaller and recovers more quickly. The results also demonstrate the improved regulation against line changes. As in the previous circuit, the input voltage was simulated at 24 and 28 V. The improved circuit is useful in applications in which the output regulation and/or waveform are important.

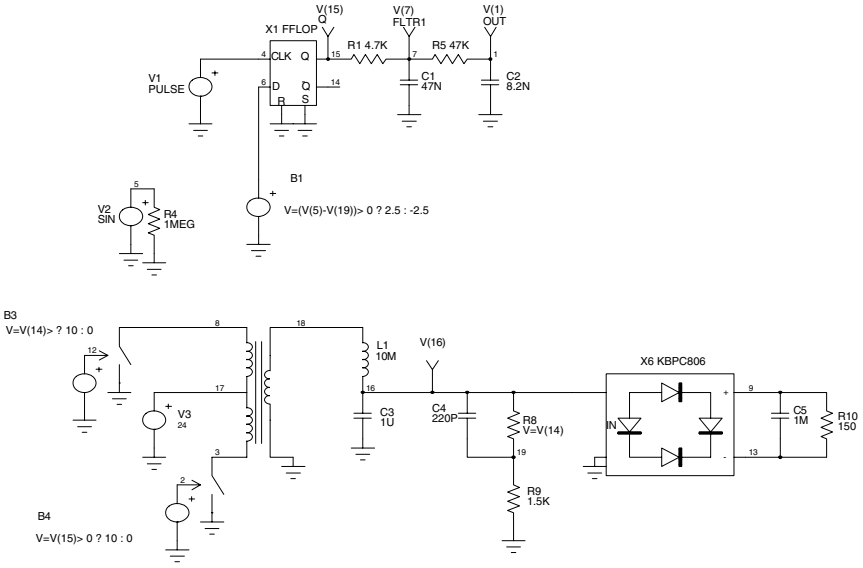
Powering Nonlinear Loads

One of the greatest problems with DC-to-AC converters is the nonlinear load. The nonlinear load is often a rectifier circuit, which may be found in most power supplies. A typical example is the power supply that is used in a personal computer. If the DC-to-AC converter is used as a UPS for a personal computer, it is likely that the power supply input circuit will contain a simple rectifier and filter. The circuits in Fig. 7.12




```
UPS3: TO POWER A NON-LINEAR LOAD
.TRAN 9.766U 10M UIC
.FOUR 400HZ V(13)
.PROBE
* V(1)=OUT
* V(15)=Q
* V(7)=FLTR1
.PRINT TRAN V(1) V(15) V(7) V(3)
R1 15 7 4.7K
C1 7 0 47N IC=0
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
V2 5 0 SIN 0 1.5 400
R4 5 0 1MEG
R5 7 1 47K
C2 1 0 8.2N IC=0
EB1 6 0 Value={ IF ( (V(5)-V(7)) > 0 , 2.5 , -2.5 ) }
X2 18 0 8 11 10 XFMR-TAP Params: RATIO=.1
X4 10 0 2 SWITCH
V3 11 0 24
L1 18 3 10M
C3 3 0 1U
X3 8 0 12 SWITCH
EB3 12 0 Value={ IF ( V(14) > 0 , 10 , 0 ) }
EB4 2 0 Value={ IF ( V(15) > 0 , 10 , 0 ) }
X6 3 0 9 13 KBPC806
C5 9 13 1M IC=140
R10 9 13 150
X1 4 6 0 0 14 15 FFLOPZero
.END
```

Figure 7.12a Schematic and netlist of the push-pull converter driving a nonlinear load. Original configuration similar to Fig. 7.7.




```
UPS4: TO POWER A NON-LINEAR LOAD
.TRAN 9.766U 10M UIC
.FOUR 400HZ V(13)
.PROBE
* V(1)=OUT
* V(15)=Q
* V(7)=FLTR1
.PRINT TRAN V(1) V(15) V(7) V(3)
R1 15 7 4.7K
C1 7 0 47N IC=0
V1 4 0 PULSE -2.5 2.5 10N 10N 10N 5U 9.766U
V2 5 0 SIN 0 1.5 400
R4 5 0 1MEG
R5 7 1 47K
C2 1 0 8.2N IC=0
EB1 6 0 Value={ IF ( (V(5)-V(19)) > 0 , 2.5 , -2.5 ) }
X2 18 0 8 11 10 XFMR-TAP Params: RATIO=.1
X4 10 0 2 SWITCH
V3 11 0 24
L1 18 3 10M
C3 3 0 1U
X3 8 0 12 SWITCH
EB3 12 0 Value={ IF ( V(14) > 0 , 10 , 0 ) }
EB4 2 0 Value={ IF ( V(15) > 0 , 10 , 0 ) }
R8 3 19 161K
R9 19 0 1.5K
C4 3 19 220P
X6 3 0 9 13 KBPC806
C5 9 13 1M IC=140
R10 9 13 150
X1 4 6 0 0 14 15 FFLOPZero
.END
```

Figure 7.12b Schematic and netlist of the push-pull converter driving a nonlinear load. Improved configuration similar to Fig. 7.10.

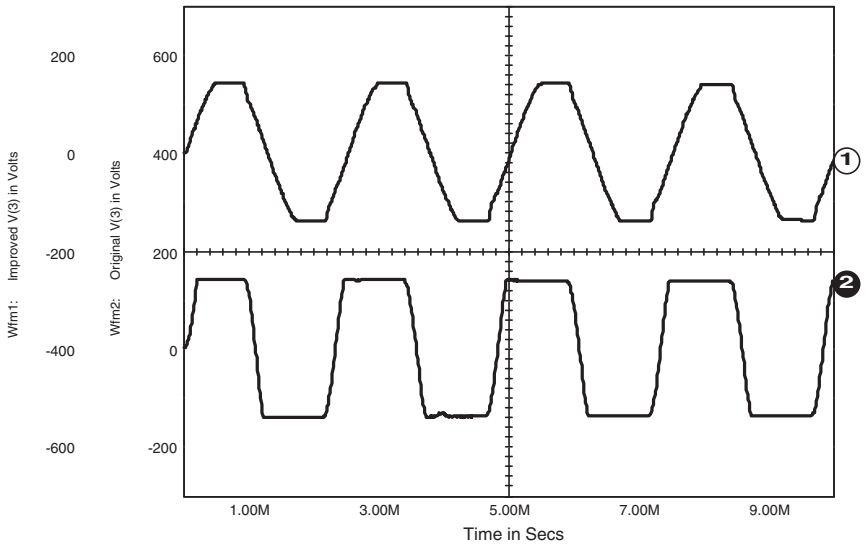


Figure 7.13 Simulation results of the circuits in Figs. 7.12b (waveform 1) and 7.12a (waveform 2).

demonstrate the behavior of both the original circuit (Fig. 7.7) and the improved circuit (Fig. 7.10) when they are used to power a nonlinear load.

The upper trace shows the result of our improved circuit, while the lower trace shows the results of the original circuit. Both of the simulations resulted in the same peak output amplitude, which has been reduced to 142 V as a result of the high current demand by the nonlinear load. The major difference between the two circuits is the output wave shape. The improved circuit maintains the sinusoidal wave shape throughout the waveform, with the exception of the flattened peaks. The original circuit produces a square wave as a result of the unloaded condition that occurs throughout the waveform except at the peaks. The end result is a major difference in the RMS amplitude (108 and 127 V, respectively). The increased RMS voltage of the original circuit can easily cause the saturation of transformers within the load. The increased RMS voltage may also stress other components which are sensitive to the RMS content of the load.

Three-Phase Sine Reference

The circuit example in Fig. 7.14 demonstrates a three-phase sine-wave reference using the mixed-mode simulation techniques. A six-stage shift register is used to generate three quasi-square waves that are exactly

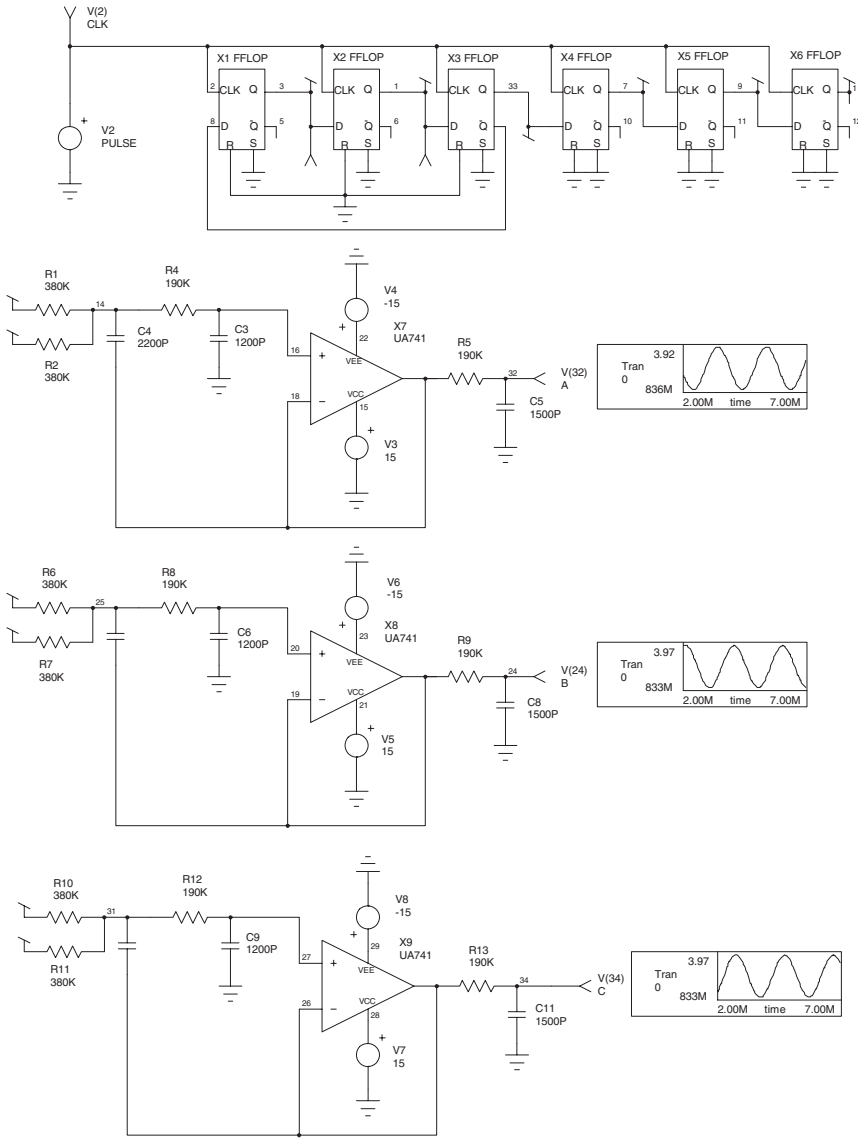


Figure 7.14 Schematic and netlist for a three-phase sine-wave reference.

```
3PHASE: A THREE PHASE SINE WAVE
.PROBE
.TRAN 1U 7M ; UIC
.FOUR 500HZ V(32)
* V(3)=Q1
* V(1)=Q2
* V(2)=CLK
* V(32)=A
* V(24)=B
* V(30)=C
.PRINT TRAN V(3) V(1) V(2) V(32)
.PRINT TRAN V(24) V(30) V(33)
V4 22 0 DC=-15
X6 2 9 0 0 12 13 FFLOPFive
V5 21 0 DC=15
C3 16 0 1200P
X7 18 16 18 15 22 UA741
R1 3 14 380K
V6 23 0 DC=-15
X8 19 20 19 21 23 UA741
C4 14 18 2200P
R2 1 14 380K
V7 28 0 DC=15
X9 26 27 26 28 29 UA741
C5 32 0 1500P
V8 29 0 DC=-15
C6 20 0 1200P
R4 14 16 190K
C7 25 19 2200P
R5 18 32 190K
C8 24 0 1500P
R6 33 25 380K
C9 27 0 1200P
R7 7 25 380K
R8 25 20 190K
R9 19 24 190K
X1 2 8 0 0 5 3 FFLOPFive
R10 9 31 380K
X2 2 3 0 0 6 1 FFLOPFive
R11 13 31 380K
X3 2 1 0 0 8 33 FFLOPFive
C10 31 26 2200P
R12 31 27 190K
X4 2 33 0 0 10 7 FFLOPFive
V2 2 0 PULSE 0 5 100N 10N 10N 100U 333.33U
C11 30 0 1500P
R13 26 30 190K
V3 15 0 DC=15
X5 2 7 0 0 11 9 FFLOPFive
.END
```

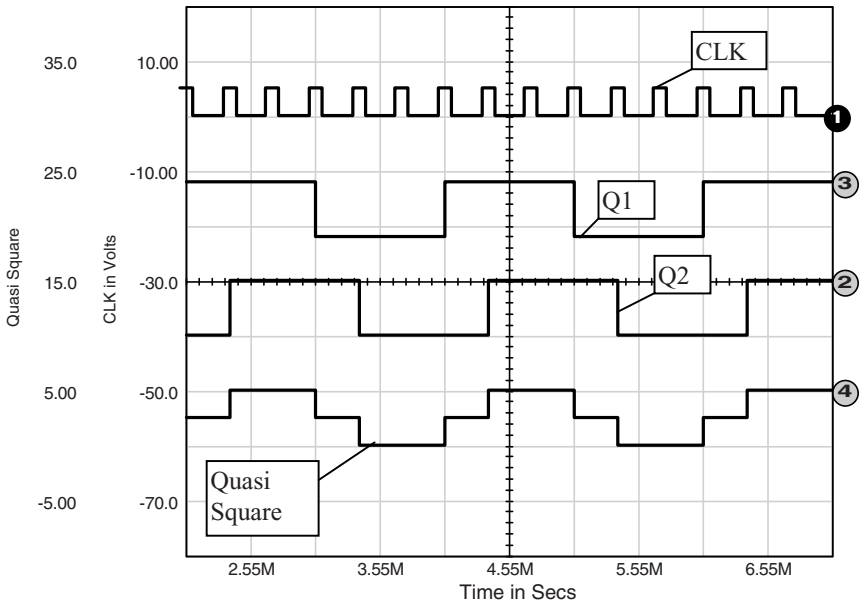
Figure 7.14 (*Continued*)

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(32)

DC COMPONENT = 2.475499E+00

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	5.000E+02	1.430E+00	1.000E+00	2.003E+01	0.000E+00
2	1.000E+03	1.102E-03	7.704E-04	8.055E+01	4.049E+01
3	1.500E+03	3.476E-04	2.430E-04	1.483E+02	8.822E+01
4	2.000E+03	8.351E-04	5.839E-04	-9.185E+01	-1.720E+02
5	2.500E+03	4.363E-03	3.051E-03	-3.703E+00	-1.038E+02
6	3.000E+03	4.820E-04	3.370E-04	1.227E+02	2.568E+00
7	3.500E+03	4.187E-03	2.928E-03	-7.488E+01	-2.151E+02
8	4.000E+03	7.734E-04	5.408E-04	8.985E+01	-7.038E+01
9	4.500E+03	3.807E-04	2.662E-04	1.590E+02	-2.129E+01

TOTAL HARMONIC DISTORTION = 4.398894E-01 PERCENT



Digital Signals CLK, Square Wave, Quasi Square

Figure 7.15 Fourier result (top) and digital signals (bottom) showing a single phase.

120°apart. Each quasi-square wave has a conduction angle of 120°. The 120° quasi-square waveform has the advantage of having no third harmonic content. Each quasi-square wave is filtered by a second-order active low-pass filter. The quasi-square waves are created by averaging two square waves that are phase shifted by 60°.

The Fourier results from the output file are shown in Fig. 7.15. Note that as a result of the quasi-square waveform, the first significant harmonic is the fifth harmonic. The sine-wave output distortion can be

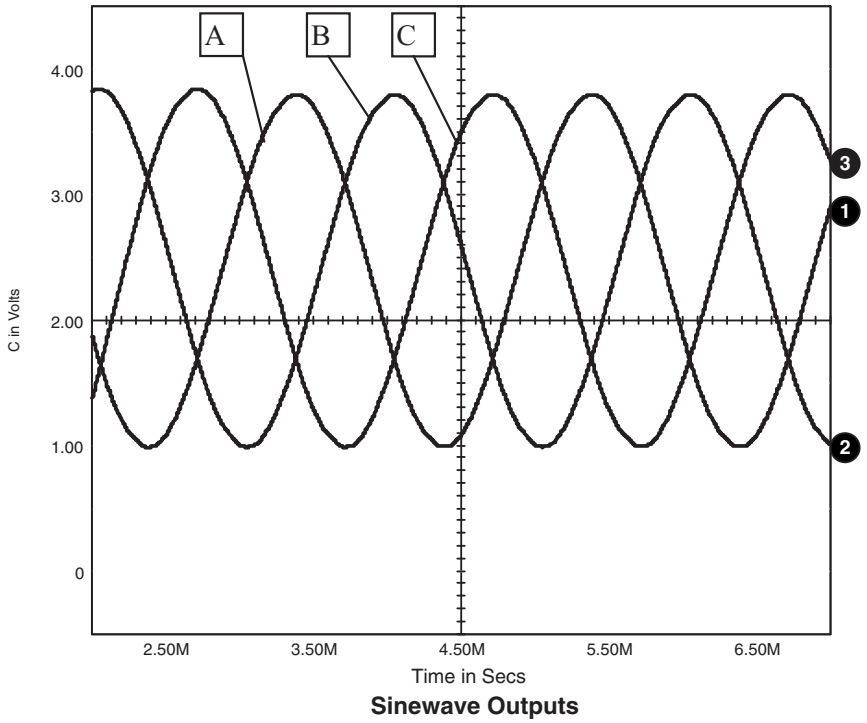


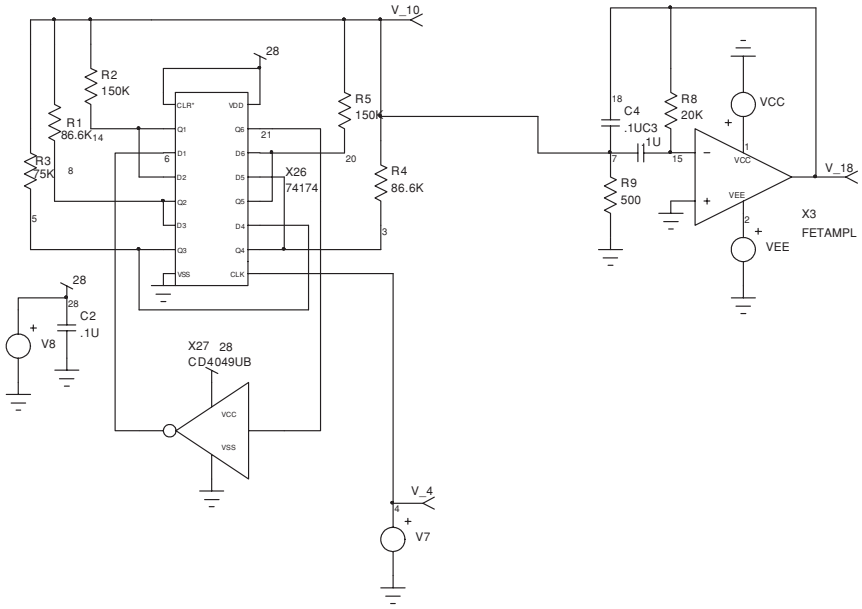
Figure 7.16 Results for the three-phase sine-wave reference circuit in Fig. 7.14.

further reduced by using a higher order active filter (which will reduce the corner frequency of the existing filters) or replacing the quasi-square waveform with a more sophisticated waveform in order to eliminate several additional harmonics.

Care must be taken in the placement of the filters, because component tolerances can easily alter the angles between phases. A Monte Carlo simulation can be performed to analyze the effect of component tolerances on the phase angles (and amplitudes) of the sine-wave outputs. The resulting filtered sine-wave output is shown in Fig. 7.16.

An improved stepped waveform

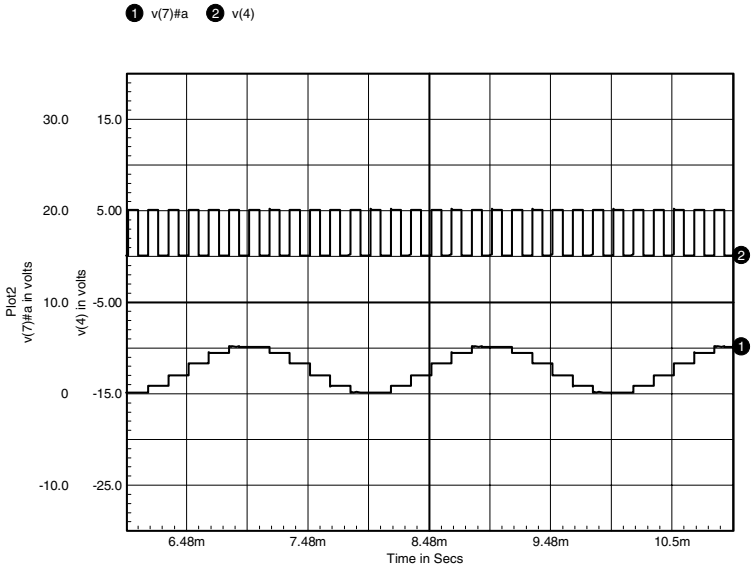
The circuit in Fig. 7.17 demonstrates another stepped waveform. Although the 120° conduction angle of the circuit in Fig. 7.14 eliminated the third harmonic, this waveform can eliminate all harmonics up to the eleventh harmonic. Resistors R1 through R5 form a "cheap and dirty" D/A converter, while the amplifier circuit is configured as a bandpass filter. This circuit can be used as a reference circuit but is also widely used in power stages. When used in a power stage, the stepped waveform is generally created by summing the outputs of several transformers, each




```
STAIR SINE.CIR
.TRAN 1u 10m 5m UIC
.FOUR 500 v(18)
.PROBE
C2 28 0 .1U
VCC 1 0 DC=15
VEE 2 0 DC=-15
C3 15 7 .1U
R1 7 8 86.6K
C4 7 18 .1U
R2 7 14 150K
V7 4 0 PULSE 0 5 0 .1U .1U 83.33U 166.66U
R3 7 5 75K
V8 28 0 PULSE 0 5
R4 7 3 86.6K
R5 7 20 150K
X26 28 14 6 14 8 8 5 0 4 3 5 20 3 20 21 28 74174
R8 15 18 20K
X27 21 6 28 0 CD4049UB
R9 7 0 500
X3 15 0 18 1 2 FETAMPL Params: GAIN=1k FT=1meg VOS=1m
.END
```

Figure 7.17 Schematic and netlist for an improved stepped waveform.

of which is driven by a separate phase-shifted power converter. The resulting stepped waveform is shown in Fig. 7.18. The simulated result is the top waveform while the measured result is the bottom waveform. The filtered sine-wave output is shown in Fig. 7.19.



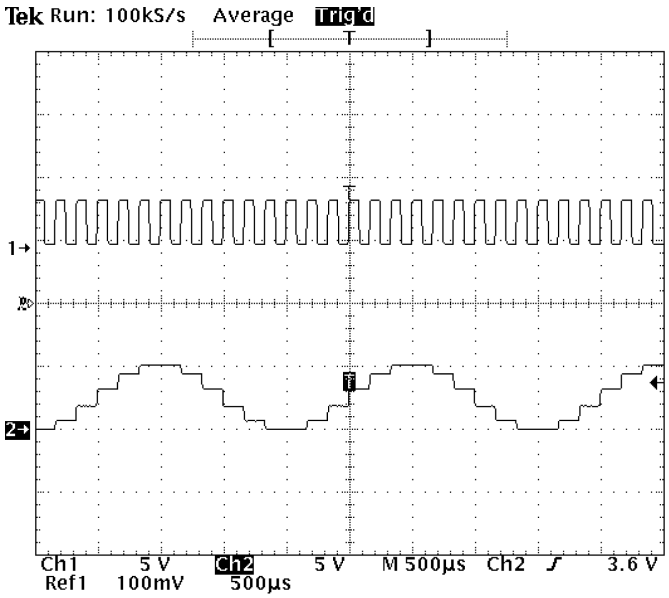


Figure 7.18 Measured and simulated unfiltered output (node 7 with filter disconnected).

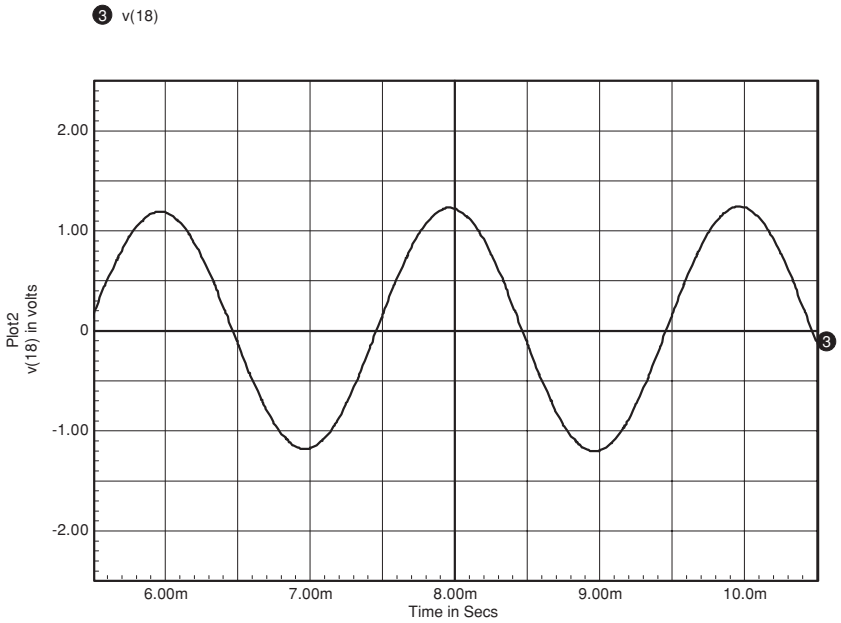
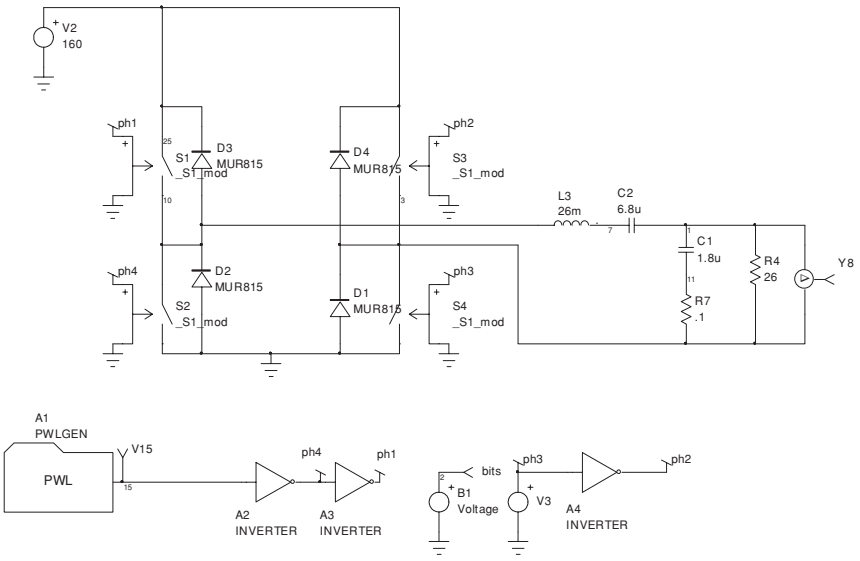


Figure 7.19 Filtered output (node 7 with filter connected).

Harmonic Neutralized Full-Bridge Inverter

There are many other configurations and bit patterns that can greatly reduce the harmonic content of a power train. The schematic in Fig. 7.20 demonstrates a full-wave half-bridge circuit that minimizes the harmonic content up to the ninth harmonic. In this circuit an XSPICE PWLGEN model is used to simulate the contents of a ROM. The PWLGEN model reads a text file that is a continuous PWL statement. The model allows the waveform to be repeating (see Fig. 7.21). Although not an advantage in this case, one of the benefits of the PWLGEN model is that an arbitrary waveform can be generated, whereas the state machine model in Fig. 7.5 is limited to a digital value (1 or 0). PSpice supports a repeating PWL statement with points stored in a file, e.g., "V3 5 0 PWL REPEAT FOREVER FILE DATA1.TAB ENDREPEAT" as seen in the netlist. The output switches, which are generally either MOSFETs or IGBTs, are simulated using switches in order to simplify and speed up the simulation. A measurement was made on a prototype of the full-bridge inverter for comparison with the simulated results. A spectrum analysis plot was also made from the prototype, and the result is shown in Fig. 7.22.




```
64 Sample Sine Inverter 2.cir – PSPICE Netlist
.TRAN .5u 30m 10m 1u
.OPTIONS ITL1=500 ITL4=500 GMIN=1N RELTOL=.01
.FOUR 400 v(1,3)
.PROBE
S1 25 10 ph1 0 _S1_mod
.MODEL _S1_mod VSWITCH VT=3 VH=.1 RON=.02 ROFF=1meg
S2 10 0 ph4 0 _S1_mod
S3 25 3 ph2 0 _S1_mod
S4 3 0 ph3 0 _S1_mod
X2 15 ph4 INVD
X3 ph4 ph1 INVD
X4 ph3 ph2 INVD
Rph1 ph1 0 1G
Rph4 ph4 0 1G
Rph2 ph2 0 1G
L3 10 7 26m
C1 1 11 1.8u
D1 0 3 MUR815
R4 1 3 26
VPWL 15 0 PWL REPEAT FOREVER FILE 64s.txt ENDREPEAT
V2 25 0 DC=160
R7 11 3 .1
D2 0 10 MUR815
D3 10 25 MUR815
D4 3 25 MUR815
EB1 BITS 0 Value={ V(10,3) }
RBITS BITS 0 1G
V3 ph3 0 PULSE 0 5 0 .1u .1u 1.25m 2.5m
C2 7 1 6.8u
.END
```

Figure 7.20 Harmonic neutralized full-bridge inverter schematic and netlist (XSPICE and PSpice versions).

```
64 Sample Sine Inverter 2.cir – XSPICE Netlist
.TRAN .5u 30m 10m 10u UIC
.FOUR 400 v(1,3)
.OPTIONS abstol=1E-8 itl4=1000 method=TRAP
.OPTIONS gmin=10n reltol=0.005
.PRINT TRAN V15
.PRINT TRAN bits
.PRINT TRAN Y8
S1 25 10 ph1 0 _S1_mod
.MODEL _S1_mod SW VT=3 VH=.1 RON=.02 ROFF=1meg
S2 10 0 ph4 0 _S1_mod
S3 25 3 ph2 0 _S1_mod
S4 3 0 ph3 0 _S1_mod
A2 15_Din ph4_Dout INVERTERA2
A3 ph4_Din ph1_Dout INVERTERA3
A4 ph3_Din ph2_Dout INVERTERA4
L3 10 7 26m
C1 1 11 1.8u
D1 0 3 MUR815
R4 1 3 26
A1 15 PWLGENA1
.MODEL PWLGENA1 vsrc_pwl( input_file=64s.txt repeat=TRUE)
V2 25 0 DC=160
R7 11 3 .1
D2 0 10 MUR815
D3 10 25 MUR815
D4 3 25 MUR815
B1 2 0 V=v(10,3)
V3 ph3 0 PULSE 0 5 0 .1u .1u 1.25m 2.5m
C2 7 1 6.8u
.END
```

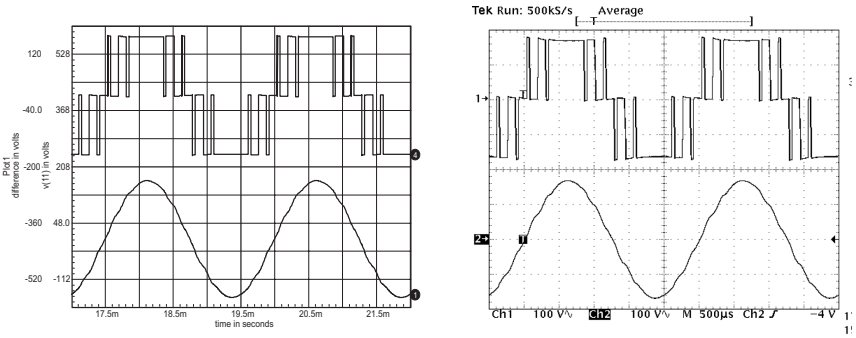
Figure 7.20 (*Continued*)

Harmonic Neutralized Half-Bridge Inverter

In a similar fashion, many of the harmonics can be eliminated in a half-bridge configuration (see Fig. 7.23). Using a 128-bit digital pattern, most of the third, fifth, and seventh harmonics can be minimized (see Fig. 7.24). The ninth harmonic, however, is substantially larger than that of the full-bridge configuration or even larger than a square wave. Fortunately, the ninth harmonic is easily minimized by the output filter, though the result is not as good as that of the full-bridge circuit. Higher bit counts could further reduce the harmonic content.

The half-bridge configuration is often used in three-phase transformerless conversions, where a full-bridge circuit is not possible. The half-bridge configuration is also generally much less expensive because it uses half the number of MOSFETs and drivers.

The output voltage is generally regulated by controlling the DC input that feeds the half-bridge circuit.



FOURIER COMPONENTS OF TRANSIENT RESPONSE V(1,3)

DC COMPONENT = -1.955657E-03

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	4.000E+02	1.620E+02	1.000E+00	-6.901E+00	0.000E+00
2	8.000E+02	9.838E-02	6.072E-04	-2.742E+01	-1.362E+01
3	1.200E+03	2.878E-01	1.776E-03	1.033E+02	1.240E+02
4	1.600E+03	7.250E-02	4.475E-04	-1.498E+02	-1.222E+02
5	2.000E+03	1.002E-01	6.185E-04	6.752E+01	1.020E+02
6	2.400E+03	4.970E-02	3.068E-04	1.647E+02	2.061E+02
7	2.800E+03	6.924E-02	4.274E-04	8.369E+01	1.320E+02
8	3.200E+03	2.986E-02	1.843E-04	1.192E+02	1.744E+02
9	3.600E+03	1.042E-01	6.434E-04	-6.238E+01	-2.784E-01

TOTAL HARMONIC DISTORTION = 2.197904E-01 PERCENT

Figure 7.21 Fourier and graphical result of the full-bridge inverter in Fig. 7.20.

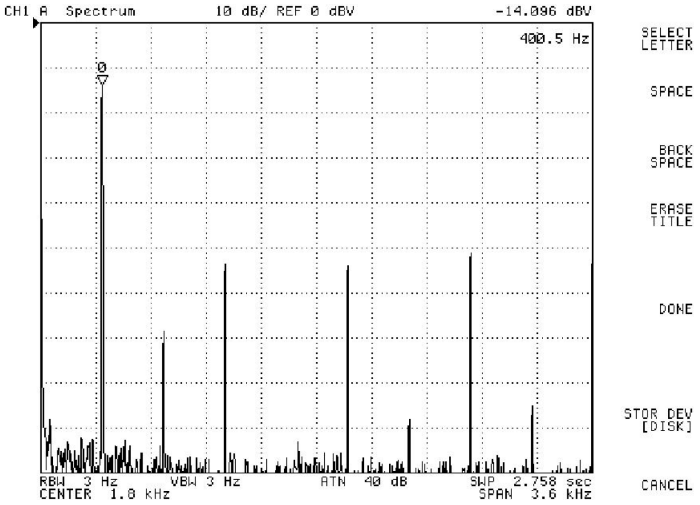
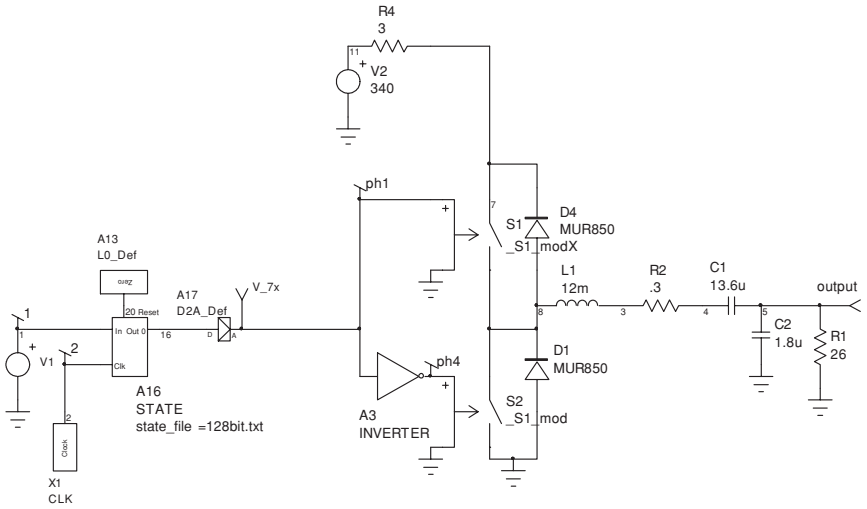
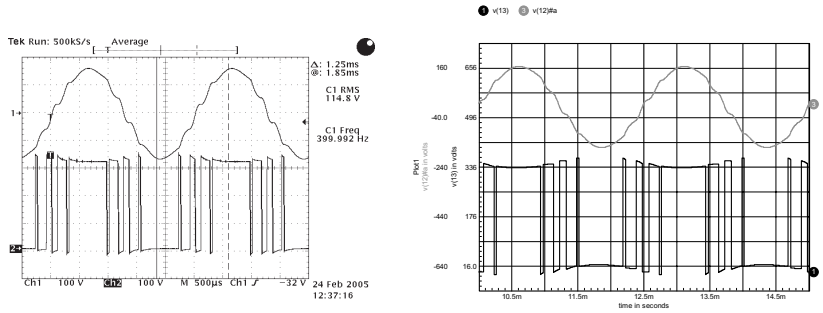


Figure 7.22 Spectrum analysis result of the full-bridge inverter in Fig. 7.20.




```
128 Bit Half Bridge
.TRAN .5u 15m 10m 1u UIC
.FOUR 400 v(5) v(8)
.OPTIONS abstol=1E-8 itl4=1000 method=TRAP
.OPTIONS gmin=1E-9 icstep=40
.PRINT TRAN output
.PRINT TRAN V_7x
L1 8 4 25m
C1 4 5 6.8u
C2 5 0 1.8u
R1 5 0 26
X1 2 CLK Params: FREQ=51.2k DUTY=50
S1 7 8 ph1 0 _S1_mod
.MODEL _S1_mod SW VT=3 VH=.1 RON=.02 ROFF=1meg
V1 1 0 DC=0
S2 8 0 ph4 0 _S1_mod
V2 11 0 DC=320
R4 11 7 3
D2 0 8 MUR850
D3 8 7 MUR850
A3 ph1_Din ph4_Dout INVERTERA1
A13 20 L0_DefA5
A17 [ 16 ] [ ph1 ] D2A_DefA8
A16 [ 1_Din ] 2 20 [ 16 ] STATEA20
.END
```

Figure 7.23 Harmonic neutralized half-bridge inverter schematic and netlist.



Fourier analysis for v(5):

No. Harmonics: 10, THD: 0.929872 %, Gridsize: 200, Interpolation Degree:1

Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0	0.000802049	0	0	0
1	400	69.0061	-6.8934	1	0
2	800	0.00413678	17.1877	5.99481e-005	24.0811
3	1200	0.152741	86.0766	0.00221344	92.97
4	1600	0.00195197	46.8701	2.8287e-005	53.7635
5	2000	0.0586701	76.1783	0.000850217	83.0717
6	2400	0.0015346	64.6708	2.22386e-005	71.5643
7	2800	0.0260316	-108.27	0.000377237	-101.38
8	3200	0.00110158	79.6249	1.59635e-005	86.5184
9	3600	0.61989	69.068	0.00898312	75.9614

Figure 7.24 Fourier and graphical results of the full-bridge inverter in Fig. 7.23.

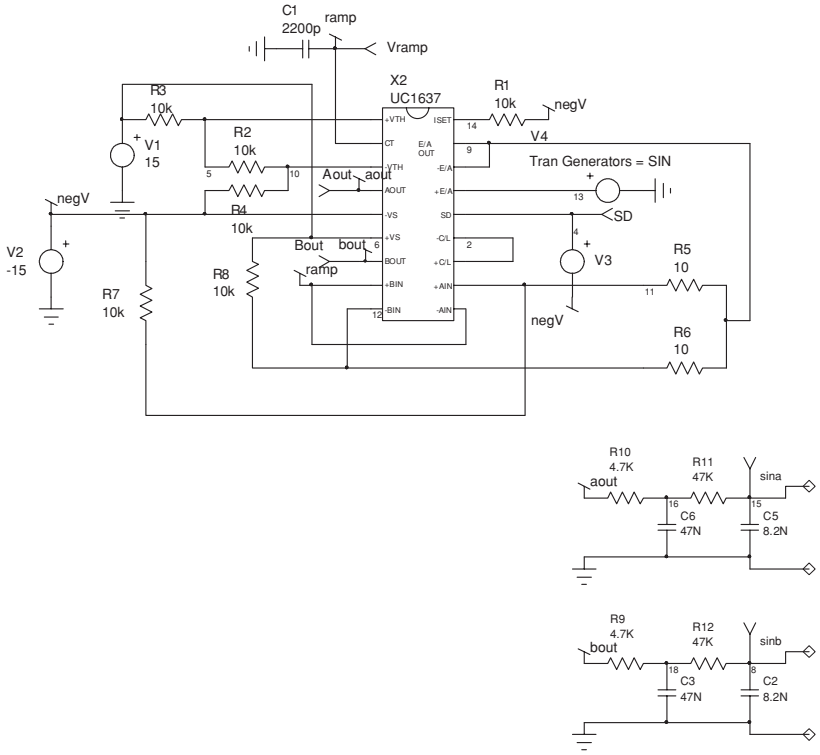


Figure 7.25 Fourier and graphical results of the full-bridge inverter.

```
PWM Inverter.cir
.TRAN .5u 15m 5m 1u UIC
.FOUR 400 v(15) v(16) v(15,bout)
.PROBE
* V(4) SD
* V(8) sinb
* V(15) sina
C2 8 0 8.2N
R1 14 negV 10k
C1 0 ramp 2200p
V1 6 0 DC=15
V2 negV 0 DC=-15
R2 10 5 10k
R3 6 5 10k
R4 10 negV 10k
R5 11 9 10
R6 12 9 10
R7 11 negV 10k
R8 6 12 10k
V4 13 0 SIN 0 4.5 400
V3 4 negV PULSE 0 3m 150u
X2 5 ramp 10 aout negV 6 bout ramp 12 ramp 11 2 2 4 13 9 9 14 UC1637
R9 bout 18 4.7K
R12 18 8 47K
C3 18 0 47N
C5 15 0 8.2N
R10 aout 16 4.7K
R11 16 15 47K
C6 16 0 47N
.END
```

Figure 7.25 (*Continued*)

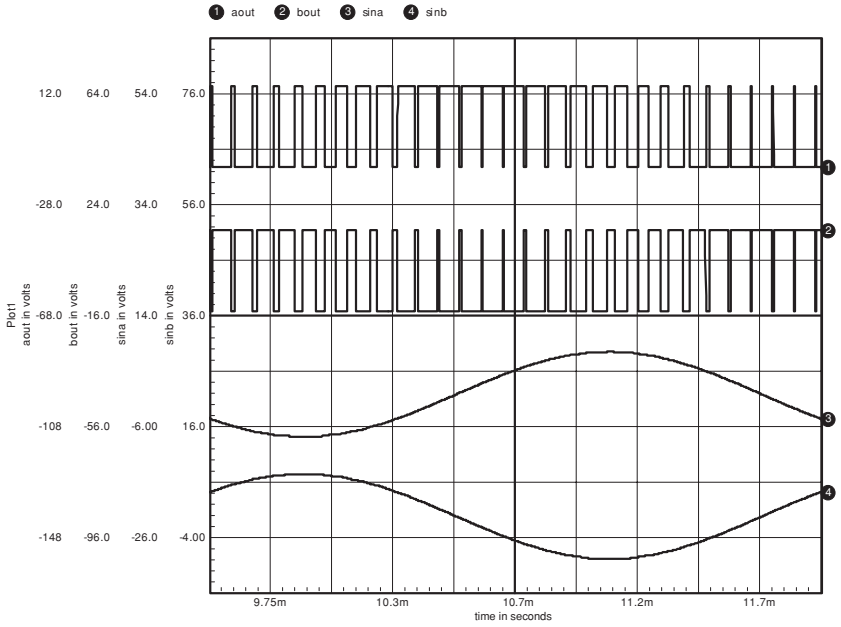


Figure 7.26 PWM inverter simulation results.

PWM Inverter

A PWM inverter compares a control voltage with a triangle waveform, which is at the switching frequency. The switching frequency is much higher than the fundamental output frequency. Integrated circuit devices such as the UC3637 offer all the functions required, including a variable dead time control to avoid overlapping of the upper and lower switches. This controller is often used in motor control applications, but it can also be used for audio switching amplifiers, ultrasonics, or UPS applications. A simple example is shown in Fig. 7.25, with the simulation results shown in Fig. 7.26. A very low switching frequency is used in this example in order to provide a visual representation of the switched output. A simple two-stage RC filter is used to filter the output. In a typical application, the output filter would be an LC filter and UC3637 would be used to drive a power stage.

PWM amplifiers are also available as hybrid devices and more recently as monolithic integrated circuit devices. In these devices, the entire control circuit and output stage are contained in a very small package. A good example of this type of device is the SA12 device, which is manufactured by Apex. Apex also provides SPICE model support for these devices.