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Preface

This book presents a study of analog electronics as a stand-alone course or as a course to be augmented by one of the many complete undergraduate textbooks on the subject. Theory and closely coupled laboratory projects, which are based entirely on computer-based data acquisition, follow in a sequential format. All analytical device characterization formulations are based exactly on SPICE.

In addition to traditional curricula in electrical engineering and electronics technology, the course is suitable for the practicing engineer in industry. For the engineer with a general undergraduate electronics background, for example, the course of study can provide an upgrade in basic analog electronics. Under these or similar circumstances, it can be taken as self-paced or with minimum supervision.

Two course sequences are possible, depending on the emphasis desired:
• For a course that stresses MOSFET characterization and circuits, beginning with Unit 1 and following the sequence is recommended. A brief review of relevant circuit analysis and the most rudimentary basics of electronics are presented initially, with associated projects. The projects include an introduction to LabVIEW programming along with the measurements of basic circuits. The programming aspects are directly relevant to the thrust of the course; they emphasize the measurement of analog electronics circuits. The student is thus provided with a basic understanding of LabVIEW concepts used throughout the projects.

• If, on the other hand, interest is directed more toward LabVIEW and computer data acquisition, device characterization, and circuit simulation, the appropriate beginning sequence is Units A through C. The associated projects are Project A, Projects B, Project C1, and Project C2. Project A is a programming and measurement exercise that emphasizes and explores the use of LabVIEW DAQ software, the discrete nature of analog-to-digital and digital-to-analog conversions, LabVIEW-based voltmeters with autoranging, ac voltmeters, and simultaneous sending and receiving of waveforms initiated with a function generator. This is followed with projects on transistors and transistor circuits, which are based on the bipolar junction transistor. Although the BJT is losing ground as the most important transistor in electronics (compared to the MOSFET), its inherently more complex behavior provides for a rich array of circuit simulation formulations and design challenges. The projects include the mix of NPN and PNP devices in a single amplifier. The transistors recommended are the complementary pair NTE 186 (2N6288) and NTE 187 (2N62xx). The transistors are rated at 3 A and are therefore almost indestructible. At the much lower current levels of the projects, device heating is negligible, which is important, as all measurements assume that the circuit is at room temperature. Also, highlevel model effects are avoided, whereas low-level effects abound.

With both approaches, all the measurement LabVIEW programs are provided. Many of the extraordinary features provided by LabVIEW are included in the programs. The programs therefore may serve additionally as a tutorial in advanced aspects of LabVIEW. The basics of operational amplifiers and their applications are treated in two units and two projects.

The book format consists of one or more units of background material for each laboratory project. A given set of theoretical units and the associated project have a related Mathcad problems file (Problemxx.mcd) and Mathcad exercise file (ExerciseXX.mcd), relating to the theory and project, respectively. The files are also in a pdf format (ProblemXX.pdf, ExerciseXX.pdf). A Mathcad file (ProjectXX.mcd) for evaluating the results of the projects is included with each project. Accompanying each Mathcad project file are SPICE simulator files based on PSPICE. The SPICE models for the simulations use, in each case, the parameters for the devices obtained in laboratory projects. Since the Mathcad projects use the exact SPICE formulations, the results from Mathcad and SPICE are identical in the case of the use of basic simulation levels.
Samples of all of the projects have been completed and are included. These provide for either demonstrations or simulated results without actually running the programs with circuits. The measured data are stored in LabVIEW graphics and can be extracted to obtain data files in the same manner as actually making the measurements. In some cases, the simultaneous taking of data, plotting and curve fitting is simulated. Units 13 and 14 are theoretical only but each has Mathcad problems on the topic of these respective units.

Special features of the lab experience are as follows:

- The lab projects are based entirely on computer data acquisition using LabVIEW and a National Instruments data acquisition card (DAQ) in the computer for interfacing with the circuit board.
- Each device category has an associated project for evaluating SPICE parameters in which device model parameters are obtained. Subsequent amplifier projects use the parameters in performance assessment.
- No external instrumentation is required. The function generator, voltmeters, and oscilloscopes are virtual and provided by LabVIEW and a DAQ card in the computer. The projects on the current-mirror load common-source amplifier and the operational amplifier require an external power supply.
- Circuits are constructed on a special circuit board. The board is connected to the computer DAQ card through a National Instruments shielded 68-pin cable. The circuit board allows expedient, error-free construction of the circuits, as connector strips for the respective output and input channels and ground are available directly on the board.

Topics included in this course treat many of the most relevant aspects of basic modern analog electronics without straying into peripheral areas. The course essentially streamlines the study of analog electronics. There is not a unit on, for example, feedback per se, but most basic types of feedback are addressed at some point. The role that the device plays in frequency response is omitted. This is consistent with the fact that to a large extent, the intention is that theory and measurements can be connected.

Students of electrical engineering or electronics engineering of today have a vast array of subjects to attempt to master; it is not reasonable to expect them to labor through a classical extensive study of the subject of analog electronics, although some basic knowledge should be required. Specialization can come at a later stage, if desired.

As mentioned, many LabVIEW features are utilized in the projects. To some extent, the goal of demonstrating the extensive array of the capabilities of LabVIEW influences the design of the various projects. This includes sending voltages (including waveforms), receiving voltages (including autoscaling), scanning, graphics, reading data files, writing data files, computations such as extraction of harmonic content of a signal, assembling data in a composite form, along with a host of array manipulation processes and data curve fitting.

References
CMOS analog circuits including applications (advanced):


Extensive coverage of analog circuits, which includes a comprehensive discussion of feedback and frequency response (advanced):


CMOS analog circuits (with some BJT circuits) with extensive coverage of applications (advanced):


Presentation of the physical and empirical association between semiconductor devices and their models, MOSFETs and BJTs:


General textbook on electronics (basic):


Physical description of semiconductor devices:


General textbook on electronics (basic):


General treatment of analog circuits including applications (basic to advanced):


Hardware and Software Requirements
Circuit connections to the DAQ require a cable and a facility for connecting to individual pins. An efficient system is based on a National Instruments Connector Block (CB-68LP) and a basic circuit board as shown here.

Connections to the circuit board from the connector block are made one time. The two resistors of the circuit are connected to output channels 0 and 1, respectively. Thus, for example, Chan0_out, as noted, is dedicated to the top strip on the circuit board. The bottom top strip is associated with Chan0_in, and so forth.

All of the project LabVIEW files are programmed to be consistent with the plus bus (rail), Chan0_out, and the minus bus (rail), Chan1_out. Therefore, it is intuitively helpful to have the output channels physically connected in this fashion.

The project examples included with the book were conducted on a special circuit box that connects directly to the shielded 68-pin connector. This bypasses the connector block. A shielded cable is strongly recommended in any event. Many of the projects involve the measurement of relatively low voltage signals.

In addition, the lab projects included in the book require the following (or equivalent):

- Pentium PC (or equivalent).
- LabVIEW 6.0i Student Edition or LabVIEW 6.0i or later version.
- Mathcad Professional 2001 or later version.
- National Instruments Shielded 68-pin Cable.

Semiconductor Devices and Components (Recommended)

6-Transistor (3-gate) CMOS Array – CD4007[^1]
CMOS Opamp – SGS-Thomson TS271

NPN - Medium-Power NPN BJT – NTE186

PNP - Medium-Power PNP BJT – NTE187

Capacitors

Resistors
The CD4007 chip contains three CMOS inverters or three PMOS and three NMOS transistors. Since they are inverters, NMOS and PMOS pairs have Hardware and Software Requirements internally connected gates. However, this does not prevent having a sufficient number of the individual transistors in the analog laboratory projects.

The TS271 is chosen as it has simple external resistor biasing. Thus, students can gain an intuitive feel for the relation between the characteristics of the CMOS opamp and bias current with straightforward exchange of bias resistors. In the case of a group of students, for example, each student can select a different bias current, such that all of the results can be assembled to plot the opamp characteristics, such as gain and frequency response versus bias current. In addition, the circuitry of the opamp is straightforward and may be understood within the scope of the book. Extensive experience in our laboratory with devices has demonstrated that this opamp can withstand considerable abuse without failing even though it is a MOSFET chip. It is however, strongly advised that the power supply never be turned on until the power-supply pins, input pins and output pin are connected in the circuit.

The NTE186 is a rugged npn BJT that is investigated at current levels well below the normal operating range. Heating of the device is thus minimized and for the
measurements, it can be assumed to be at room temperature. Also, various high-level injection effects, which render the basic SPICE parameter set invalid, are avoided.

[****] Complementary paired with the NTE186.

**LabVIEW VI Libraries and Project and Problem Folders and Files**

Each project has a folder, which contains the LabVIEW library plus any related Mathcad files for that project. Mathcad files include those for the exercises and results analysis (project files). The project folder also has circuit-simulator subfolders for Schematics and Capture.

A LabVIEW VI library is included for each project. These are LabVIEW files with extension .lib. The LabVIEW files within a library have extension .vi. A given project library will contain most of the LabVIEW virtual instruments for that project. The additional VIs are in the User.lib folder, which is in the LabVIEW application folder. The User.lib folder contains all the LabVIEW libraries and other LabVIEW files that are not included in the individual project libraries. The folders are Read_Rite, Dat_File, FunctGen, and Subvi.

Each problem folder has a set of problems associated with the unit with the same number. Each problem set has a pdf file (Word), a Mathcad solutions file, a pdf version on the Mathcad file and a circuit-simulator subfolder.

There are also pdf files for the composite of the problems (WordProb.pdf), Mathcad problem-solution files (MathcadProb.pdf), project exercises (MathcadExer.pdf), project Schematics exercises (SchematicsExer.pdf), and project Capture exercise (CaptureExer.pdf).

The procedure for installation of the libraries from the CD onto the computer is described in the Readme files.

**Unit 1. Elementary Circuit Analysis for Analog Electronics**

In this unit, we present a basic review of segments of circuit analysis which recur repeatedly in electronic circuits. A firm grasp on these is essential to developing an understanding of the analysis and design of basic electronic circuits. A transistor is included in the circuits to show a correlation between circuit analysis and electronics. Only steady-state circuit situations are considered here. This includes dc and sinusoidal. Some transient analysis is considered in connection with operational amplifier applications with capacitors.
1.1. Resistor Voltage Divider and MOSFET DC Gate Voltage

Figure 1.1(a) shows a basic NMOS amplifier stage. This is the dc (or bias) portion of the circuit, which excludes the signal part. The terminals of the transistor are designed G (gate), D (drain) and S (source). The design calls for a dc voltage $V_G$, with respect to the zero reference voltage, which is obtained by dividing the supply voltage $V_{DD}$ between bias resistors $R_{G1}$ and $R_{G2}$. Since the gate terminal has zero current, the voltage, $V_G$, at the gate can be assessed with the resistor network separated from the circuit as in Fig. 1.1(b). The goal is to relate the node voltage $V_G$ to the values of $R_{G1}$ and $R_{G2}$ and $V_{DD}$. The result is the basic resistor voltage-divider relation.

**Figure 1.1. (a) Dc circuit for the basic NMOS amplifier. (b) Circuit for determining the gate voltage, $V_G$.**

Note that since $V_{DD}$ is given with respect to the reference zero volts, the $V_{DD}$ designation at the top node is equivalent to the supply voltage, also referred to as $V_{DD}$. The current $I_{RG}$ is

Equation 1.1

$$I_{RG} = \frac{V_{DD}}{R_{G1} + R_{G2}}$$

The voltage across the resistor $R_{G2}$ is $V_G$ (since $V_G$ is with respect to the zero reference) and this is

Equation 1.2
It can be concluded that the gate voltage is the value of $R_{G2}$ divided by the sum of the two gate-bias resistors.

1.2. Output Circuit and DC Drain Voltage

For the dc circuit in Fig. 1.1, the drain voltage is determined from

Equation 1.3

As illustrated in Fig. 1.2, for the purpose of a solution to (1.3), the transistor can be replaced by a current source as shown in Fig. 1.2. Drain current $I_D$ is a function of $V_G$; that is, $I_D = f(V_G)$. Thus, in a design, the value of $V_G$ determines the value of $V_D$. $I_D$ is related to $V_G$ according to

Equation 1.4

$$V_D = V_{DD} - I_D R_D$$

**Figure 1.2. Circuit for illustrating the determination of the drain voltage, $V_D$.**

This relation and parameters $V_{th0}$ and $k_n$ are discussed in Unit 2.
1.3. Frequency Response of the Amplifier Stage

Capacitance associated with amplifiers may cause the output to fall off at low and high frequencies. This effect is referred to as the frequency response of the amplifier. A generalization of possible capacitance is shown in the circuit of Fig. 1.3. Capacitor $C_g$ is an external capacitance, which is included to attach a sine-wave signal source, consisting of $V_{\text{sig}}$ (e.g., sine-wave peak) and $R_s$, without interrupting the dc bias circuitry. Similarly, there could be an output capacitance, which couples the signal output voltage to an external load resistor. Capacitor $C_T$ is associated with the internal capacitance of the transistor. It may be regarded as an equivalent effective capacitance that represents all of the capacitance of the transistor.

*Figure 1.3. Amplifier including possible circuit capacitance.*

Generally, the frequency range over which a given capacitor is effective is much different for the two capacitors. Capacitor $C_g$ affects the output at low frequencies, while the effect of $C_T$ is realized at the high end of the spectrum. Thus, their effects can be considered separately if, as assumed in the following, the high and low ends of the response function are widely separated in frequency, that is, by several orders of magnitude.

*Figure 1.4 shows the signal circuits for the two cases of low (a) and high (b) frequencies.*

As discussed in Unit 2, the signal circuit is formulated from the complete circuit by setting all dc voltages to zero. This includes, for this amplifier, the power supply and dc voltage across the capacitor $C_g$. Note that the transistor plays no apparent role in the frequency response in the equivalent circuit. It is, of course, critically important in dictating the value of $C_T$.

*Figure 1.4. Circuits for low (a) and high (b) frequencies.*
The two circuits, (a) and (b), are technically high-pass and low-pass circuits, respectively. In combination, they have a midband range, which is the normal range of frequency for operation of the amplifier. As mentioned above, if the midband separates the low and high portions by a sufficient range of frequency, the effects may be considered separately, as suggested in Fig. 1.4.

The response function is obtained by considering the frequency dependence of the node voltage $V_g(f)$ for the constant-magnitude sine-wave source voltage, $V_{\text{sig}}$. (Since the only voltages under consideration in the circuits of Fig. 1.4 are those associated with signals, lowercase subscript is used. This is discussed further in Unit 2.)

The frequency response is first considered for the low end of the spectrum and involves $C_g$ only, as in the circuit of Fig. 1.4(a). We can utilize the voltage-divider relation obtained above as (1.2). For this case this is

**Equation 1.5**

$$V_g(f) = \frac{R_G}{R_G + R_s + \frac{1}{j2\pi f C_g}} V_{\text{sig}} = \frac{R_G}{R_G + R_s + \frac{1}{j2\pi f (R_G + R_s) C_g}} V_{\text{sig}}$$

where $R_G = R_{G1} \parallel R_{G2}$.

Using the definitions

**Equation 1.6**

$$V_{go} = \frac{R_G}{R_G + R_s} V_{\text{sig}}$$

and
\textbf{Equation 1.7}
\[ f_{lo} = \frac{1}{2\pi (R_g + R_z) C_g} \]

the result is condensable to

\textbf{Equation 1.8}
\[ V_g (f) = V_{go} \frac{1}{1 - \frac{f_{lo}}{f}} \]

The magnitude is

\textbf{Equation 1.9}
\[ |V_g (f)| = V_{go} \frac{1}{\sqrt{1 + \left(\frac{f_{lo}}{f}\right)^2}} \]

At \( f = f_{lo} \), \( V_g (f) = V_{go} / \sqrt{1 + 1} \). This, by definition, is the response magnitude for the 3-dB frequency, \( f_{3dB} \), for the low-frequency end of the response function. That is, in general, \( f_{3dB} \) is the frequency at which the response falls to \( 1/\sqrt{2} \) (for decreasing frequency) from the maximum, asymptotic value. Thus, for the simple case here of one capacitor, \( f_{3dB} = f_{lo} \).

The equation for the response function associated with \( C_T \) is similar to (1.8) and is

\textbf{Equation 1.10}
\[ V_g (f) = V_{go} \frac{1}{1 + \frac{f}{f_{hi}}} \]

where
The frequency $f_{3dB}$ for this case is just $f_{hi}$. The frequency response of circuits of the type of Fig. 1.4 is measured in Project 1. In the design of the project circuits, capacitors and resistors are selected to give widely different $f_{lo}$ and $f_{hi}$ values.

### 1.4. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_G = V_{GS} = V_{R_{G2}} = I_{G} R_{G2} = \frac{R_{G2}}{R_{G1} + R_{G2}} V_{DD}$</td>
<td>Resistor-circuit voltage divider.</td>
</tr>
<tr>
<td>$I_D = k_n (V_G - V_{t, no})^2$</td>
<td>Drain current and gate voltage relation.</td>
</tr>
<tr>
<td>$V_g(f) = V_{go} \frac{1}{1 - \frac{f_{lo}}{f}}$</td>
<td>Low-frequency frequency-response function.</td>
</tr>
<tr>
<td>$V_g(f) = V_{go} \frac{1}{1 + \frac{f}{f_{hi}}}$</td>
<td>High-frequency frequency-response function.</td>
</tr>
<tr>
<td>$V_{go} = \frac{R_G}{R_G + R_s} V_{sig}$</td>
<td>Midband magnitude of the signal gate voltage.</td>
</tr>
</tbody>
</table>

### 1.5. Exercises and Projects

**Project Mathcad Files**

- Exercise01.mcd - Project01.mcd

**Laboratory Project 1**  
*Basic Circuit Analysis for Electronic Circuits and Programming Exercises*

- P1.1 Resistor Voltage-Divider Measurements
- P1.2 Resistor Voltage Divider with Current Measurement
- P1.3 Resistor Voltage Divider with Resistor Measurement
- P1.4 Resistor Voltage Divider with a Sine-Wave Source Voltage
- P1.5 Frequency Response of a Resistor-Capacitor Circuit

## Unit 2. Transistors and Voltage Amplification
Radio transmitters and receivers have existed since before the end of the nineteenth century. A practical form of wireless telegraph, attributed to G. Marconi, appeared in 1895, and successful transmission across the Atlantic Ocean was achieved in 1901. However, in the early part of the twentieth century, systems were limited by the lack of a means of voltage amplification. The appearance of a voltage amplification device, the vacuum tube, dramatically improved the concept, as microvolt signals could be boosted for receiving and transmitting.

In the middle of the twentieth century, the transistor appeared. The idea of transistors based on a sandwich of pn junctions (BJT) and a field-effect transistor based on pn junctions (JFET) and on a metal–oxide–semiconductor (MOS) structure (basically, a capacitor) were all understood at the time. However, pn-junction devices became a practical realization much sooner than the MOS structure, due to fabrication complications in producing the MOS device as well as perhaps a perceived lack of need. The JFET served as an interim field-effect transistor until the MOS technology evolved. It provided for a transistor with very high input resistance and was used extensively as the input transistors for BJT opamps.

A textbook on radio, Elements of Radio, published in 1948 (Marcus and Marcus, 1948), makes no mention of transistors. A 1958 text, (Millman, 1958), Vacuum-Tube and Semiconductor Electronics, gives equal weight to vacuum tubes and BJTs in electronic circuits but makes no mention of the field-effect transistor. Slightly later (Nanavati, 1963), in An Introduction to Semiconductor Electronics, as the title suggests, vacuum tubes are dropped completely and the only reference to a field-effect transistor is in one section of the last chapter and this refers to a junction field-effect transistor. In 1965, in his textbook Analysis and Design of Electronic Circuits, Chirlian devotes a small portion of the book to vacuum tubes, but most of the emphasis is on circuits based on the BJT (Chirlian, 1965). No mention is made of the field-effect-transistor. An example of a book in which BJTs and field-effect transistors of both types were finally given balanced treatment was published in 1979 (Millman, 1979). Textbooks tend to lag the industry a bit, and during the 1970s, MOSFET circuits were emerging rapidly, driven by the simultaneous development of integrated circuits. The four editions of a text on analog circuits by Gray and Meyer, (1977, 1984, 1993) and Gray, et al. (2001) serve well as a series through which we observe a transition from mostly BJT to, in the last two editions, more-or-less equal treatment of BJT and MOSFET devices. A recent textbook on the subject of analog integrated circuits (Johns and Martin, 1997) takes the approach that such circuits are now totally dominated by MOSFETS but includes some BJT applications. BiCMOS, a combination of MOSFET and BJT devices on the same integrated circuit, is growing in popularity as more ways of taking advantage of the superior properties of the two transistor types are developed.

Since the earliest transistors, there has been persistent competition between BJT and MOS transistors. It has been, to a large extent (along with many other considerations), a matter of power consumption versus speed; the BJT has been faster but is associated with high power consumption. The MOSFET has gradually taken over as the most important transistor, with increased emphasis on integrated circuits and improved speeds.
2.1. BJT and MOSFET Schematic Symbols, Terminal Voltages, and Branch Currents

The BJT can be either a pnp or an npn. The MOSFET similarly can be a pmos or an nmos. The equivalents are npn and nmos and pnp and pmos. The following discussion is based on the npn and nmos, as shown in Fig. 2.1. (All polarities and current directions are reversed for the pnp and pmos. This provides for important versatility in applications.)

**Figure 2.1. BJT npn and MOSFET nmos transistors. The terminal configurations are designated common emitter and common source.**

![BJT npn and MOSFET nmos transistors](image)

The BJT terminals are designated collector, base, and emitter while those of the MOSFET are drain, gate, and source. The terminal configurations in Fig. 2.1 are, for the BJT, the common emitter, and for the MOSFET, the common source, in amplifier-stage parlance. This suggests that both the input (left side) and output (right side) are referred to the common terminal. For example, for the BJT, the input terminal voltage is $V_{BE}$ and the output terminal voltage is $V_{CE}$. Similarly, for the MOSFET, we have $V_{GS}$ and $V_{DS}$. Note that in the convention of subscripts in electronics, the first subscript is assigned positive. This matches the assignments in the diagram, and the plus and minus signs are superfluous.

Note also the convention for symbols for all currents and voltage.

- Total voltage and current: $v_{XY}, i_X$
- Dc, bias, quiescent, or operating point: $V_{XY}, I_X$
- Signal or ac (RMS, peak): $V_{xy}, I_x$
- General instantaneous signal: $v_x, i_x$

The voltage and current symbols in Fig. 2.4 are therefore for dc. For a voltage, a single subscript means that this terminal (or node) voltage is referred to the common terminal. For example, in the npn case above, $V_{CE} = V_C$.

**Figure 2.4. Basic NMOS amplifier with resistor gate biasing and input signal $V_s$. (a) Complete circuit. (b) Signal (or ac or incremental) circuit. The signal circuit**
is obtained by setting the power supply (dc) node to zero volts. (c) Linear signal circuit replaces the linear schematic representation.

The input terminals \(v_{BE}\) and \(v_{GS}\) are the control terminals; that is, they control the output currents \(i_C\) and \(i_D\). In both cases, the terminal pairs possess extremely nonsymmetrical voltage – current behavior. With the polarities as shown, the currents flow readily, whereas with the opposite polarities, the output currents are cut off or are, for most purposes, essentially zero.

The basic (simplified) general relations between the currents and voltages are:

Equation 2.1

\[
\text{BJT: } i_C = I_c e^{v_{BE}/V_T}
\]

Equation 2.2

\[
\text{NMOS: } i_D = \kappa_n \left(v_{GS} - V_n\right)^2
\]
\(I_S, V_T, k_n, V_{in}, \) and \(V_T\) are device model parameters or physical constants.

In linear circuit applications, for example, as amplifier stages, the transistors are provided with a circuit configuration that sets up dc, or bias, currents and terminal voltages (sometimes referred to as the Q-point, for quiescent, or in SPICE, the operating point). In the amplifier application, a signal voltage is applied to the input, that is, superimposed on the dc magnitude, which must be much smaller than the dc voltage if the signal input-output relation is to be linear. This is apparent from (2.1) and (2.2), which are nonlinear relations. All of the currents and terminal voltages will change in response to the input signal, and all of these incremental changes must be small compared to any of the dc currents or voltages, in order for the linear relationships to be valid.

In circuit applications, both types of transistors are operated in all three possible terminal configurations. This provides for a wide variety of amplifier-stage characteristics, including gain and input and output impedance.

### 2.2. Fundamentals of Signal Amplification: The Linear Circuit

The most fundamental property of a useful electronic voltage amplification device is that it possess a transconductance that leads to the possibility of voltage gain. Transconductance is defined as the ratio of the signal (ac, incremental) current out, \(i_{out} \equiv \delta i_{OUT}\), and the applied input signal voltage, \(v_{in} \equiv \delta v_{IN}\). That is, transconductance \(g_m\) is

\[
g_m = \frac{\delta i_{OUT}}{\delta v_{IN}} = \frac{di_{OUT}}{dv_{IN}} = \frac{i_{out}}{v_{in}}
\]

Equation 2.3

For the BJT, \(i_{OUT} \equiv i_C\) and \(v_{IN} \equiv v_{BE}\), while for the NMOS, \(i_{OUT} \equiv i_D\) and \(v_{IN} \equiv v_{GS}\). Thus, (2.1) and (2.2) can be used for the BJT and MOSFET, respectively, to obtain an expression for \(g_m\). The results are

\[
BJT: g_m = \frac{I_C}{V_{BE}} = \frac{I_C}{V_T}
\]

Equation 2.4

and
Equation 2.5

\[ g_m = \frac{I_d}{V_{GS}} = \frac{2I_D}{V_{GS} - V_{Tn}} \]

\( I_C \) and \( I_D \) are the dc (bias) currents of the transistors, so for comparison they can be made equal. At room temperature, the thermal voltage is \( V_T = 26 \text{ m} \). For the MOSFET, \( V_{GS} \) is the gate – source bias voltage and \( V_m \) is the transistor threshold voltage. The difference, as in the denominator of the transconductance expression, could typically be about \( V_{GS} - V_m = 500 \text{ mV} \).

The expression (2.3) suggests the linear model given in Fig. 2.2. Included in the model is an input resistance, \( r_{in} \), which accounts for the fact that there can be an incremental current flowing into the input terminal for an increment of input voltage. The model applies in general to amplifying devices, including the vacuum tube (VT), BJT, JFET, and MOSFET. There exists a wide range of magnitude of transconductance and input resistance between the devices. The input resistance, though, affects only the loading of the input signal source; otherwise, the relation of (2.3) applies in all cases, and the transconductance is the key to the gain for a given device type. The input resistance is essentially infinite for the vacuum tube and the MOSFET (common source) but can be as low as a few ohms in some configurations for the BJT (e.g., common base).

**Figure 2.2. Basic linear model of a voltage amplification device. Model parameters are \( g_m \) and \( r_{in} \).**

It is interesting to compare the transconductance of the BJT and MOSFET along with the vacuum tube. We will make a comparison at \( I_D = I_C = 10 \text{ mA} \) (suitable for a vacuum tube) even though transistors would not usually be operated at such high currents, especially in an integrated circuit. Consulting a source of information for a triode 6SN7 (perhaps one of the most common tubes of all time), one deduces from a graphical analysis the plate characteristics that, for example, \( g_m(\text{VT}) = 3 \text{ mA/V} \). From (2.4) and (2.5), we obtain \( g_m(\text{BJT}) = 385 \text{ mA/V} \) and \( g_m(\text{MOSFET}) = 40 \text{ mA/V} \) with \( V_{GS} - V_m = 500 \text{ mV} \). The BJT is decidedly superior in this respect, and this is one of the factors contributing to the sustained life of the transistor in industry. That is, the BJT amplifier stage can potentially have a much higher voltage gain. The vacuum tube is clearly inferior to both transistors.
and points to the reason for the need for so many amplification stages in some VT amplifiers.

The output voltage of amplifiers based on any of the devices will depend on the value of the load resistance, $R_L$, which is added to the circuit of Fig. 2.2 in Fig. 2.3. Note that, in general, $R_L$ is not necessarily an actual resistor but could be an effective resistance, as dictated by the amplifier circuitry that is connected to the output of a given stage, combined with a bias resistor. The output voltage induced across $R_L$ will be

\[ V_{\text{out}} = -I_{\text{out}}R_L = -g_mV_{\text{in}}R_L \]

*Figure 2.3. Basic linear model of a voltage amplification device with load $R_L$ connected.*

The minus sign is a result of the current flowing up through $R_L$. The signal voltage gain is the incremental output voltage divided by the incremental input voltage such that the gain can readily be obtained from (2.6) as

\[ a_v = \frac{V_{\text{out}}}{V_{\text{in}}} = -g_mR_L \]

Thus, the gain is directly related to the parameter $g_m$ for a given transistor. In general, $a_v$ can be positive or negative, depending on the terminal configuration. For example, the common base (BJT) and common gate (MOSFET) are positive (noninverting) gain amplifiers.
2.3. Basic NMOS Common-Source Amplifier

An example of the application of the transconductance relation for the transistor is the basic circuit in Fig. 2.4. Setting dc voltages (in this case, VDD) equal to zero in Fig. 2.4(a) leads to the signal (or ac) circuit [Fig. 2.4(b)]. This follows from the fact that the signal circuit involves only incremental variables (changes) and VDD is a constant.

The schematic symbol for the transistor in the signal circuit associates the output current with the input voltage according to the linear relation of (2.3). For linear circuit analysis, the linear equivalent circuit of Fig. 2.2 (Fig. 2.4(c)) replaces the linear schematic-symbol representation [Fig. 2.4(b)]. For the MOSFET, r_{in} is infinite and therefore omitted.

The overall gain from the signal source to the output is \( a_v = V_o/V_s \), which is

\[
a_v = \frac{V_o}{V_s} = \frac{V_o}{V_g} = \frac{R_{GL}}{R_{GL} + R_{G2}} g_m R_D
\]

where \( V_o/V_g \) is (2.7) and \( V_g/V_s \) is provided by the simple resistor-divider relation given in (1.2).

2.4. Transistor Output Resistance and Limiting Gain

The linear-equivalent circuit of Fig. 2.2 includes an idealization in that the output is a pure current source. In real transistors, the collector (BJT) or drain (MOSFET) current increases with increasing V\(_{CE}\) or V\(_{DS}\). This is accounted for by including an output resistance, r\(_{out}\), in the linear model, as added to the circuit in Fig. 2.5. For the BJT and MOSFET, respectively, the value of r\(_{out}\) is

Equation 2.9

\[
r_{out} = r_{CE} = \frac{\partial V_{CE}}{\partial i_C} = \frac{V_A}{I_C}
\]

Equation 2.10

\[
r_{out} = r_{DS} = \frac{\partial V_{DS}}{\partial i_D} = \frac{V_A}{I_D}
\]
where $V_A$ is the characterizing transistor parameter. Note that this voltage dependence is not included in (2.1) and (2.2); these equations are consistent with the simplified circuit model of Fig. 2.2. Similarly, the voltage dependence will alter $g_m$ from the simple forms of (2.4) and (2.5). This is discussed in Unit 4.

The actual gain, with a load $R_L$, which includes the output resistance, can be obtained from modification of (2.7) to include $r_{out}$ in parallel with $R_L$ as in Fig. 2.5. The result is

Equation 2.11

$$a_v = -g_m \frac{R_L r_{out}}{R_L + r_{out}}$$

The parameter $V_A$ of both transistors can typically be about 100 V. (In MOSFETs, the parameter is usually referred to as $\lambda$, which is the reciprocal, $\lambda = 1/V_A$.) A useful comparison between the devices is the maximum limiting gain of the common-emitter and common-source amplifier voltage gains, which applies for the case of $R_L \rightarrow \infty$. The gain in this case is

Equation 2.12

$$a_{v\text{lim}} = -g_m r_{out}$$

Using (2.4), (2.5), (2.9), and (2.10), we obtain for the limiting gain:

Equation 2.13
BJT: $a_{V_{\text{lim}}} = \frac{V_A}{V_T}$

\[ \text{MOSFET: } a_{V_{\text{lim}}} = -\frac{2V_A}{V_{GS} - V_{tn}} \]

Using sample numbers from above, the comparison gives $a_{V_{\text{lim}}}(\text{BJT}) \approx 4000$ and $a_{V_{\text{lim}}}(\text{MOSFET}) \approx 400$. The vacuum tube, type 6SN7, has a typical output resistance $r_{out} \equiv r_p \approx 7\, \text{K\Omega}$ (p for plate), which leads to a limiting gain magnitude of about 21. (This is referred to as the $\mu$ of the tube.) You have to respect the amplifier designers of the vacuum-tube era when considering what was accomplished despite the limitations of these amplifying devices.

In modern integrated circuits, it is possible to implement load circuits, which have an effective $R_L >> r_{out}$ such that the limiting gain can be achieved. This is particularly important in MOSFET amplifiers to make up for the relatively low value of $g_m$.

### 2.5. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_C = I_S e^{V_{BE}/V_T}$, $g_m = \frac{i_C}{V_T}$</td>
<td>BJT transfer function and transconductance relation.</td>
</tr>
<tr>
<td>$i_D = k_n \left( V_{GS} - V_{tn} \right)^2$, $g_m = \frac{2I_D}{V_{GS} - V_{tn}}$</td>
<td>MOSFET transfer function and transconductance relation.</td>
</tr>
<tr>
<td>$a_v = \frac{V_{out}}{V_{in}} = -g_m R_L$</td>
<td>General voltage-gain relation from the transistor input.</td>
</tr>
<tr>
<td>$a_v = -\frac{R_{G1}}{R_{G1} + R_{G2}} g_m R_D$</td>
<td>Gain relation from the signal source.</td>
</tr>
<tr>
<td>$r_{out} = \frac{V_A}{i_C}$</td>
<td>General relation for the transistor output resistance.</td>
</tr>
<tr>
<td>$a_v = -g_m \frac{R_{L} r_{out}}{R_L + r_{out}}$</td>
<td>Voltage gain, including the effect of the transistor output resistance.</td>
</tr>
</tbody>
</table>
2.6. Exercises and Projects

Project Mathcad
Files
Lab Project 2

P2.1 Basic NMOS Common-Source Amplifier with Programming Exercises
P2.2 NMOS Common-Source Amplifier with Resistor Gate Bias Circuit
P2.3 Amplifier with Signal and Gain Measurement

2.7. References to the Electronics Book Sequence


Unit 3. Characterization of MOS Transistors for Circuit Simulation

In this unit, the basic (Level 1 SPICE) dc MOSFET characteristic equations are introduced. The amplifier exercises and projects use the results for design and analysis. Circuit solutions are compared with measured results from the circuit to make an assessment of the degree to which the transistor models for the MOSFET represent actual device behavior. The parameters for this unit are presented in Table 3.1. Note that in the
case of KP, we can only measure K and would be able to extract KP only if gate width W and length L were known.

<table>
<thead>
<tr>
<th>SPICE Name</th>
<th>Math symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTO</td>
<td>$V_{tno}, V_{tpo}$</td>
<td>Zero-bias threshold voltage.</td>
</tr>
<tr>
<td>KP</td>
<td>$k = \frac{KP \cdot W}{2 \cdot L}$</td>
<td>Transconductance parameter.</td>
</tr>
<tr>
<td>Gamma</td>
<td>$\gamma_n, \gamma_p$</td>
<td>Body-effect parameter.</td>
</tr>
<tr>
<td>Phi</td>
<td>$2\Phi_F$</td>
<td>Surface inversion potential.</td>
</tr>
<tr>
<td>Lambda</td>
<td>$\lambda_n, \lambda_p$</td>
<td>Channel length modulation.</td>
</tr>
</tbody>
</table>

### 3.1. Physical Description of the MOSFET

A diagrammatic NMOS is shown in Fig. 3.1. The device consists of a three-layer structure of metal–oxide–semiconductor (MOS). A two-terminal MOS structure (connections to metal and semiconductor) is essentially a parallel-plate capacitor. In the same manner as for a normal capacitor, when a positive gate voltage, $V_G$, is applied with respect to the p-type body (for NMOS) (i.e., with respect to the metal contact on the underside of the p-type semiconductor body (or substrate)), negative charges are induced under the oxide layer in the semiconductor. When $V_G$ (with respect to the semiconductor body) exceeds the threshold voltage, $V_{tno}$, a channel of free-carrier electrons forms under the oxide; that is, the onset of the channel occurs when $V_G = V_{tno}$. The substrate is n type for the PMOS and the channel is made up of free-carrier holes.

*Figure 3.1. MOS transistor consisting of a metal – oxide – semiconductor layered structure (plus a metal body contact on the bottom). A positive gate voltage, $V_G > V_{tno}$, induces a conducting channel under the oxide, which connects the two n regions, source and drain. All voltages are with respect to $V_B$, that is, the body (substrate) of the transistor. (a) No channel; (b) uniform channel; (c) channel is just pinched off at the drain end of the channel; (d) channel length is reduced due to drain pn-junction depletion region extending out along the channel.*
An n-channel MOSFET device is then completed by fabricating n regions, source and gate, for contacting the channel on both ends of the channel. For $V_G < V_{tno}$ [Fig. 3.1(a)] there is no channel under the oxide, and the two n regions are isolated pn junctions. When $V_G > V_{tno}$ and source voltage, $V_S$, and drain voltage, $V_D$, are both zero (all with respect to the body) [Fig. 3.1(b)] a uniform-thickness n-type channel exists along the length of the oxide layer and the source and drain regions are connected by the channel. Thus, the channel is a voltage-controlled resistor where the two ends of the resistor are at the source and drain and the control voltage is applied at the gate.

In electronic circuit applications, the terminal voltages are referred to the source; gate and drain voltages are designated as $V_{GS}$ and $V_{DS}$ (NMOS). In analog circuits, $V_{GS} > V_{tno}$ (in order for a channel to exist), $V_{DS}$ is positive, and a drain current flows through the channel and out by way of the source (and the gate current is zero). On the drain end of the channel, the voltage across the oxide layer is $V_{GD} = V_{GS} - V_{DS}$. The channel at the drain end just shuts off when $V_{GD} = V_{tno}$. $V_{DSsat} = V_{GS} - V_{tno}$ [Fig. 3.1(c)] is defined for this condition as the saturation voltage. The transistor is referred to as in the linear (or triode) region or active region for $V_{DS} < V_{DSsat}$ and $V_{DS} > V_{DSsat}$, respectively.

For $V_{DS} > V_{DSsat}$ (active mode of operation), the channel length decreases from $L$ to $L'$ as the reverse-biased depletion region of the drain pn junction increases along the channel (along the oxide–semiconductor interface) [Fig. 3.1(d)]. The increment $V_{DS} - V_{DSsat}$ drops across the depletion region of the drain pn junction. In long-channel devices, the reduction of channel length is relatively small compared to the channel length. In this case, the length is roughly a constant and the channel resistance, for a given $V_{GS}$, is independent of $V_{DS}$. 
From a circuit point of view, for $V_{DS} \gg V_{DSSat}$, by Ohm's law,

\[
I_D \approx \frac{V_{DSSat}}{R_{chan}(V_{GS})}
\]

where $R_{chan}(V_{GS})$ is the resistance of the channel and is a function of $V_{GS}$. Assuming that $L' \approx L$, for a given $V_{GS}$, $R_{chan}(V_{GS})$, and thus $I_D$, is approximately a constant for $V_{DS} \geq V_{DSSat}$. Thus, the drain, in circuit terms, appears like a current source. In many modern MOSFET devices, this is only marginally valid. In the following, the definition $V_{effn} \equiv V_{DSSat} = V_{GS} - V_{tno}$ will be used. (The subscript is an abbreviation for effective.) The PMOS has a counterpart, $V_{effp} \equiv V_{SDDsat} = V_{SG} - V_{tpo}$. $V_{effp}$ is a frequently recurring term in device and circuit analytical formulations.

### 3.2. Output and Transfer Characteristics of the MOSFET

The equations used in the following to characterize the MOSFET transistor are from the SPICE Level 1 model. SPICE also has more detailed models in Level 2 and Level 3. These can be specified when running SPICE. However, the number of new model parameters, in general, in circuit simulation is practically boundless. Level 1 is chosen here as it is the most intuitive, that is, the most suitable for an introductory discussion of device behavior. Some new models, for example, which focus on frequency response at very high frequencies, can include pages of equations. In addition, Level 1 is suitable and adequate for many examples of circuit simulation.

The basic common-source NMOS circuit configuration is repeated in Fig. 3.2. Here it serves as a basis for discussing the dc SPICE parameters of the MOSFET transistor. In the example, $V_{DS} = V_{DD}$. The output characteristic is a plot of $I_D$ versus $V_{DS}$ for $V_{GS} = \text{const}$. A representative example is shown in Fig. 3.3. As mentioned, the low-voltage region is referred to as the linear region, triode region, or presaturation region. Outside this region for higher voltages is the active (saturation) region. This is referred to here as the active region to avoid confusion with the fact that the nomenclature is just the opposite in the case of the BJT; that is, the low-voltage region is called the saturation region. As discussed in Unit 3.1, the linear and active regions are delineated by $V_{effn} \equiv V_{DSSat} = V_{GS} - V_{tno}$.

**Figure 3.2.** Common-source circuit configuration for discussion of the dc model parameters of the NMOS transistor. The three-terminal transistor symbol implies that the body and source are connected.
The output-characteristic equation in the linear region corresponds to $V_{DS}$ ranging from the condition of Fig. 3.1(b) to that of Fig. 3.1(c). As $V_{DS}$ increases from zero, the channel begins to close off at the drain end (i.e., the channel becomes progressively more wedge shaped). The result is an increase in the resistance of the channel as a function of $V_{DS}$, and therefore a sublinear current–voltage relation develops.

When $V_{GS} > V_{th}$, the electron charge in the channel can be related to the gate voltage by $Q_{\text{chan}} = C_{\text{ox}}(V_{GS} - V_{th})$ (per unit area of MOSFET looking down at the gate), where $C_{\text{ox}}$ is the parallel-plate capacitance (per unit area) formed by the MOS structure. This provides a simple linear relation between the gate voltage and the charge in the channel.

The conductivity in the channel is $\sigma_{\text{chan}} = \mu_{n}Q_{\text{chan}}/t_{\text{chan}}$, where $\mu_{n}$ is the mobility of the electrons in the channel and $t_{\text{chan}}$ is the thickness of the channel into the semiconductor. Thus, in the case of a uniform channel (i.e., for $V_{DS} \rightarrow 0$), the channel conductance is Equation 3.2
Equation 3.3

\[ k_n = \frac{K_{P_n}}{2} \frac{W}{L} \]

where \( K_{P_n} = \mu_n C_{ox} \) is the SPICE transconductance parameter (the \( n \) subscript is the equation symbolic notation for the NMOS; the parameter in the device model is just \( K_P \)), \( W \) is the physical gate width, and \( L \), again, is the channel length. Parameter \( K_{P_n} \) is related to the electron mobility in the channel and the oxide thickness. Therefore, it is very specific to a given MOSFET device.

As \( V_{DS} \) increases, but is less than \( V_{eff,n} \) [transition from Fig. 3.1(b) to 3.1(c)], the wedge-shaped effect on the channel is reflected functionally in the channel conductance relation as

Equation 3.4

\[ G_{\text{chan}} = 2k_n \left( V_{\text{eff,n}} - \frac{V_{DS}}{2} \right) \]

This leads to an output characteristic equation for the linear region, which is

Equation 3.5

\[ I_D = G_{\text{chan}} V_{DS} = 2k_n \left( V_{\text{eff,n}} V_{DS} - \frac{V_{DS}^2}{2} \right) \]

The derivation leading to (3.4) and (3.5) is given in Unit 3.4. The linear-region relation, (3.5), is applicable for \( V_{DS} \) up to \( V_{DS} = V_{eff,n} \), which is the boundary of the linear and active regions. The active-region equation is then obtained by substituting into (3.5), \( V_{DS} = V_{eff,n} \), giving
This active-region current corresponds to the zero-slope ideal curve in Fig. 3.3. As discussed in Unit 3.1, the drain current is not actually constant in the active region (in the same manner as for a BJT), due to the fact that the physical length of the channel is reduced for increasing $V_{DS}$ beyond $V_{DS} = V_{effn}$. The reduction in the channel length has the effect of slightly reducing the resistance of the channel. This is taken into account using the fact that $k_n \propto 1/L$, from (3.3), where $L$ is the effective physical length between the source and drain regions. For $V_{DS} > V_{effn}$, a reduced length $L' = L(1 - \lambda_n V_{DS})$ is defined which leads to a new effective $k'_n$.

Equation 3.7

$$k'_n = k_n \left(1 + \lambda_n V_{DS}\right)$$

where $\lambda_n$ is the SPICE channel-length modulation parameter (Lambda). Substituting $k'_n$ for $k_n$ in (3.6) produces

Equation 3.8

$$I_D = k'_n V_{effn}^2 \left(1 + \lambda_n V_{DS}\right)$$

(Note: A preferred form would be $I_D = k_n V_{effn}^2[1 + \lambda_n (V_{DS} - V_{effn})]$ because the channel-length effect only begins for $V_{DS} > V_{effn}$ and $k_n$ could be defined properly for effective length $L$ at $V_{DS} = V_{effn}$. Level 1 SPICE uses (3.8).)

Level 1 SPICE also applies this channel-length reduction factor to the equation in the linear region, (3.5). To match the linear-region equation to the active-region equation, (3.5) becomes, at the edge of the active -- linear regions,

Equation 3.9

$$I_{DSat} = k_n V_{effn}^2 \left(1 + \lambda_n V_{effn}\right)$$
and, in general

Equation 3.10

\[ I_D = 2k_n \left( 1 + \lambda_n V_{DS} \right) \left( V_{eff} V_{DS} - \frac{V_{DS}^2}{2} \right) \]

[Again, the fact that the channel length is not reduced with the transistor in the linear region would suggest the use of (3.9) throughout the linear region. Level 1 SPICE uses (3.8) and (3.10).]  

In general, \( V_{in} \) is a function of the source-body voltage, \( V_{SB} \). We assume for the moment that \( V_{SB} = 0 \). This applies, for example, to the common-source circuit in Fig. 3.2, since the body will always be at zero volts, and the source in this case is grounded as well. For this case, \( V_{in} = V_{tno} \), as used above. In laboratory projects we measure the output characteristic from which parameter \( \lambda_n \) can be obtained. This is based on (3.8). The I – V slope in the active region is

Equation 3.11

\[ \text{slope} = \frac{\partial I_D}{\partial V_{DS}} = k_n V_{eff}^2 \lambda_n \]

From the data measured, a straight-line curve fit determines the slope and the zero \( V_{DS} \) intercept (\( I_D \) at \( V_{DS} = 0 \)). These are used in (3.11) to obtain \( \lambda_n \) from \( \lambda_n = \text{slope/intercept} \). The intercept is the extension of the active region of Fig. 3.3 (dashed line) to the \( I_D \) axis.

When applying the equations of this development to the PMOS, the voltage between the gate and source is defined as positive with respect to the source, that is, \( V_{SG} \). To be consistent, the threshold voltage for the PMOS, \( V_{tp} \), is also positive. In the SPICE model, however, the threshold voltage is assigned negative because positive is taken for both types of devices with respect to the gate (\( V_{GS} \) is negative for the PMOS), and the threshold voltage for the PMOS is negative.

The transfer characteristic is obtained by holding \( V_{DS} \) constant and varying \( V_{GS} \). In the MOSFET parameter-determination experiments of Projects 3 and 4, we plot \( V_{GS} \) versus \( \sqrt{I_D} \) for the transistor biased into the active region. The equation is

Equation 3.12

\[ V_{GS} = \frac{\sqrt{I_D}}{k_n^2} + V_{tno} \]
where \( k_n' \) is (3.7)

\[
k_n' = k_n \left( 1 + \lambda_n V_{DS} \right)
\]

The slope in (3.12) is \( 1/\sqrt{k_n'} \) and the zero \( \sqrt{k_n'} \) intercept is expected to be \( V_{tno} \). LabVIEW obtains the slope and intercept from a straight-line fit to the data. The measured transfer characteristic thus yields the two parameters \( k_n' \) and \( V_{tno} \).

In Project 4, parameter \( \lambda_n \) is obtained from finding \( k_n' \) at two different \( V_{DS} \) values. This is based on Equation 3.13

\[
\frac{k_{n10}}{k_{n3}} = \frac{1 + \lambda_n (10\ \text{V})}{1 + \lambda_n (3\ \text{V})}
\]

where the \( k_n' \) values are measured and \( \lambda_n \) is the only unknown.

### 3.3. Body Effect and Threshold Voltage

In Fig. 3.4 is shown an example of a circuit in which the body and source cannot be at the same voltage. We now use the four-terminal symbol for the NMOS, which includes the body contact. In most applications, the body would be tied to the lowest potential in the circuit (NMOS), in this case, \( V_{SS} \) (e.g., \( V_{SS} = -5 \text{ V} \)). But by the nature of the circuit, the source voltage is \( V_S = V_{SS} + I_D R_S \), such that the source-body voltage is \( V_{SB} = I_D R_S \).

**Figure 3.4. NMOS transistor circuit with a resistor, \( R_S \), in the source branch. With the body attached to \( V_{SS} \), \( V_{SB} = I_D R_S \).**
In MOSFET devices, the threshold voltage depends on \( V_{SB} \) and in SPICE is modeled according to (NMOS) Equation 3.14

\[
V_{t,n} = V_{t,\text{no}} + \gamma_n \left( \sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F} \right)
\]

SPICE parameters contained in the equation are \( V_{t,\text{no}} \) (VTO), \( \gamma_n \) (Gamma), and \( 2\Phi_F \) (Phi) (Table 3.1). Typically, \( \gamma_n \approx 0.5 \, \text{V}^{1/2} \) and \( 2\Phi_F \approx 0.6 \, \text{V} \). Therefore, for example, for \( V_{SB} = 5 \, \text{V} \), the body effect adds 0.8 V to \( V_{t,\text{no}} \).

In the case of the CMOS array ICs of our lab projects (CD4007), the body effect for the PMOS is significantly less pronounced than for the NMOS (\( \gamma_p < \gamma_n \)), but the parameter for the channel-length-modulation effect is much smaller for the NMOS than for the PMOS (\( \lambda_n < \lambda_p \)). The combination suggests that the chip is a p-well configuration; that is, the NMOS devices are fabricated in "wells" of p-type semiconductor that are fabricated into an n-type substrate. The PMOS devices reside directly in the n-type substrate material. As far as our measurements are concerned, the extremes in parameters are an advantage, as we are interested in observing the effects of the various parameters.

In Project 4, a number for \( \gamma_n \) is obtained by measuring \( V_{t,n} \) as a function of \( V_{SB} \). The results are plotted as \( V_{t,n} \) versus \( \sqrt{V_{SB} + 2\Phi_F} - \sqrt{2\Phi_F} \). LabVIEW calculates the X variable. The data plotted should give a straight line with slope \( \gamma_n \). The effectiveness of SPICE modeling for representing the behavior of the transistor in a circuit is investigated in Project 4. The transfer characteristic, \( V_{GS} \) versus \( I_D \), is measured for a circuit of the type shown in Fig. 3.4, where the circuit has \( V_{SB} = I_D R_S \). In the project, \( V_{SS} \) is swept over a range of values to produce a range of \( I_D \) of about a decade. From (3.14), the threshold voltage characteristic that includes the body effect is

Equation 3.15
The input circuit loop equation (Fig. 3.4) is

Equation 3.16

\[-V_{SS} = I_D R_S + V_{GS}\]

Including the body effect, \(V_{GS}\) is now [from (3.12)]

Equation 3.17

\[V_{GS} = \sqrt{\frac{I_D}{k_n \left(1 + \lambda_n V_{GS}\right)}} + V_{tn}\]

where, for this special case, \(V_{DS} = V_{GS}\) (\(V_D = 0, V_S = 0\)).

A solution is obtainable through combing (3.14), (3.16), and (3.17) for \(I_D\) and \(V_{GS}\). These equations contain every parameter from this discussion of MOSFET SPICE parameters along with \(R_S\). In a project Mathcad file, Project04.mcd, a solution is obtained to provide a comparison with the measured \(V_{GS}\) versus \(I_D\) for the circuit. The Mathcad iteration formulation is, from (3.16),

Equation 3.18

\[I_D(V_{SS}, V_{GS}) = \frac{|V_{SS}| - V_{GS}}{R_S}\]

and, from (3.15) and (3.17),

Equation 3.19

\[V_{GS} = \sqrt{\frac{I_D(V_{GS}, V_{SS})}{k_n \left(1 + \lambda_n V_{GS}\right)}} + V_{tn} + \gamma_n \left(\sqrt{I_D(V_{GS}, V_{SS}) R_S + 2\Phi_F} - \sqrt{2\Phi_F}\right)\]
I_D and V_GS are found for the range of V_SS corresponding to that used in the measurement, which is 2.5 < |V_SS| < 10 V.

### 3.4. Derivation of the Linear-Region Current – Voltage Relation

The voltage along the channel is defined as V_c(x) (Fig. 3.5), with the range 0 at x = 0 (source) to V_c(L) = V_D (drain). The device is in the linear-region mode, that is, V_D < V_\text{eff}.

The charge in the channel at x is

\[ Q_\text{chan} = C_{\text{ox}} \left[ V_{\text{GS}} - V_c(x) - V_{\text{tno}} \right] \]

where the charge at the source is \( Q_\text{chan} = C_{\text{ox}} (V_{\text{GS}} - V_{\text{tno}}) \), as in the case of (3.2).

**Figure 3.5. Diagrammatic NMOS transistor biased into the linear region.**

A generalization of (3.2) for the incremental conductance, \( dG_\text{chan}(x) \), at x over a length dx is

\[ dG_{\text{chan}}(x) = \sigma_{\text{chan}} \frac{t_{\text{chan}} W}{dx} = \mu_n Q_{\text{chan}}(x) \frac{W}{dx} = 2 \mu_n \frac{L}{dx} \left( V_{\text{GS}} - V_c(x) - V_{\text{tno}} \right) \]

The voltage drop across the length dx, for a drain current I_D, is

\[ \text{Equation 3.22} \]
\[ dV_c(x) = dR_{chan}(x)I_D \]

where \( R_{chan}(x) = 1/G_{chan}(x) \). Using (3.21), the incremental voltage across \( dx \) is

Equation 3.23

\[ dV_c(x) = \frac{dx}{k_n L \left[ V_{GS} - V_c(x) - V_{tno} \right]} I_L \]

Rearranging the equation and integrating gives

Equation 3.24

\[ \frac{V_{DS}}{n} \int_0^{V_{CS} - V_c(x) - V_{tno}} dV_c(x) = \frac{I_D}{L} \int_0^L dx = I_D \]

which leads to the result (3.5), repeated here

\[ I_D = 2k_n \left[ (V_{GS} - V_{tno}) V_{DS} - \frac{V_{DS}^2}{2} \right] \]

### 3.5. Summary of Equations

<table>
<thead>
<tr>
<th>Equations for NMOS. For PMOS, reverse the order of subscripts and define ( I_D ) out of the drain.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_D = 2k_n \left( 1 + \lambda_n V_{DS} \right) \left( V_{eff} V_{DS} - \frac{V_{DS}^2}{2} \right) )</td>
</tr>
<tr>
<td>( Q_{chan} = C_{ox} \left[ V_{GS} - V_c(x) - V_{tno} \right] )</td>
</tr>
<tr>
<td>( k_n = \frac{K_{Pn} W}{2 L} )</td>
</tr>
<tr>
<td>( V_{eff} = V_{GS} - V_{tno} )</td>
</tr>
<tr>
<td>( V_{tn} = V_{tno} + \gamma_n \left( \sqrt{V_{SB}^2 + 2\phi_p} - \sqrt{2\phi_p} \right) )</td>
</tr>
</tbody>
</table>
3.6. Exercises and Projects

Project Mathcad Files  Exercise03.mc d - Project03.mcd - Exercise04.mcd, Project04.mcd

Laboratory Project 3  Characterization of the PMOS Transistor for Circuit Simulation

P3.4  Low-Voltage Linear Region of the Output Characteristic
P3.5  PMOS Parameters from the Transfer Characteristic
P3.6  PMOS Lambda from the Transfer Characteristic
P3.7  PMOS Output Characteristic
P3.8  PMOS Lambda

Laboratory Project 4  Characterization of the NMOS Transistor for Circuit Simulation

P4.4  NMOS Parameters from the Transfer Characteristic
P4.5  NMOS Lambda from the Transfer Characteristic
P4.6  NMOS Gamma SubVI
P4.7  NMOS Gamma
P4.8  NMOS Circuit with Body Effect

Unit 4. Signal Conductance Parameters for Circuit Simulation

The basic low-frequency linear model for a MOS transistor has three conductance parameters: the transconductance parameter, \( g_m \), the body-effect parameter, \( g_{mb} \), and the output conductance parameter \( g_{ds} \). They are the proportionality constants between incremental variables of current and voltage. For the linear model to be valid, the increment must be small compared to the dc (bias) value of the variable. To qualify as small, the increment must be sufficiently small, in each case, as to avoid unacceptable degrees of nonlinearity in the variable relationships. The conditions are explored in Unit 5 in connection with linearity of an amplifier gain function.

In the following, the three conductance parameters are explored, and in each case, an expression for obtaining the circuit value is developed. The discussion is based on a standard amplifier stage to provide for an association with electronic circuits.

4.1. Amplifier Circuit and Signal Equivalent Circuits

To serve as an illustration of the utility of the parameters, the discussion of the linear model and \( g \) parameters will be accompanied by a signal-performance evaluation of an NMOS transistor in the most general amplifier configuration (Fig. 4.1). The circuit includes drain and source resistors, and input is at the gate terminal. As shown in Fig. 4.1...
output can be at the drain (common-source amplifier) or source (source-follower amplifier).

**Figure 4.1.** (a) Ideal NMOS in a basic common-source amplifier circuit (output, $V_{ocs}$). Dc supply nodes of Fig. 4.1(a) are set to zero volts to obtain the signal circuits of Fig. 4.1(b) and (c). An alternative output is $V_{oef}$ [shown in (b)], which is the source-follower amplifier stage. Voltage variable $V_g$ is the input for both cases.

**Figure 4.1** shows the dc (bias) circuit (a) and signal circuit (b). Replacing all dc nodes with signal ground and replacing the dc variables with signal variables as in Fig. 4.1 produces the signal circuit. It will be assumed that the schematic symbol for the transistor in signal circuit (b) is equivalent to the ideal, intrinsic linear model of the transistor. The total drain current of the model is $I_d = g_m V_{gs}$, as, for example, in the basic circuit of Fig. 2.4. The linear equivalent model is that of Fig. 4.1(c). The symbolic transistor in Fig. 4.1(b) is more intuitively representative in terms of the overall circuit perspective than that of Fig. 4.1(c). For this reason, the Fig. 4.1(b) version is chosen for use in all of the following discussions of MOSFET circuits. All other details of the transistor model, as discussed in this unit, will be added externally.

Signal $V_g = V_i$ is applied to the gate (input) and, in response, a signal voltage, $V_o$, appears at the drain (or source). We would like to analyze the signal performance in terms of voltage gain, $a_v = V_o/V_i = V_d/V_g$ (or $a_v = V_d/V_g$), of the circuit based on a linear (small-signal) analysis. In any case, the voltage gain is $a_v = G_m R_x$, where $G_m$ is the circuit transconductance (as opposed to the transistor transconductance) and $x = D$ (common source) or $x = S$ (source follower). Thus, the goal will be to obtain a relation for $G_m$ for a given linear model of the transistor. Circuit transconductance is determined in the following for models with the various parameters included.
4.2. Transistor Variable Incremental Relationships

As illustrated previously diagrammatically, for example, in Fig. 3.2, the MOSFET is a four-terminal device. The four-terminal version of the schematic symbol is repeated here in Fig. 4.2. The terminals again are the source, drain, gate, and body. The drain current and the three terminal-pair voltages are all interdependent such that \( i_D = f(v_{DS}, v_{GS}, v_{SB}) \). Use of the three-terminal schematic symbol for the transistor, as in Fig. 4.1, conveys the assumption that the body and source are connected. For an applied incremental \( V_{gs} \), for example, there will be, in response, incremental drain current \( I_d \) and incremental voltages \( V_{ds} \) and \( V_{sb} \). The linear model is based on relating the current to the three voltages. This is

Equation 4.1

\[
I_d = \frac{\partial i_D}{\partial v_{DS}} v_{ds} + \frac{\partial i_D}{\partial v_{GS}} v_{gs} + \frac{\partial i_D}{\partial v_{SB}} v_{sb} = g_m v_{gs} + g_{ds} v_{gs} + g_{mb} v_{sb}
\]

Figure 4.2. Four-terminal NMOS schematic symbol in a common source configuration.

The linear-model representation is shown in Fig. 4.3. Figure 4.3(a) shows a current-source version. The body-effect parameter, \( g_{mb} \), is defined as positive. The minus sign is required as the partial derivative in (4.1) is negative. In Fig. 4.3(b) the body-effect current source is reversed to eliminate the minus sign, and the current source associated with \( g_{ds} \) is replaced with a resistance. The latter is possible as the voltage-dependent current source is between the same nodes as the voltage.

Figure 4.3. (a) Linear model that includes all contributions to the signal drain current, \( I_d \), as given in (4.1). The body-effect parameter, \( g_{mb} \), is a positive number such that current from the current source is in the direction opposite the arrow. (b) Current source of body effect is reversed to eliminate the minus sign, and a resistor replaces the \( g_{ds} \) current source.
In the following units, using the detailed functions (3.8) and (3.14), which relate the four variables, expressions, as used in SPICE, will be obtained for the three proportionality constants: transconductance parameter, \( g_m \), output conductance parameter, \( g_{ds} \), and body-effect transconductance parameter, \( g_{mb} \). The results will be used to obtain numerical results for the circuit transconductance, \( G_m \), for various cases.

4.3. Transconductance Parameter

The transconductance parameter, \( g_m \), was introduced in Unit 2 in the treatment on the rudimentary electronic amplifier; it is the proportionality constant of the linear relationship between the output (responding) current and the input (control) voltage \((2.3)\). For the MOSFET, NMOS, or PMOS, \( I_d = g_m V_{gs} \), where \( I_d \) is into the drain for both transistor types. An ideal transistor can be modeled with this alone. A simple model, which includes no other components, would often be adequate for making estimates of circuit performance.

To obtain an expression for \( g_m \) as a function of the general form \( i_D = f(v_{GS}, v_{DS}, v_{SB}) \) [e.g., (3.8)], we use the definition [from (4.1)]

Equation 4.2

\[
 g_m = \left. \frac{\partial i_D}{\partial V_{GS}} \right|_{V_{ds}=V_{sb}=0}
\]
Using (3.8) to express $i_D$, the resulting relation for $g_m$ is

**Equation 4.3**

$$g_m = \frac{\partial}{\partial v_{GS}} \left[ k_n (v_{GS} - v_{in})^2 \left(1 + \lambda_n V DS\right)\right] = 2k_n (v_{GS} - v_{in}) \left(1 + \lambda_n V DS\right) = 2k' n V_{effn}$$

where \( k'_n = k_n (1 + \lambda_n V_{DS}) \) \((3.7)\) and \( V_{effn} = V_{GS} - V_{in} \). Note that the use of $V_{DS}$ is consistent with the partial derivative taken with respect to $v_{GS}$, that is, $V_{ds} = 0$. Also, the use of $V_{in}$ implies that $v_{SB} = 0$. In general, $V_{SB}$ could be nonzero, although in the definition of $g_m$, $V_{sb}$ must be zero. For the case of nonzero $V_{SB}$ (bias), one substitutes for $V_{in}$ a constant $V_{in}(V_{SB})$ in the $g_m$ expression.

Alternative forms for the $g_m$ expression can be obtained from (3.8), which is, solving for $V_{effn}$,

**Equation 4.4**

$$V_{effn} = \frac{I_D}{k'_n}$$

Using (3.8), (4.3), and (4.4), $g_m$ takes on altogether three forms:

**Equation 4.5**

$$g_m = 2k'_n V_{effn} = 2\sqrt{k'_n I_D} = 2 \frac{I_D}{V_{effn}}$$

Usually, in initial design, $k_n$ replaces $k'_n$ to eliminate the $V_{DS}$ dependence without a serious penalty in accuracy.

Using the simple linear transistor model, an expression for the circuit transconductance, $G_m$, for the circuit of Fig. 4.1 will now be obtained. The input loop equation for an applied gate signal voltage, $V_g$, is

**Equation 4.6**
\[ V_g = V_{gs} + I_d R_s \]

which is, with \( V_{gs} = I_d/g_m \),

Equation 4.7

\[ V_g = \frac{I_d}{g_m} + I_d R_s = \frac{1}{g_m} \left( 1 + \frac{g_m R_s}{I_d} \right) I_d \]

and

Equation 4.8

\[ G_m = \frac{I_d}{V_g} = \frac{g_m}{1 + g_m R_s} = g_m \left( 1 + \frac{2I_d}{V_{eff}} R_s \right) \]

The far right-hand side uses (4.5). For example, for a 1-V drop across \( R_S \) and \( V_{eff} = 0.5 \) V, \( G_m = g_m/5 \). Note that the ratio of the signal voltage drop across \( R_S \) and signal voltage \( V_{gs} \) is \( g_m R_S : 1 \). The \( G_m \) concept is utilized routinely in MOSFET circuits (and BJT circuits), which gives the effective reduced transconductance, referred to \( V_g \), in the presence of the source resistor.

4.4. Body-Effect Transconductance Parameter

For circuits in which the signal \( V_{sb} \) is nonzero, there will be an additional component of \( I_d g_{mb} V_{sb} \). An example is the circuit of Fig. 4.1 but with body terminal connected to ground. This feature is added to the circuit as shown in Fig. 4.4. The proportionality constant for this case, \( g_{mb} \), is the body-effect transconductance. It is defined as

Equation 4.9

\[ g_{mb} = \left. \frac{\partial i_D}{\partial v_{SB}} \right|_{v_{gs}=v_{ds}=0} \]
Figure 4.4. Signal circuit with the addition of a current source due to the body effect. In this example, $V_b = 0$ V and $V_{sb} = I_dR_S$.

\[
\begin{align*}
R_D & \quad \downarrow \quad I_d \\
V_g & \quad \downarrow \quad V_b \\
& \quad \downarrow \quad \text{gmb \ } V_{sb} \\
R_S & \quad \downarrow \\
& \quad \downarrow
\end{align*}
\]

which is [with (3.8) and (3.14) for $i_D$ and $V_{in}$]

Equation 4.10

\[g_{mb} = \frac{\partial i_D}{\partial v_{tn}} \frac{\partial v_{tn}}{\partial v_{SB}} = -g_m \frac{V_r}{2\sqrt{V_{SB} + 2\varphi}}\]

The minus sign is consistent with a current source in the opposite direction from that of Fig. 4.4 (as shown in Fig. 4.3) as $i_D$ is defined as positive into the drain. The preference is to turn the current source around as in Figs. 4.3 and 4.4 and use positive $g_{mb}$. The result for $g_{mb}$ is a factor, $\eta$, times $g_m$, that is

Equation 4.11

\[g_{mb} = \frac{\gamma_n}{2\sqrt{V_{SB} + 2\Phi_F}} \] 
\[g_m = \eta \gamma_n\]

For $\gamma_n = 0.5$ $V^{1/2}$, $V_{SB} = 5$ V, and $2\Phi_F = 0.7$ V, $g_{mb} = 0.1g_m$ ($\eta = 0.1$). Note that $g_{mb}$ is not zero even with the source connected to the body [i.e., with $V_{SB} = 0$ in (4.11)]. However, signal $V_{sb}$ is zero in such a case, such that $g_{mb}$ does not have to be taken into account. In general, even with $V_{SB} \neq 0$ it is possible for $V_{sb} \neq 0$, in which case, $g_{mb}$ must be included.
in the model (e.g., in Project 8 on the study of the source-follower stage, at the low end of the bias current scan).

4.5. Output Conductance Parameter

The output conductance accounts for the finite slope of the output characteristic, an example of which is shown in Fig. 4.5. The plot for the SPICE formulation [(3.8)] of the active region is also shown (applicable to the device for \( V_{DS} > V_{effn} \)). Both plots are for \( V_{GS} = \) constant (i.e., \( V_{gs} = 0 \) and \( g_m V_{gs} = 0 \)).

**Figure 4.5. Output characteristics illustrating nonzero active-region slope. Also shown is the SPICE formulation for the active region. For the plots, \( \lambda_n = 1/10 \) \( V \). A possible bias point with \( I_D \) and \( V_{DS} \) is included.**

![Graph showing output characteristics with equations and current calculations](image.png)

In the ideal case, for any \( V_{DS} \) in the active region, the current is the same for a given \( V_{GS} \), and the drain current is simply \( I_D = g_m V_{gs} \). The real case, though, obviously possesses a current dependence on \( V_{DS} \). The linear model treats \( g_m \) as a constant (calculated at the bias values) and includes the effect of the nonzero slope with the output conductance, \( g_{ds} \), such that \( I_D = g_m V_{gs} + g_{ds} V_{ds} \) (without or neglecting the body effect). The circuit shown in Fig. 4.6 includes the \( g_{ds} \) component.

**Figure 4.6. Signal circuit that includes addition of the output conductance. The equivalent resistance has magnitude \( 1/g_{ds} \).**

![Signal circuit with additional output conductance component](image.png)
An expression for the output conductance is obtained from the definition

Equation 4.12

\[ g_{ds} = \frac{\partial i_D}{\partial V_{GS}} \left| V_{DS} = V_S = 0 \right. \]

Again using (3.8), the result is

Equation 4.13

\[ g_{ds} = \lambda_n k_n V_{\text{eff}}^2 \frac{(1 + \lambda_n V_{DS})}{1 + \lambda_n V_{DS}} = \lambda_n m \approx \lambda_n I_D \]

where \( V_{\text{eff}} = V_{GS} - V_{th} \) is constant and where \( I_D \) is the dc (bias) current. The last term (on the right-hand side) is the form that is generally used in practice for an initial design, as it does not require a value for \( V_{DS} \). Note that \( g_{ds} \) is not a conductance in the physical sense but has the correct dimensions and behaves in the circuit like a conductance.

We will now obtain the circuit transconductance for the case where the effect of \( g_{ds} \) is included. Upon application of an input signal, \( V_g \), a signal drain current, \( I_d \), will flow in the output circuit. This causes a signal voltage to appear across \( R_S \) and \( R_D \), which is equal to the voltage to \( V_{dr} \). That is,

Equation 4.14
\[ V_{ds} = (R_S + R_D)I_d \]

The associated current through the output resistance is thus

Equation 4.15

\[ I_{g_{ds}} = g_{ds}V_{ds} = g_{ds}\left( R_S + R_D \right)I_d \]

The effect is to reduce the current through \( R_S \) and \( R_D \) and thus reduce the circuit transconductance of the common-source amplifier stage. The output current with the current of (4.15) subtracted from the basic \( g_mV_{gs} \) is

Equation 4.16

\[ I_d = g_mV_{gs} - g_{ds}\left( R_S + R_D \right)I_d \]

which is, when solved for \( V_{gs} \),

Equation 4.17

\[ V_{gs} = \frac{1 + g_m\left( R_S + R_D \right)}{g_m}I_d \]

Again using (4.6), which is \( V_g = V_{gs} + I_dR_S \), the new circuit transconductance is

Equation 4.18

\[ G_m = \frac{g_m}{1 + g_{ds}\left( R_S + R_D \right) + g_mR_S} = \frac{g_m}{1 + \lambda_nI_D\left( R_S + R_D \right) + \frac{2I_D}{V_{eff}R_S}} \]

With a 1-V drop across \( R_S \) and a 5-V drop across \( R_D \), and with \( \lambda_n = 1/50 \) V, the new \( G_m \) is \( g_m/5.12 \), compared with \( g_m/5 \) when neglecting \( g_{ds} \) [(4.8)].
In general, the complete circuit includes, in addition, the body-effect transconductance current source of Figs. 4.3 and 4.4. The omission of this current source in Fig. 4.6 implies that \( V_{sb} = 0 \) because the source and body are connected. This connection is possible to implement in special cases such as in some of our MOSFET lab projects where only one transistor on the chip is used or for the case of a differential stage where the source of two transistors is at the same node. It is also possible to eliminate the body-effect current source by bypassing the source resistor with a bypass capacitor. The capacitor places the source at signal ground. However, in this case, the dc threshold voltage is still affected by \( V_{SB} = I_D R_S \).

In Unit 8, the circuit transconductance equivalent to (4.8) and (4.18), but which includes the body effect [(8.49)], is given as

\[
G_m = \frac{g_m}{(R_D + R_S)g_{ds} + 1 + g_m (1 + \eta)} R_S
\]

where \( \eta \) is defined in (4.11). For \( g_{ds} = 0 \) and \( \eta = 0 \), (4.19) reduces to (4.8). Note that including the body effect will in general have more effect on \( G_m \) than including \( g_{ds} \), as \( \eta \) can be on the order of 0.2. In all cases where we can calculate the circuit transconductance, \( G_m \), the magnitude of the voltage gain is obtainable from \( -G_m R_D \) (common-source stage) and \( G_m R_S \) (source-follower stage).

### 4.6. Graphical Perspective of Output Characteristics and the Load Line

The transistor output characteristics from Unit 3 and the variable increments along with their linear relationships are illustrated in Fig. 4.7. This would be applicable, for example, to the amplifier of Fig. 2.4. (As in that circuit, no body effect is included.) The circuit is biased with drain – source voltage \( V_{DS} \) and drain current \( I_D \). A positive signal \( V_g \) is applied to the gate terminal. In response, there appears drain signal voltage \( -V_d \), due to the rise in drain current. Signal voltages are with respect to the source or ground.

*Figure 4.7. Transistor output characteristics without and with input signal, \( V_g \). A solution for the drain current and drain – source voltage in both cases is the intersection between the respective characteristics and the load line of the amplifier circuit.*
The two output characteristic curves correspond to bias $V_{GS}$ only and with gate voltage $V_{GS} + V_g$. In both cases, the solution to the drain current and voltage is the intersection between the transistor characteristic curve and the load line, which is a plot of the output circuit loop equation. This is (with reference, for example, to Fig. 2.4)

Equation 4.19

$$I_d = \frac{V_{DD}}{R_D} - \frac{V_{DS}}{R_D}$$

The solution is always constrained to this straight-line equation. The solution for $v_{DS}$ with and without signal is based on (4.19) and (3.8), which is

$$I_d = k_n \left( v_{GS} - v_{TH0} \right)^2 \left( 1 + \lambda_n v_{DS} \right)$$

The combined contributions to $I_d$ associated with the two $g$ parameters is

Equation 4.20

$$I_d = g_m V_g - |g_b| V_d$$

By the nature of the load-line function, the two terms will always have opposite signs; when $V_g$ is negative, $V_d$ will be positive.
4.7. Summary of Equations

\[ g_m = 2k_n' \sqrt{V_{\text{effn}}} = 2\sqrt{k_n' I_D} = 2 \frac{I_D}{V_{\text{effn}}} \]

Transconductance.

where

\[ k_n' = k_n (1 + \lambda_n V_{DS}) \]

\[ g_m = 2k_n' V_{\text{effn}} = 2\sqrt{k_n' I_D} = 2 \frac{I_D}{V_{\text{effn}}} \]

Approximate transconductance.

where

\[ V_{\text{effn}} = \sqrt{\frac{I_D}{k_n'}} \]

\[ G_m = \frac{I_d}{V_g} = \frac{g_m}{1 + g_m R_S} \]

Amplifier circuit transconductance with a source resistance.

\[ g_{mb} = \frac{\gamma_n}{\sqrt{V_{SB} + 2\Phi_F}} = g_m \]

Body-effect transconductance.

\[ g_{ds} = \frac{\lambda_n I_D}{1 + \lambda_n V_{DS}} \]

Output conductance.

\[ g_{ds} = \lambda_n I_D \]

Approximate output conductance.

\[ G_m = \frac{g_m}{1 + g_{ds}(R_S + R_D) + \beta_m R_S} \]

Amplifier circuit transconductance with \( g_{ds} \) included.

Subscripts are for NMOS. All equations are the same for PMOS with "p" subscript substitution and subscript-order reversal for bias-voltage variables.

Unit 5. Common-Source Amplifier Stage

Two types of common-source amplifiers will be investigated in lab projects. One is with the source grounded and the other is with a current-source bias (dual power supply). In Units 5.1 and 5.2 we discuss various aspects of the common-source stage with grounded source, in Unit 5.3 we take up circuit-linearity considerations, and in Unit 5.4 we cover the basics of the dual-power-supply amplifier. Both amplifiers are based on the PMOS, as in the projects. The first two units are mostly a review of the basic amplifier as presented in previous units, to reinforce the basic concepts. The PMOS replaces the NMOS (Units 2 and 4) in this unit, to provide familiarity with the opposite polarity in bias considerations and to illustrate that the linear model applies in the same manner for both transistor types.
5.1. DC (Bias) Circuit

Dc circuits for the grounded-source amplifier are shown in Fig. 5.1 (PMOS). The circuit in (a) is based on a single power supply, and the gate bias is obtained with a resistor voltage-divider network. The circuit in (b) is for a laboratory project amplifier. Both $V_{GG}$ and $V_{SS}$ are negative, since the source is at ground. There is no voltage drop across $R_G$ since there is negligible gate current. $R_G$ is necessary only to prevent shorting the input signal, $V_i$. The bias current $I_D$ for a given applied $V_{SG}$ will respond according to (3.8), which is

$$I_D = k_p (V_{SG} - V_{ip0})^2(1 + \lambda_p V_{SD})$$

Figure 5.1. Basic PMOS common-source amplifiers. Single-power-supply amplifier (a) and laboratory amplifier (b) with $V_{SG} (= V_{GG})$ and $V_{SS}$ controlled by DAQ output channels. Note that either end of the circuit of (a) can be at ground.

The two circuits are equivalent, as $V_{GG}$ and $R_G$ of Fig. 5.1b are the Thévenin equivalent of the bias network of the Fig. 5.1(a). In the project on the amplifier, they are actually a voltage and a resistor. This is not a bias-stable circuit, as a slight change in $V_{SG}$ or the transistor parameters can result in a significant change in $I_D$. The dual-power-supply circuit of Unit 5.4 is considerably better in this respect.

5.2. Amplifier Voltage Gain

This dc (bias) circuit becomes an amplifier now simply by adding a signal source at the gate as in Fig. 5.2. This requires a coupling capacitor, as shown here in the complete circuit, to prevent disturbing the bias upon connecting the input signal to the circuit.

Figure 5.2. A signal source is connected to the gate through a coupling capacitor. The capacitor is necessary to isolate the dc circuit from the signal source.
In the amplifier of Project 5, the signal will be superimposed on the bias voltage at the node of $V_{GG}$. This can be facilitated with LabVIEW and the DAQ. A capacitor, as in an actual amplifier, is therefore not required. The requirement for having LabVIEW control over both $V_{GG}$ and $V_{SS}$, and the limitation of two output channels, dictates this configuration.

In Project 5 we measure the gain as a function of bias current, $I_D$. For a SPICE comparison, we need an expression for the gain. For the ideal case, which neglects the output conductance, $g_{ds}$, the output current is related to the input voltage by (4.1), which is

$$I_d = g_m V_{gs} = g_m V_i$$

The output signal voltage is, in general,

Equation 5.1

$$V_{ds} = V_o = -I_D R_D$$

The convention used here for subscript order for signal (linear) variables is common to the NMOS and PMOS. This is consistent with the fact that the linear model does not distinguish between the two types. Thus, for example, the dc terminal voltage for a PMOS is $V_{SG}$, but the signal equivalent is $V_{gs}$ (Fig. 5.3) and the signal input voltage is positive at the input terminal (common-source, gate input). For the PMOS, $i_D$ is defined as positive out of the drain, but the signal output current is into the drain (as in the NMOS). We note that a positive $V_{gs}$ ($V_{gs} = -V_{sg}$) corresponds to a decrease in the total gate – source voltage, $v_{SG}$, which is consistent with a decrease of $i_D$ and positive $I_d$. 
Figure 5.3. Signal-equivalent version of the amplifier stage. Dc nodes are set to zero volts (circuit reference). The reactance of \( C_g \) is assumed to be zero.

Thus, the negative sign in (5.1) is consistent with the flow of current \( I_d \) up through the resistor (Fig. 5.3) for positive \( V_i = V_{gs} \). The common-source stage is an inverting amplifier and has an inherent 180° phase shift. From (4.1) and (5.1), the gain is

Equation 5.2

\[
a_v = \frac{V_o}{V_i} = -g_m R_D
\]

where both \( V_i = V_{gs} \) and \( V_o = V_{ds} \) are with respect to ground or the source terminal for the common-source stage.

If the output resistance, \( 1/g_{ds} \), cannot be neglected (which is the case for the project on PMOS amplifiers), the transistor current, \( g_m V_i \), is shared between the output resistance and \( R_D \). The portion that flows through \( R_D \) is (Fig. 5.4)

Equation 5.3

\[
I_{R_D} = g_m V_i \frac{1}{1 + g_m R_D}
\]

Figure 5.4. Common-source amplifier stage signal circuit, with all dc nodes set to zero volts. The transistor model includes output resistance \( 1/g_{ds} \), which appears directly in parallel with \( R_D \) with the source grounded.
Note again that the signal schematic transistor represents a current source with value $g_m V_i$, as established in connection with Fig. 4.1. The additional feature of the transistor model is included with the addition of $1/g_{ds}$. This resistance is actually part of the transistor and is between the drain and source of the transistor, but the circuit as given is equivalent, as the source is at ground. Since the output voltage is $V_o = -I_{RD}R_D$, the new gain result is

Equation 5.4

$$a_v = -g_m \frac{R_D}{1 + g_{ds}R_D}$$

Note that this form evolves from ideal transistor current, $g_m V_{gs}$, flowing through the parallel combination of the output resistance and $R_D$.

To facilitate an intuitive grasp of the magnitude of the effect of $g_{ds}$, we use the expression for $g_{ds}$ (4.13) in (5.4), to obtain

Equation 5.5

$$a_v = -g_m \frac{R_D}{1 + \lambda_p I_D R_D}$$

Note that $I_D R_D$ is the voltage drop across $R_D$. For example, for a $-10$-V power supply, we choose $I_D R_D \approx 5$ V. A measurement of $\lambda_p$ for our devices will show that $\lambda_p \approx 1/20$ V, which results in $\lambda_p I_D R_D \approx 1/4$. Thus, the effect of $g_{ds} (= \lambda_p I_D)$ for this case is significant.

Finally, we can get an overall current dependence for $a_v$ with the elimination of $g_m$, using (4.5) with $k_p = k_p \approx k_p$, which results in
Equation 5.6

\[ a_{VO} = -2 \sqrt{\frac{k_p I_D}{1 + \lambda_p I_D R_D}} \frac{R_D}{1 + \lambda_p I_D R_D} \]

Using an alternative form for \( g_m (= 2I_D/V_{effp}) \), also (4.5), the gain expression is

Equation 5.7

\[ a_v = -2 \frac{I_D R_D}{V_{effp} (1 + \lambda_p I_D R_D)} \]

where

\[ V_{effp} = \sqrt{\frac{I_D}{k_p (1 + \lambda_p V_{SD})}} \approx \sqrt{\frac{I_D}{k_p}} \]

For simplicity, approximate forms of (4.5) and (4.13) of \( g_m \) and \( g_{ds} \) are used here, which are independent of \( V_{SD} \). For reference, the "exact" and approximate forms of (4.5) and (4.13), respectively, are repeated here:

\[ g_m = 2 \sqrt{k_p (1 + \lambda_p V_{SD})} I_D \approx 2 \sqrt{k_p} I_D \]

and

\[ g_{ds} = \lambda_p \frac{I_D}{1 + \lambda_p V_{SD}} \approx \lambda_p I_D \]

The "exact" equations of \( g_m \) and \( g_{ds} \) are used in conjunction with the amplifier projects to compare the computed gain with the measured gain plotted against \( I_D \). This is done in both LabVIEW and Mathcad. Parameters \( k_p \) and \( V_{spo} \) (to get \( V_{effp} \)) will be extracted from the measured dc data, and \( \lambda_p \) will be used as an adjustable parameter to fit the SPICE and measured gain data.
5.3. Linearity of the Gain of the Common-Source Amplifier

The connection between $I_d$ and $V_{gs}$ is linear provided that $V_{gs}$ is small enough, as considered in the following units. Use of the linear relations also assumes that the output signal remains in the active region (i.e., neither in the linear region nor near cutoff). This is discussed below. NMOS subscripts are used. The results are the same for the PMOS, with a "p" subscript substituted for "n" and the subscript order reversed for all bias-voltage variables.

5.3.1. Nonlinearity Referred to the Input

The general equation again is (3.8)

\[ i_D = k'_z \left( V_{GS} - V_{to} \right)^2 \]

Then using $I_d = i_D - I_D$ and $V_{GS} = V_{GS} + V_{gs}$, the equation for the incremental drain current becomes

Equation 5.8

\[ I_d = k'_z \left[ 2 \left( V_{GS} - V_{to} \right) V_{gs} + V_{gs}^2 \right] \]

which leads to a nonlinear (variable) transconductance, $g'_m$, given by

Equation 5.9

\[ g'_m = \frac{I_d}{V_{gs}} = \frac{k'_n \left( 2V_{eff} V_{gs} + V_{gs}^2 \right)}{V_{gs}} = g_m \left( 1 \pm \frac{V_{gs}}{2V_{eff}} \right) \]

Therefore, the condition for linearity is that $V_{gs} \ll 2V_{eff}$, with $V_{eff} = V_{GS} = V_{to}$ and using

With this condition not satisfied, an output signal is distorted. However, for the purpose of measuring the amplifier gain, our signal voltmeter will take the average of the positive and negative peaks, which is

Equation 5.10
In the parabolic relationship, the squared terms cancel entirely. In general, though, the output signal contains harmonic content (distortion) when $V_{gs}$ is too large compared to $V_{effn}$.

5.3.2. Nonlinearity Referred to the Output

The discussion above of limits imposed on $V_{gs}$ assumes that the transistor remains in the active mode. To clarify this point, reference is made to the output characteristics of Fig. 5.5. The graph has plots of the output characteristic for three values of $v_{GS}$ in addition to the load line. The characteristic plot in the midrange is for no signal. Operating point variables are $V_{DS} \approx 2.5$ V and $I_{D} \approx 40 \mu A$. With a large, positive $V_{gs}$, the characteristic moves up to the high-level plot ($i_{Dhi}$) and the opposite occurs for a large but negative $V_{gs}$ ($i_{Dlo}$). The high-level plot is shown for when the transistor is about to move out of the active region and into the linear region. Attempts to force $V_{DS}$ to lower values will create considerable distortion in the output signal voltage. The lower curve suggests that the positive output signal is on the verge of being cut off (clipped) for an additional increase in the negative-input signal voltage.

Figure 5.5. Common-source amplifier stage output characteristics. Output characteristics are from top to bottom, large high-current signal swing, $i_{Dhi}$, dc bias, $I_{D}$, low-current signal swing, $i_{Dlo}$. Also shown is the load line. The current – voltage circuit solution is always the intersection between a given characteristic and the load line.

According to the discussion above, the negative signal output voltage is limited to
Equation 5.11

\[ V_{\text{dsmin}} = V_D - V_{\text{effn}} \]

Technically, \( V_{\text{effn}} \) is from the high-current signal state, but for simplicity, a reasonable estimate can be made from the dc case; that is, \( V_{\text{effn}} = V_{GS} - V_{tho} \). The positive signal limit is

Equation 5.12

\[ V_{\text{dsplus}} = V_{DD} - V_D = I_D R_D \]

The actual output-signal limit is dictated by the smaller of the two for a symmetrical periodic signal such as a sine-wave. In the example shown in Fig. 5.5, \( V_{\text{effn}} \approx 0.5 \) V, \( V_D \approx 2.5 \) V, and \( V_{DD} = 5 \) V. The plus and minus signal-voltage limits are about 2.5 V and 2.0 V, respectively. Depending on the dc bias, the limit could be dictated by one or the other. In the amplifier projects, the gain will typically be measured over a range of dc bias current for a fixed resistor. This means that for the low-current end of the scan, the signal will be limited by the magnitude of \( I_D R_D \) and, by design, the plus and minus swings will be made to be about equal at the highest dc current.

Distortion associated with the nonlinear \( I_D - V_{gs} \) relation and that due to signal limits at the output may be taking place simultaneously. This is seen from the gain expression (5.7) \((g_{ds} = 0)\)

\[ |a_v| \approx 2 \frac{V_{Ro}}{V_{\text{effp}}} \]

where \( a_v \equiv V_{ds}/V_{gs} \) and where the approximation is for the case of neglecting the \( \lambda_n \) factor. Thus, for a given \( V_{ds} \), \( V_{gs} \) is

Equation 5.13

\[ V_{gs} = \frac{V_{\text{effp}}}{2V_{Ro}} V_{ds} \]
If, for example, $V_{ds}$ is pushed to the positive output-signal limit, then $V_{ds} = V_{RD}$. According to (5.13), $V_{gs} = V_{eff}/2$, and $V_{gs}$ exceeds the condition for a linear $I_d - V_{gs}$ relation as given in (5.9),

$$g_m = \frac{I_d}{V_{gs}} = g_m \left(1 \pm \frac{|V_{gs}|}{2V_{eff}}\right)$$

5.4. Current-Source Common-Source Amplifier: Common-Source Amplifier with a Source Resistor

The bias circuit of the current-source bias amplifier, shown in Fig. 5.6, has a dual power supply. One advantage of this is that the input is at zero dc volts such that the signal can be connected directly without interfering with the bias. The dc circuit equation for setting up the bias is

Equation 5.14

$$I_D = \frac{V_{DD} - V_{SG}}{R_S}$$

where $(k_p' \approx k_p) V_{SG} \approx \sqrt{I_D/k_p} + V_{tp}$.

This circuit is more bias stable than the grounded source amplifier, as slight changes in $V_{sg}$ (due to device parameter variations or temperature) are usually small compared to $V_{DD}$. Note that $V_{tp}$ is used in lieu of $V_{tpo}$ as $V_{BS} \neq 0$. The chip (CD4007) used in the projects is a p-well device (as noted in Unit 3), with the NMOS transistors in the well. The well is connected to $V_{SS}$, while the body of the chip is connected, as in Fig. 5.6, to $V_{DD}$. The pn junction formed by the well and the bulk is thus reverse-biased with a voltage $|V_{SS}| + V_{DD}$.

**Figure 5.6.** Dc circuit of the dual-power-supply common-source amplifier. The gate is at ground potential, allowing the signal to be connected directly to the gate. $R_G$ is necessary only to prevent shorting out the input signal.
In the amplifier projects, however, we have the latitude to connect the body and source as there is only one transistor in the circuit and the body can float along with the source. Thus we can assume that $V_{tp} = V_{tpo}$. As shown in Fig. 5.7, the signal circuit requires the addition of a bypass capacitor, $C_s$. This places the source at signal ground provided that the capacitor is large enough. The criterion for this is discussed in Unit 6. The voltage-gain equation is the same as in the amplifier, with the source actually grounded.

**Figure 5.7. Amplifier circuit with a bypass capacitor attached between the source and ground to tie the source to signal ground. Signal input is attached directly to the gate. Body and source are connected internally in the project chip for the transistor used in the amplifier.**

Without the bypass capacitor, $R_s$ is in the signal circuit and a fraction of the applied signal voltage at the gate is dropped across the resistor. The signal circuit for this case is
shown in Fig. 5.8. The circuit transconductance of the amplifier with $R_S$ was discussed initially in Unit 4. This is reviewed in the following.

An applied input signal, $V_i = V_g$, divides between the gate – source terminals and the source resistor according to \((4.6)\)

$$V_g = V_{gs} + I_d R_S$$

**Figure 5.8. Signal circuit for dual-power supply common-source amplifier. Input signal voltage, $V_I$, is divided between $V_{gs}$, the control voltage, and the source resistor according to the ratio 1: $g_m R_S$.**

When combing this with $I_d = g_m V_{gs}$, we obtain \((4.7)\)

$$V_g = V_{gs} + g_m V_{gs} R_S = (1 + g_m R_S) V_{gs} = (1 + g_m R_S) \frac{I_d}{g_m}$$

The circuit transconductance, $G_m$, is then \((4.8)\)

$$G_m = \frac{I_d}{V_g} = \frac{g_m}{1 + g_m R_S}$$

The gain for this case is thus (neglecting $g_{ds}$)

Equation 5.15
In one of the amplifier projects, \( R_S = R_D \), and the gain without the bypass capacitor is actually less than unity.

### 5.5. Design of a Basic Common-Source Amplifier

Unlike in the laboratory environment, an actual practical common-source amplifier would have a single power supply for the base and collector circuit bias. Also, the circuit design requires a tolerance to a wide range of parameter variation, including that due to temperature change. In this unit, the design process for a possible common-source amplifier is discussed. Emphasis is on dc bias stability, that is, on tolerance to device parameter and circuit component variations.

The common-source amplifier to be designed is shown in Fig. 5.9. Source resistor, \( R_S \), is included for bias (and gain) stabilization. The goal is for the circuit to function properly for any NMOS transistor, which has device parameters \( k_n \) and \( V_{tno} \) that fall into a wide range of values, as is normally expected. Tolerance to component variation, such as resistor values, could also be built into the design.

**Figure 5.9.** NMOS common-source amplifier with \( R_S \) for bias and gain stabilization. Gate bias is provided by a voltage-divider network consisting of \( R_{G1} \) and \( R_{G2} \). The body and source terminals are connected.

Gate voltage \( V_{G1} \) is provided by the voltage divider, consisting of resistors \( R_{G1} \) and \( R_{G2} \). Since there is no gate current, the gate bias voltage is \([1.2]\)
Voltage $V_G$ is thus relatively stable and can be considered constant. Once $V_G$ has been established, the drain current will be dictated by

Equation 5.16

$$I_D = \frac{V_G - V_{GS}}{R_S}$$

Since the gate – source voltage is given by

Equation 5.17

$$V_{GS} = \sqrt{\frac{I_D}{k_n}} + V_{tno}$$

the drain current, $I_D$, may be expressed in terms of the device parameters as

Equation 5.18

$$I_D = \frac{V_G - \sqrt{\frac{I_D}{k_n}} - V_{tno}}{R_S}$$

This result reveals the dependence of $I_D$ on the magnitudes of $k_n$ and $V_{tno}$. (Again, for simplicity, as in the amplifier projects, we will assume that the body and source are connected such that $V_m = V_{tno}$.)

Bias current $I_D$ is assumed to be a given. The initial design then is conducted for the NMOS nominal, average values for $k_n$ and $V_{tno}$. Any combination of $V_G$ and $R_S$ that satisfies (5.18) will provide the design $I_D$. Specific values for $V_G$ and $R_S$ will be dictated by stability requirements. Suppose that $k_n$ is expected to fall within $k_{no} \pm \delta k_n$ and $V_{tno}$ within $V_{tnoo} \pm \delta V_{tno}$, where $k_{no}$ and $V_{tnoo}$ are the nominal values of the original design. Assume that the design bias current associated with $k_{no}$ and $V_{tnoo}$ is $I_{D0}$. At the extremes for the parameters, the low and high currents will be
Equation 5.19

\[
I_{D_{\text{Do,hi}}} = \frac{V_G - \sqrt{\frac{I_D}{k_n \pm \delta k_n} - (V_{tno} \pm \delta V_{tno})}}{R_S}
\]

Resistor \( R_S \), for the given \( V_G \) and design drain current, is

Equation 5.20

\[
R_S = \frac{V_G - V_{GSo}}{I_{D_0}}
\]

\( V_{GSo} \) is obtained from (5.17), using the nominal parameter values. The low and high current limits tend to converge on \( V_G/R_S \) as \( V_G \) becomes large. That is, in the limit, \( V_G \) dominates the voltages in the numerator of (5.19), thus rendering the expression insensitive to the minor contributions from changes in \( k_n \) and \( V_{tno} \).

An important design consideration is drain – source voltage, \( V_{DS} \), as this dictates the output signal range. This is calculated from

Equation 5.21

\[
V_{DS} = V_{DD} - I_D \left( V_D + R_S \right)
\]

In the design of the amplifier, drain resistor \( R_D \) is normally selected for equal positive and negative peak-signal maximums. This configuration is illustrated in Fig. 5.10, which shows the output characteristic of the transistor in the circuit. The signal is limited by \( V_{DD} - V_{RS} \) and \( V_{effno} = V_{GSo} - V_{tno} \) at the high and low ends of the voltage range, respectively. Therefore, nominal bias should be set at

Equation 5.22

\[
V_{DSo} = \frac{V_{DD} - I_{D0}R_S + V_{effno}}{2}
\]

Figure 5.10. Output characteristic of the transistor of the amplifier with bias \( V_{DS} \) set approximately according to (5.22). The signal is restricted within the range
$V_{DD} - V_{RS}$ and approximately $v_{eff}$. The characteristic curves are for no signal (solid plot) and for the signal at a maximum (dashed plot), as limited by the transistor going into the inactive (linear) region. The load lines are dc (solid line) and signal (ac, dashed line).

For simplicity, it is assumed that $v_{eff} \approx V_{effno}$. $V_{effno}$, $V_{DDo}$, and $I_{Do}$ are the bias values at the nominal parameter values. The bias drain voltage is $V_{DS0}$ plus the drop across $R_S$, that is,

\begin{equation}
V_{Do} = V_{DS0} + I_{Do}R_S
\end{equation}

Knowing $V_{Do}$ then provides for the calculation of $R_D$ from

\begin{equation}
R_D = \frac{V_{DD} - V_{Do}}{I_{Do}}
\end{equation}

where $V_{Do}$ and $I_{Do}$ are for the initial design with $k_{no}$ and $V_{tnoo}$.

An optimization design sequence plots the limits for a range of $V_G$ and for specified $\delta V_{tno}$ and $\delta k_n$. An example is shown in Fig. 5.11. The plot of $V_{DS0}$ corresponds to the nominal $k_{no}$ and $V_{tnoo}$. The curve slopes downward as $I_S R_S$ increases for increasing $V_G$ at constant nominal bias current, $I_{Do}$. $V_{DShi}$ is for the combination of $\delta V_{tno}$ and $\delta k_n$, which gives the
maximum positive deviation from the nominal, and $V_{DSlo}$ is the opposite. The example of Fig. 5.11 is for $V_{DD} = 10\ \text{V}$ and design bias current of $I_{Do} = 100\ \mu\text{A}$ and nominal parameters $k_{no} = 300\ \mu\text{A/V}^2$, $V_{tnoo} = 1.5\ \text{V}$, $\delta V_{tno} = 0.1\ \text{V}$, and $\delta k_{n} = 100\ \mu\text{A/V}^2$.

Experience with the CMOS chip of our amplifier project (Project 7) indicates that these are representative.

Figure 5.11. Computed high and low range of $V_{DS}$ as a function of gate-bias voltage $V_{G}$. The computation is with $k_{no} = 300\ \mu\text{A/V}^2$, $V_{tnoo} = 1.5\ \text{V}$, $\delta V_{tno} = 0.1\ \text{V}$, and $\delta k_{n} = 100\ \mu\text{A/V}^2$.

Figure 5.12 shows plots of the computed positive and negative signal-peak limits. Due to the increasing $V_{RS}$ with increasing $V_{G}$, the signal range decreases, as shown by the plots. Thus, the signal-peak limits have a maximum, as is evident in the graph. The design of the amplifier uses $V_{G}$ at the maximum of the lower curve. The value of $V_{G}$ is consistent with the maximum $V_{DSlo}$ in the plot of Fig. 5.11. In the example, $V_{G} = 3\ \text{V}$.

Figure 5.12. Computed maximums for negative and positive output voltage signal peaks as a function of $V_{G}$: $V_{dplus}$, positive maximum; $V_{dminus}$, negative maximum.
Once $V_G$ is determined, the selection of $R_{G1}$ is made from (1.2), which is

$$V_G = \frac{R_G}{R_G + R_{G1}} V_{DD} = \frac{R_G}{R_{G1}} V_{DD}$$

where $R_G$ is the parallel combination

$$R_G = \frac{R_{G2} R_{G1}}{R_{G2} + R_{G1}}$$

$R_G$ can be selected somewhat arbitrarily but could be dictated by the coupling capacitor, $C_G$, requirement. Associated with the coupling capacitor is the 3 - dB frequency (6.2), which is

$$f_{3dB} = \frac{1}{2\pi R_G C_G}$$

$R_{G2}$ is then calculated from

$$R_{G2} = \frac{R_{G1} R_G}{R_{G1} - R_G}$$
The gain equations for the circuit of Fig. 5.9, with and without a bypass capacitor, are (5.2) and (5.15), respectively. These are

\[ a_v = -g_m R_D \]

and

\[ a_v = -\frac{g_m R_D}{1 + g_m R_S} \]

In the design procedure outlined in this unit, emphasis is on stability and the gain falls out. This would typically be the case for this type of amplifier. We note that due to the characteristically small \( g_m \) of MOSFETs, the voltage gain is relatively small. Gain can be improved considerably through the use a current-source load, as in the amplifier of Unit 10.

### 5.6. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
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<tbody>
<tr>
<td>( a_v = -g_m R_D )</td>
<td>Common-source amplifier-stage voltage gain.</td>
</tr>
<tr>
<td>( a_v = -g_m \frac{R_D}{1 + \lambda_p I_D R_D} )</td>
<td>Common-source amplifier gain including output resistance, PMOS. (Same for NMOS with ( \lambda_m ).)</td>
</tr>
<tr>
<td>( g_m' = g_m \left( 1 \pm \frac{V_{gs}}{2V_{eff}} \right) )</td>
<td>Nonlinear transconductance for large input signals. (Same for PMOS with ( V_{effp} ).)</td>
</tr>
<tr>
<td>( V_{ds minus} = V_{DS} - V_{effn} )</td>
<td>Negative output signal limit, NMOS.</td>
</tr>
<tr>
<td>( V_{ds minus} = V_{SD} - V_{effn} )</td>
<td>Negative output signal limit, PMOS.</td>
</tr>
<tr>
<td>( V_{ds plus} = V_{DD} - V_{DS} = I_D R_D )</td>
<td>Positive output signal limit, NMOS.</td>
</tr>
<tr>
<td>( V_{ds plus} =</td>
<td>V_{SS}</td>
</tr>
<tr>
<td>( a_v = -\frac{g_m R_D}{1 + g_m R_S} )</td>
<td>Voltage gain of common-source stage with source resistor.</td>
</tr>
<tr>
<td>( g_m = \frac{g_m}{1 + g_m R_S} )</td>
<td>Circuit transresistance of common-source stage with source resistor.</td>
</tr>
</tbody>
</table>

### 5.7. Exercises and Projects

**Project Mathcad Files**
- Exercise05.mcd - Project05.mcd

**Laboratory Project 5**
- **PMOS Common-Source Amplifier**
Unit 6. Coupling and Bypass Capacitors and Frequency Response

As noted in Unit 1, due to the external capacitors that are attached to the circuit for configuring the signal circuit, the gain of the amplifiers will tend to fall off at the low-frequency end of the frequency spectrum. The design basis for choosing the capacitors for a given application is considered in the following. The gain-frequency dependence due to the input coupling capacitor, the source-resistor bypass capacitor, and the load coupling capacitor is discussed. A discussion of response roll-off on the high end of the spectrum is deferred to Unit 11.

6.1. Grounded-Source Amplifier: Coupling Capacitor

A version of the circuits of Fig. 5.2, as given in Fig. 6.1, is generalized to include a resistance, $R_s$, as part of the input signal source. The input signal at the gate (and thus the output) will fall off for decreasing frequencies as the magnitude of reactance of the capacitor increases. The value of the capacitor is selected such that the reactance will be small compared to the value of the sum of the resistors, at the lowest operating frequency.

Figure 6.1. Circuit with coupling capacitor. Capacitor blocks the signal at low frequencies. $C_g$ and $R_G = R_{G1} \parallel R_{G2}$ must be selected for $|X_{Cg}| << R_s + R_G$ at the gain measurement frequency.
In this amplifier, all the gain-frequency dependence is between \( V_g \) and \( V_s \). The relation between the gate signal, \( V_g \), and source signal, \( V_s \), based on a voltage-divider relation is

Equation 6.1

\[
V_g = \frac{R_g}{R_g + R_s + \frac{1}{2\pi f C_g}} V_s = \frac{R_g}{R_g + R_s} \left( 1 - \frac{j}{f} f_g \right) V_s
\]

with

Equation 6.2

\[
f_g = f_{3\text{dB}} = \frac{1}{2\pi (R_g + R_s) C_g}
\]

where \( R_G = R_{G1} \parallel R_{G2} \).

With \( R_s \) included, the \( f_{3\text{dB}} \) expression applies to an actual amplifier. In Project 6, the signal-source voltage is applied directly to the gate. We select a combination of \( R_G \) and \( C_g \) to obtain a suitably low \( f_{3\text{dB}} \). This must be more than a factor of 10 lower than the gain measurement frequency assure that the capacitor is not influencing the measurements.

In Projects 5 and 7, no capacitor is used at the input as the signal is superimposed on the dc gate voltage. This is to facilitate the need for both DAQ output channels to provide the bias. However, Project 6, one channel provides the bias, as in Figs. 5.1(a) and 6.1, and the other channel is used for the signal with connection to the input through a coupling capacitor.

### 6.2. Current-Source Bias Amplifier: Bypass Capacitor

The PMOS common-source amplifier circuit with the bypass capacitor is shown in Fig. 6.2. At some low frequency, the effect of the capacitor is absent, and the gain is computed from (5.15), which is

\[
a_v = -\frac{g_m R_D}{1 + g_m R_S}
\]
Figure 6.2. Dual-power-supply common-source amplifier stage with bypass capacitor. The object is to determine the frequency for which the source is effectively at signal ground.

Over a range of frequencies, the gain evolves from (5.15) to (5.2), $a_v = -g_m R_D$ (neglecting the output resistance of the PMOS). The frequency-dependent transition region is determined by replacing $R_S$ in (5.15) with the impedance of $R_S$ in parallel with the reactance of $C_s$. This is

Equation 6.3

$$a_v(f) = -\frac{g_m R_D}{1 + g_m \frac{R_S}{1 + j2\pi f R_S C_s}}$$

or

Equation 6.4

$$a_v(f) = -\frac{g_m R_D \left(1 + \frac{f}{f_0}\right)}{1 + j \frac{f}{f_0} + g_m R_S} = -\frac{g_m R_D}{1 + g_m R_S} \frac{1 + j \frac{f}{f_c}}{1 + j \frac{f}{f_c}}$$

with

Equation 6.5
\[ f_z = \frac{1}{2\pi R_S C_s} \]

and

Equation 6.6

\[ f_s = \frac{1}{2\pi R_S \frac{1}{1 + g_m R_S}} \cdot \frac{1}{C_s} = (1 + g_m R_S) f_z \]

Note that the "RC" factor has an "R,", which is R_S in parallel with 1/g_m, the latter being the output resistance looking into the source of the transistor. The two frequencies f_s and f_z are technically the pole and zero of the response function.

We note that g_m R_S = 2I_D R_S / V_{eff}. Since V_{eff} could be as low as V_{eff} = 0.2 V, then g_m R_S >> 1 in some cases. The corner frequency, f_{3dB}, occurs at

Equation 6.7

\[ a_{v_{3dB}} = \frac{g_m R_D}{\sqrt{2}} - \frac{g_m R_D}{1 + g_m R_S} \left( \frac{f_{3dB}}{f_z} \right)^2 = g_m R_D \sqrt{\frac{f_z^2 + f_{3dB}^2}{f_z^2 + f_{3dB}^2}} \]

which gives

Equation 6.8

\[ f_{3dB} = \sqrt{f_z^2 - 2f_z^2} = \sqrt{(1 + g_m R_S)^2 f_z^2 - 2f_z^2} = \sqrt{(1 + g_m R_S)^2 - 2} f_z \approx f_z \]

such that

Equation 6.9
where the far-right-hand term applies for \( g_m R_s \gg 1 \). This is typically only marginally satisfied in MOSFET circuits.

The derivation carried out here was initiated from (5.15), which neglects the output resistance of the transistor. In the case of the MOSFET devices of our projects, the simplification is valid for the NMOS transistor but marginal for the PMOS transistor. This is because \( \lambda_p \gg \lambda_n \). The result (6.9) still serves to estimate the required value for \( C_s \), even for the case of the PMOS. Nevertheless, a more detailed derivation is carried out in the next unit. This permits comparisons, in a project, of SPICE and Mathcad solutions with amplifier gains and frequency response.

### 6.3. Precision Formulation of the Low-Frequency Gain and Characteristic Frequencies

In Unit 8, the gain of a common-source stage with source resistor, which includes the effect of the output resistance, is shown to be \([8.36]\)

\[
a_{\text{volo}} = \frac{-g_m R_D}{1 + g_d R_D + (g_m + g_d) R_s}
\]

This is designated here as \( a_{\text{volo}} \) to emphasize that it is the constant low-frequency asymptotic gain. If the source-branch impedance is substituted for \( R_s \), this becomes

\[
a_v(f) = \frac{-g_m R_D}{1 + g_d R_D + (g_m + g_d) \frac{R_s}{1 + j \frac{f}{f_z}}}
\]

where \( f_z \) is (6.5). This can be rearranged in the form of (6.4), which is

\[
\]
where the new pole frequency is

Equation 6.12

\[ f_s = \left[ 1 + \frac{(g_m + g_{ds})R_S}{1 + g_{ds}R_D} \right] f_z \]

and \( a_v \) is (8.36).

6.4. Load Coupling Capacitor

The complete practical amplifier includes a load, \( R_L \), at the output. This requires an additional coupling capacitor. The amplifier with an attached load is shown in Fig. 6.3. We will assume that the effect of the output resistance, \( r_{ds} \), can be neglected. The transistor appears as a current source of magnitude \( I_d \). The equivalent signal circuit at the output can be represented as shown in Fig. 6.4(a) and (b). In Figure 6.4(b), the current source and drain resistor are replaced with a voltage-source equivalent. From Fig. 6.4(b), the output voltage is

Equation 6.13

\[ V_o(f) = \frac{R_L}{R_D + R_L + 1/2\pi fC_d} I_d R_D \]

Figure 6.3. Amplifier with capacitively coupled load resistor, \( R_L \). The capacitor must be large enough not to attenuate the output between the drain and load resistor.
The expression with the high-frequency asymptotic value and frequency dependence is

Equation 6.14

\[ v_o(f) = \frac{R_D R_L I_d}{R_D + R_L} \frac{1}{1 + 1/j2\pi f C_d (R_D + R_L)} \]

which is

Equation 6.15

\[ v_o(f) = \frac{R_L R_D}{R_D + R_L} I_d \frac{1}{1 + f_d / f} \]

where

Equation 6.16

\[ f_d = \frac{1}{2\pi (R_D + R_L) C_d} \]

**Figure 6.4.** (a) Equivalent circuit consisting of a current source and the load components. (b) Conversion of current source to voltage source.
Current source $I_d$ is not dependent on frequency (at the low end of the spectrum) when no other capacitors are considered. However, in general, with both $C_d$ and $C_s$ attached, the combined response is

Equation 6.17

$$a_v(f) = -\frac{g_m R_D}{1 + g_m R_S} \frac{1 + j \frac{f}{f_z}}{\left(1 + j \frac{f}{f_z}\right) \left(1 + j \frac{f}{f_d}\right)}$$

where $f_d$ is (6.16), $f_z$ is (6.5), $f_s$ is (6.6), and $R_D$ is in parallel with $R_L$. With $C_d = C_s$, usually $f_d << f_s$ such that (6.9) is the approximate $f_{3dB}$ for the circuit with both capacitors connected.

Combining the frequency-dependent terms to obtain (6.17) assumes that current source $I_d$ is independent of components $C_d$, $R_D$, and $R_L$. This is a correct assumption as long as the output resistance of the transistor is neglected. When better precision is required, the derivation starts with the general form of the circuit transconductance, as deducible from (8.36), and replaces both $R_D$ and $R_S$ with the impedance in those respective branches, $Z_D$ and $Z_S$. This gives

Equation 6.18

$$G_m(f) = -\frac{g_m}{1 + g_m z_D + (g_m + g_ds) z_S}$$
The gain follows from multiplying the transconductance by the load at the drain, \( Z_D \), and multiplying by the voltage divider, \( V_o/V_d = R_L/(R_L + 1/j2\pi fC_d) \). The result is

\[
a_v(f) = \frac{-g_mR_D'}{1 + g_dsZ_D + (g_m + g_ds)Z_S} \frac{1}{1 + \frac{f_d}{f}}
\]

### 6.5. Summary of Equations

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_g )</td>
<td>( f_{3dB} = \frac{1}{2\pi(R_g + R_s)C_g} )</td>
<td>MOSFET coupling capacitor corner-frequency equation.</td>
</tr>
<tr>
<td>( f_z )</td>
<td>( \frac{1}{2\pi R_s C_s} )</td>
<td>Zero and pole equations for bypass capacitor response function.</td>
</tr>
<tr>
<td>( f_p )</td>
<td>( \frac{1}{2\pi} \frac{R_s}{1 + g_m R_S} C_S )</td>
<td>Computation of ( f_{3dB} ) frequency with one pole and one zero.</td>
</tr>
<tr>
<td>( f_{3dB} )</td>
<td>( \sqrt{f_z^2 - 2f_z^2 (1 + g_m R_S)^2} )</td>
<td>Approximate ( f_{3dB} ) frequency for capacitor ( C_s ).</td>
</tr>
<tr>
<td>( f_s )</td>
<td>( \left[ 1 + \frac{(g_m + g_ds)R_S}{1 + g_ds R_D} \right] f_z )</td>
<td>Pole frequency ( f_s ) with ( g_{ds} ) included in the derivation.</td>
</tr>
<tr>
<td>( f_d )</td>
<td>( \frac{1}{2\pi(R_D + R_L)C_d} )</td>
<td>Load coupling capacitor corner-frequency equation.</td>
</tr>
</tbody>
</table>

Note: Any one of the frequencies, \( f_g \), \( f_s \) (approximate), or \( f_d \) is the \( f_{3dB} \) (corner) frequency if it is the dominant (high) frequency. Otherwise, the corner frequency is some combination.

### 6.6. Exercises and Projects

Project Mathcad: 
- Exercise06.mcd - Project06.mcd - Exercise07.mcd, Project07_1.mcd
- Project07_2.mcd.
Unit 7. MOSFET Source-Follower Buffer Stage

High-gain stages in amplifiers are usually some form of differential stage or common-source stage. These are inherently high-output-resistance stages and are not suitable for low-impedance loads. The solution for a requirement to drive low-impedance loads is to insert a buffer stage between the output of the common-source stage and the load. The buffer will be a source-follower stage. The name follower comes from the fact that to a good approximation, the output voltage follows the input voltage; that is, it has an open-circuit gain of unity and low output resistance.

Although the output voltage/input voltage relation is sometimes loosely referred to as the gain, it would be more accurate to label it the voltage transfer function, as the "gain" is less than 1. The transfer function is explored in the following for various possibilities of degrees of approximation in the linear circuit.

7.1. DC (Bias) Circuit

The circuit diagram shown in Fig. 7.1 uses for the transistor a symbol that includes the body connection. This is to emphasize the fact that the output (source) of the source follower is generally (and usually) at different dc and signal potentials from the body. In Project 8 we measure the gain for both the connection shown (which we can make for this special case of one transistor on the chip being used) and with the body connected to VSS, which is signal ground. The latter demonstrates the extent of the influence that the body effect has on the gain when it is not possible to connect the body and source together as shown in Fig. 7.1.
**Figure 7.1.** Source-follower (common-drain) stage (NMOS transistor) with the input at the gate and the output at the source. In this example, the source is connected to the body. Usually, in a circuit, the body will be attached to the power supply $V_{SS}$ (NMOS).

The design of the stage will often consist of setting the dc output at $V_O = 0$ V (for a dual power supply), as this will be the final (output) stage. Therefore, $R_S$ will be selected based on the design drain current from $R_S = |V_{SS}|/I_D$. It is then necessary to determine $V_{GS}$ in order to determine the $V_G = V_{GS}$ required (which will be set by the dc circuitry of the preceding circuit).

For the usual practical application, body voltage, $V_B = V_{SS}$. With $V_S = 0$ V, $V_{SB} = |V_{SS}|$. Thus, the threshold voltage, including body effect, will be

**Equation 7.1**

\[
V_{tn} = V_{tno} + \gamma_n \left( \sqrt{|V_{SS}| + 2\phi} - \sqrt{2\phi} \right)
\]

and the gate bias voltage will be obtainable from

**Equation 7.2**

\[
V_G = \sqrt{\frac{|V_{DD}|}{k_n}} + V_{tn}
\]

If the source and body are connected, as in [Fig. 7.1](#), $V_{tn}$ is replaced with $V_{tno}$. 

```
7.2. Source-Follower Voltage Transfer Relation

A signal circuit is shown in Fig. 7.2, where the dc supplies have been replaced with ground. Also, the internal resistance, $r_{ds} = 1/g_{ds}$, of the transistor has been included in the signal circuit. Note that it is in parallel with $R_S$ since the drain is tied to signal ground. Assume for now that source and body are connected as in Fig. 7.1.

**Figure 7.2. Signal circuit of the source follower. Body effect is absent since the source and body are assumed connected.**

Regardless of the terminal configuration, for infinite output resistance and with the body and source connected, the relationship between the drain current and gate–source control voltage of the transistor is (4.1) with $g_{ds} = g_{mb} = 0$, which is [(2.5)]

$$I_d = g_m V_{gs}$$

In the source-follower circuit, the output resistance of the transistor can be included in the source-follower load and (2.5) effectively applies.

The transconductance for the circuit configuration with a source resistor was shown in Unit 4 to be [(4.8)]

$$G_m = \frac{g_m}{1 + g_m R_S'}$$

where, for this case, $R_S'$ is the source-follower load, which includes the transistor output resistance and is
Equation 7.3

\[ R'_S = R_S \| r_d = \frac{R_S}{1 + g_m R'_S} \]

Then using

Equation 7.4

\[ V_o = I_d R'_S \]

the "gain" (the transfer function is less than unity) is determined to be

Equation 7.5

\[ a_v = \frac{V_o}{V_i} = \frac{g_m R'_S}{1 + g_m R'_S} \]

Ideally, this is a unity gain, as would be the case for \( g_m R'_S \gg 1 \). In bipolar transistors, this condition is closely approached. However, in MOSFET source followers, the ideal case is in general not reached. As we will see below, this deficiency is enhanced when the body effect is included.

Note that \( a_v \) is

Equation 7.6

\[ a_v = \frac{R'_S}{\frac{1}{g_m} + R'_S} \]

This is the expression for a simple voltage divider. Thus the source follower is the equivalent of a unity-gain circuit with load \( R'_S \) and output resistance \( 1/g_m \). We can conclude that the transistor viewed from the source has an output resistance of \( 1/g_m \).

Finally, with \( R'_S \) separated into its component parts, the source-follower gain becomes
Equation 7.7
\[ a_v = \frac{g_m}{g_m + \frac{1}{R_S} + g_{ds}} \]

In general, the \( g_{ds} \) parameter can be dropped. The ratio of \( g_m/g_{ds} \) is

Equation 7.8
\[ \frac{g_m}{g_{ds}} \approx \frac{2}{\lambda_p V_{\text{eff}}} \]

7.3. Body Effect and Source-Follower Voltage Transfer Relation

Suppose now, as in Fig. 7.3, that the body terminal is connected to \( V_{SS} \), which is signal ground. Following the definition of the body-effect transconductance, \( g_{mb} \), the component of \( I_d \) due to source-body voltage \( V_{sb} \) is [from (4.1)]

Equation 7.9
\[ I_{db} = g_{mb} V_{sb} \]

Since the body is at zero potential (signal), this is

Equation 7.10
\[ I_{db} = g_{mb} V_s = g_{mb} V_o \]

This component of current can be included in the circuit, as shown in Fig. 7.3, with an additional resistance in parallel with \( R_S \) of value \( 1/g_{mb} \). That is, the body-effect contribution to the drain current is a voltage-dependent current source, where the voltage is the same as that across the current source.

Figure 7.3. Source-follower signal equivalent circuit with body connected to \( V_{SS} \) which is signal ground. The body effect is taken care of for this case with a resistance of magnitude \( 1/g_{mb} \) placed in parallel with \( R_S \) along with \( r_{ds} = 1/g_{ds} \).
With the body-effect addition, the source-follower gain expression is modified to the following:

Equation 7.11

\[ a_v = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_S} + g_{ds}} \]

The body-effect parameter is related to \( g_m \) by \((4.11)\)

\[ g_{mb} = \eta g_m \]

with

\[ \eta = \frac{\gamma_n}{2\sqrt{\lambda_B} + 2\phi_F} \]

With the substitution of \((4.11)\) in \((7.11)\), the gain is

Equation 7.12

\[ a_v = \frac{g_m}{g_m (1 + \eta) + \frac{1}{R_S} + g_{ds}} \]
In modern integrated circuits, resistor $R_S$ will be replaced with a current-source output resistance, which is significantly greater than $R_S$. The source-follower gain is, in this case, approximately (with no external load)

Equation 7.13

$$a_v = \frac{1}{1 + \eta}$$

Parameter $\eta$ will typically be in the range $0.1 < \eta < 0.2$.

Note that the body effect degrades the "gain" significantly below the ideal unity. In the project on the source-follower circuit, we measure the voltage transfer function of the source follower for a range of dc drain current with body and source connected and with the body connected to $V_{SS}$. Τηε ρεσυλτινγ χυρϖεσ ωιλλ βε χομπαρεδ το δεμονστρατε τηε βοδψ εφφεχτ ο ν τηε τρανσφερ φυνχτιον. Α χυρϖε φιτ οφ τηε ΣΠΙΧΕ εθυατιον το μεασυρεδ δατα ωιλλ προσιδε φορ αν αλτερνατιϖε δετερμινατιον οφ παραμετερ $\gamma_n$. Τhis value should be close to the value obtained from dc measurements.

### 7.4. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{tn} = V_{tno} + \gamma_n \left(\sqrt{V_{SS}^2 + 2\phi} - \sqrt{2\phi}\right)$</td>
<td>Threshold voltage $V_S = 0$ zero volts and negative power supply $V_{SS}$.</td>
</tr>
<tr>
<td>$a_v = \frac{g_m}{g_m + \frac{1}{R_S} + g_{ds}}$</td>
<td>Source-follower voltage gain with $V_{sb} = 0$.</td>
</tr>
<tr>
<td>$a_v = \frac{g_m}{g_m (1 + \eta) + \frac{1}{R_S} + g_{ds}}$</td>
<td>Source-follower voltage gain with $V_{sb} = I_d R_s$.</td>
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<tr>
<td>$g_{mb} = \eta g_m$</td>
<td>Body-effect transconductance.</td>
</tr>
<tr>
<td>$\eta = \frac{\gamma_n}{2\sqrt{V_{SB}^2 + 2\phi_F}}$</td>
<td>Source-follower body-effect degradation factor.</td>
</tr>
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</table>

### 7.5. Exercises and Projects

Project Mathcad Files
- Exercise08.mcd - Project08.mcd

Laboratory Project 8
- NMOS Source-Follower Stage
- Source-Follower DC Evaluation
- Source-Follower Voltage Transfer Relation
Unit 8. MOSFET Differential Amplifier Stage

The MOSFET differential amplifier stage is a relatively high-gain stage with grounded dc inputs, which requires no bypass capacitor. The stage also has the important advantage of having two inputs, one inverting and one noninverting. This is essential in operational amplifiers where one or the other (or both) is used, depending on the application. The two inputs also provide for operating the stage in the differential mode, where the input is not referenced to ground. The differential amplifier stage discussed here is an all-resistor circuit with source and drain resistors. In a modern integrated circuit, these are replaced with transistor current sources. However, the principle of operation is the same, and the resistor version can be implemented in our laboratory project.

Various segments of the differential amplifier comprise amplifier stages from all three terminal configurations: the common source, the common gate, and the source follower (common drain). In this unit, a detailed theoretical analysis of all three stages is undertaken (based on Level 1 SPICE). The linear models used include, progressively, the output conductance, $g_{ds}$, and the body-effect transconductance, $g_{nb}$.

8.1. DC (Bias) Circuit

The equation for the dc circuit (Fig. 8.1) is the same as for the current-source common-source stage except that the bias resistor has current $2I_D$ as the current from both transistors is flowing through this resistor. For now, the stage will be assumed to be perfectly balanced such that $I_{D1} = I_{D2} = I_D$. The bias equation is

Equation 8.1

$$I_D = \frac{V_{SS} - V_{GS}}{2R_{bias}} = \frac{V_{SS} - \sqrt{\frac{I_D}{k_n}} - V_{ln}}{2R_{bias}}$$

Figure 8.1. Dc circuit for differential-amplifier stage with resistance bias. Source and body are normally at different potentials. In the project with this circuit, we attach the two sources to the transistor body, which is allowed in a simple circuit.
Note that the threshold voltage is that for $V_{SB} \neq 0$. The solution can be obtained with the inclusion of the threshold voltage equation, also a function of $I_D$,

Equation 8.2

$$V_{tn} = V_{tno} + \gamma_n \left( \sqrt{2I_D R_{bias}} + 2\Phi_F - \sqrt{2\Phi_F} \right)$$

In the project on the differential amplifier, we can connect the sources and bodies of the two transistors. This is because only NMOS transistors are used in the circuit, and both transistors have the source connected to the same node. In this case, $V_{tn} = V_{tno}$.

**8.2. DC Imbalances**

In a real transistor, parameters $k_n$, $V_{tno}$, and $\lambda_n$ can be slightly different such that, in general, $I_{D1} \neq I_{D2}$. The ratio of the currents is given by

Equation 8.3

$$\frac{I_{D2}}{I_{D1}} = \frac{k_{n2} \left( V_{GS} - V_{tno2} \right)^2 \left( 1 + \lambda_{n2} V_{DS2} \right)}{k_{n1} \left( V_{GS} - V_{tno1} \right)^2 \left( 1 + \lambda_{n1} V_{DS1} \right)}$$

where, in the circuit with the gate of $M_1$ grounded, $V_{GS1} = V_{GS2} = V_{GS}$. For the specific case of the project on the amplifier, we can assume that $V_{DS1} \approx V_{DS2}$ such that

Equation 8.4
To simplify the relation, it is advantageous to express parameters in terms of increments. For example, threshold voltage will be expressed as a mean value

Equation 8.5

\[ V_{tno} = \frac{V_{tno1} + V_{tno2}}{2} \]

and a difference between the threshold voltage of the two transistors

Equation 8.6

\[ V_{t\epsilon} = V_{tno2} - V_{tno1} \]

such that

Equation 8.7

\[ V_{tno2} = V_{tno} + \frac{V_{t\epsilon}}{2} \]

and

Equation 8.8

\[ V_{tno1} = V_{tno} - \frac{V_{t\epsilon}}{2} \]

Using these definitions along with \( V_{eff} = V_{GS} - V_{tno} \), we have
Equation 8.9

\[
\frac{I_{D2}}{I_{D1}} = \frac{k_{n2}}{k_{n1}} \left( \frac{V_{\text{eff}} - \frac{V_{\text{tho}}}{2}}{V_{\text{eff}} + \frac{V_{\text{tho}}}{2}} \right)^2 = \frac{k_{n2}}{k_{n1}} \left( 1 - \frac{V_{t\varepsilon}}{2V_{\text{eff}}} \right)^2
\]

or, approximately,

Equation 8.10

\[
\frac{I_{D2}}{I_{D1}} \approx \frac{k_{n2}}{k_{n1}} \left( 1 - \frac{2V_{t\varepsilon}}{V_{\text{eff}}} \right)
\]

In the differential amplifier project (PMOS), we measure the drain currents along with \(V_{SG}\) over a range of drain current values. These are used to obtain, in the Mathcad project file, \(k_{n1}, k_{n2}\), and the threshold voltages and thus, \(V_{t\varepsilon}\). This will provide a comparison between the measured drain-current ratios and (8.10) as a function of \(V_{\text{eff}}\) and drain current.

8.3. Signal Voltage Gain of the Ideal Differential Amplifier Stage

This initial assessment of the gain of the differential amplifier neglects the effects of the bias resistor, \(R_{\text{bias}}\), and of the output resistance of the transistors as well as the body effect. These effects are considered below. To generalize the discussion to include the possibility of inverting and noninverting modes of operation, we base the discussion on the circuit (Fig. 8.2) with a drain resistor for both transistors. The inverting and noninverting modes take, respectively, the outputs at \(V_{d1} = V_{o1}(a_{v1})\) and \(V_{d2} = V_{o2}(a_{v2})\). Also, this is the configuration that is studied in the project on the differential amplifier. Note that the input could arbitrarily be moved to the gate of \(M_2\), in which case the output taken at \(V_{d1}\) becomes the noninverting mode, and so forth.

Figure 8.2. Circuit for our project on the differential amplifier. The circuit has resistors in both drain branches for comparing the gain from the noninverting and inverting outputs and for sensing the bias drain currents.
Assume for the present that the amplifier is perfectly symmetrical such that, for example, \( I_{D1} = I_{D2} \) and \( g_{m1} = g_{m2} \). A signal voltage \( V_i \) is applied to the gate of \( M_1 \) as shown in the diagram. The voltage divides between the two transistors (from gate 1 to gate 2) to give

Equation 8.11

\[
V_i = V_{gs1} + V_{gs2} = V_{gs1} - V_{gs2}
\]

Since \( V_{gs1} = |V_{sg2}| \) (due to the symmetry of this case), then

Equation 8.12

\[
V_{gs1} = \frac{V_i}{2} = -V_{gs2}
\]

The negative \( V_{gs2} \) results from the fact that the total \( v_{GS2} \) is reduced from bias \( V_{GS2} \) upon the application of a positive signal voltage, \( V_i \), at the gate of \( M_1 \) (i.e., \( v_{GS2} = V_{GS2} - V_i/2 \)). It follows that total \( i_{D2} \) decreases, which leads to a positive signal voltage at the drain, \( V_{d2} \). Thus, the amplification is noninverting.

As always, the relation between the signal drain current and the signal drain-source voltage is \((4.1)\), which is (with \( g_{ds} = g_{mb} = 0 \))

\[
I_d = g_m V_{gs}
\]
Eliminating $V_{gs}$ in (4.1), applied to $M_2$, with (8.12), the drain current for $M_2$ is related to the input voltage, $V_i$, by

Equation 8.13

$$I_{d2} = -g_{m2} \frac{V_i}{2}$$

Combining (8.13) with $V_{o2} = -I_{d2}R_{D2}$, the output voltage is related to the input voltage by

Equation 8.14

$$V_{d2} = V_{o2} = \frac{1}{2} g_{m2} R_{D2} V_i$$

such that the gain is

Equation 8.15

$$a_{v2} = \frac{V_{d2}}{V_i} = \frac{1}{2} g_{m2} R_{D2}$$

Note that there is no minus in the relation; that is, this is the noninverting amplifier mode. Also note that the gain for this amplifier is one-half of that for the common-source amplifier. This is a reasonable price to pay for not having a bypass capacitor. The amplification can be viewed as a source-follower stage in cascade with a common-base stage, neither of which is an inverting stage.

The inverting mode of the amplifier is for the output taken at the drain of $M_1$. For this case, $V_{o1} = -I_{d1}R_{D1}$, and from (8.12) and (4.1) applied to $M_1$, $I_{d1} = g_{m1} V_g/2$ and the voltage relationship is

Equation 8.16

$$V_{d1} = V_{o1} = -\frac{1}{2} g_{m1} R_{D1} V_i$$

This leads to the inverting gain, which is
The results above ignore the effect of resistance, $R_{bias}$. When it is included, it is no longer valid to assume that $V_{gs1} = V_{sg2}$, even with $I_{D1} = I_{D2}$. The bias-resistor effect is examined here based on a signal equivalent circuit of Fig. 8.3. The resistance at the source of $M_1$ consists of the bias resistor and the linear-model resistance $1/g_{m2}$ (which neglects $1/g_{ds2}$), looking into the source of $M_2$.

**Figure 8.3. Source circuit as viewed from $M_1$. Source resistance includes actual resistor $R_{bias}$ in parallel with input resistance at source of $M_2$, which is $1/g_{m2}$ for the conditions of this unit.**

For the noninverting mode, the circuit transconductance, $G_{m2} = I_{d2}/V_i$, is

**Equation 8.18**

$$G_{m2} = \frac{R_{bias}}{1 + g_{m2}R_{bias}}$$

Parameter $g_{m2}$ is the transconductance $I_{d2}/V_{s2}$ (i.e., from the source of $M_2$ to the output $V_{o2}$). Note that the fraction is just a voltage divider, $V_{s2}/V_i$, since the output resistance at the source of $M_1$ is $1/g_{m1}$, as noted in connection with (7.6). With $g_{m1} = g_{m2}$, the multiplying fraction assumes the value of $\frac{1}{2}$ for very large $R_{bias}$.

The noninverting gain, which includes the effect of the bias resistor, is
where the right-hand side uses $g_{m1} = g_{m2}$. The gain result is technically that of the cascade of a source-follower stage ($M_1$) and a common-gate stage, $g_{m2}R_{D2}$ ($M_2$). The multiplying fraction is $< \frac{1}{2}$.

The gain for the inverting side can be obtained by using (5.15), which is for a common-source amplifier with source resistor. This gives for the inverting-mode gain

Equation 8.20

$$a_{v1} = \frac{-g_{m1}R_{D1}}{1 + g_{m1}R_{bias}} = -\frac{1 + g_{m1}R_{bias}}{1 + 2g_{m1}R_{bias}}g_{m1}R_{D1}$$

where the right-hand side again uses $g_{m1} = g_{m2}$. The multiplying fraction is $> \frac{1}{2}$. Note that for both inverting and noninverting gains, the effect of $R_{bias}$ can be neglected for most purposes, as the multiplying fractions in (8.19) and (8.20) are both close to $\frac{1}{2}$.

The choice of the input at gate 1 is arbitrary and all of the results obtained here apply equally to the input taken at gate 2. The inverting output is always at the side of the input, and the noninverting output is always at the opposite side.

8.5. Differential Voltage Gain

Suppose that an input voltage, $V_{g12} = V_{g1} - V_{g2}$, is applied between the inputs. Due to symmetry, the voltage magnitudes at the inputs with respect to ground are $V_{g1} = V_{g12}/2$ and $V_{g2} = -V_{g12}/2$, respectively. The noninverting output, $V_{d2}$, for this case is, by superposition,

Equation 8.21

$$V_{d2} = \frac{g_{m1}R_{bias}}{1 + 2g_{m1}R_{bias}}g_{m2}R_{D2} \frac{V_{g12}}{2} + \frac{1 + g_{m1}R_{bias}}{1 + 2g_{m1}R_{bias}}g_{m1}R_{D1} \frac{V_{g12}}{2} = \frac{1}{2}g_{m2}R_{D2}V_{g12}$$
The gains for the contributions from $V_{g1}$ and $V_{g2}$ are (8.19) and (8.20), respectively. This is the case of a pure differential input with resulting gain

Equation 8.22

$$a_{vd2} = \frac{1}{2} g_m R_{D2}$$

A similar approach applied to obtain the gain for the output taken as $V_{d1}$ produces

Equation 8.23

$$a_{vd1} = -\frac{1}{2} g_m R_{D1}$$

Assume, for a numerical example, that $I_D = 100 \mu A$, $R_{D1} = 50 K\Omega$, and $g_m = 200 \mu A/V$ ($V_{effn} = 0.5 V$). In this case the gain is $a_{vd1} = -10$. This would be consistent with $V_{DD} = |V_{SS}| = 10 V$.

The gain for the case of the differential output, $a_{vd12} = (V_{d1} - V_{d2})/(V_{g1} - V_{g2})$, can be obtained from $(V_{d1} - V_{d2}) = -(1/2)g_{m1}R_{D1}V_{g12} - (1/2)g_{m2}R_{D2}V_{g12}$ and is

Equation 8.24

$$a_{vd12} = -g_m R_D$$

where $g_{m1} = g_{m2}$ and $R_{D1} = R_{D2} = R_D$. Note that (8.22) and (8.23) are the same as (8.15) and (8.17). However, (8.15) and (8.17) are the limiting forms of (8.19) and (8.20) for $R_{bias} \rightarrow \infty$, whereas (8.22) and (8.24) apply for a finite $R_{bias}$.

### 8.6. Common-Mode Voltage Gain

The common-mode gain is defined for the same voltage applied simultaneously to both inputs. The output must be the same at either output terminal (again assuming that $g_{m1} = g_{m2}$ and $R_{D1} = R_{D2}$). For example, for the output $V_{d2}$, the gain can be determined by a superposition of gains, inverting (input, $V_{g2}$) and noninverting (input, $V_{g1}$), with $R_{D2}$ in both equations.

Using (8.19) (noninverting) and (8.20) (inverting), the gain for finite $R_{bias}$ is, accordingly,
Equation 8.25

$$a_{vcm} = \left( \frac{g_m R_{bias}}{1 + 2g_m R_{bias}} - \frac{1 + g_m R_{bias}}{1 + 2g_m R_{bias}} \right) g_m R_D$$

which is

Equation 8.26

$$a_{vcm} = \frac{-g_m R_D}{1 + 2g_m R_{bias}}$$

The result is that of a common-source stage with source resistance $2R_{bias}$. This is intuitively correct as taken from the half-circuit viewpoint, where the circuit is completely symmetrical. The input from either side looks at a common-source stage except that the opposite side is contributing an equal amount of source current, thus giving an effective source resistance equal to twice the actual value. A valid approximate form for well-designed circuits (in terms of common-mode gain) is

Equation 8.27

$$a_{vcm} \approx \frac{-R_D}{2R_{bias}}$$

The same result applies to the case of the output taken at the opposite drain, with the substitution of $R_{D1}$ for $R_{D2}$. Using the circuit values following (8.23) plus $R_{bias} = 85 \, \text{k}\Omega$, $a_{vcm} \approx 0.3$. Note that this result in combination with the gain from (8.23) would indicate that this is not a particularly good design. The goal is for $a_{vd} >> a_{vcm}$.

8.7. Voltage Gains Including Transistor Output Resistance

In Project 9 we measure the gain of a "balanced" stage with drain resistors for both transistors. The amplifier is the PMOS version of the NMOS amplifier of Fig. 8.2. We obtain an exact Level 1 SPICE solution for the gains for both outputs. The example is used to explore the use of a simulator for obtaining precision results to compare with simple hand calculations.

For larger $\lambda_n$ values (NMOS), the output resistance can influence the gain and complicate the gain expressions considerably. Here we consider the effect due to $g_{ds1}$ and $g_{ds2}$ while
retaining the effect of $R_{bias}$. In the following, the gain of the inverting input, $a_{v1}$, is obtained again as a common-source stage with source resistance. The effect of $g_{ds2}$ on the effective source resistance is included (input at the source of $M_2$). The effects due to $g_{ds1}$ are also taken into consideration.

The gain of the noninverting case, $a_{v2}$, is obtained by considering the cascade of the source follower stage ($M_1$) and the common-gate stage ($M_2$), as, in effect, was done in the development of (8.19). The source-follower gain takes into account effects from $g_{ds1}$ and $g_{ds2}$, and the gain of the common-gate stage depends on $g_{ds2}$.

### 8.7.1. Gain of the Common-Source Stage with Transistor Output Conductance and Source Resistor

The circuit transconductance for a common-source stage with source resistor, with the inclusion of $g_{ds}$, was developed in Unit 4 ([4.18]). This will be reviewed and reinforced here in the form of a slightly different approach to the result. The signal circuit for this case is again given in Fig. 8.4. Using the variables of Fig. 8.4, the circuit transconductance is $G_{ml} = I_{d1}/V_i$. The object is thus to obtain a relation between these two variables.

**Figure 8.4. Circuit for obtaining the gain for the inverting output with the transistor output resistance included. $R_s$ includes all resistance contributions at the source.**

\[ I_{R_s} = I_{d1} = \frac{1}{g_{ds} + R_D + R_s} g_{ml} V_{gs1} = \frac{g_m}{1 + g_{ds}(R_D + R_s)} V_{gs1} \]
This is the portion of current source $g_{m1}V_{gs1}$, shared between $1/g_{ds}$ and $R_D + R_s$, which flows through $R_D + R_s$, that is, $I_{d1}$. Note that $R_D + R_s$ and $1/g_{ds1}$ are in parallel and shunt the transistor current source.

A relation for $V_{gs1}$ in terms of $I_{d1}$ follows, which is

Equation 8.29

\[
V_{gs1} = \frac{1+g_{ds1}(R_D+R_s)}{g_{m1}}I_{d1}
\]

The input Voltage is the sum of $V_{gs1}$ and the drop across $R_s$. That is,

Equation 8.30

\[
V_i = V_{gs1} + I_{d1}R_s
\]

Using (8.29) in (8.30) gives

Equation 8.31

\[
V_i = \left[\frac{1+g_{ds1}(R_D+R_s)}{g_{m1}} + R_s\right]I_{d1}
\]

or

Equation 8.32

\[
I_{d1} = \frac{g_{m1}V_i}{(R_D+R_s)g_{ds1} + (1+g_{m1}R_s)}
\]

The circuit transconductance follows as

Equation 8.33
The gain for this case is then

Equation 8.34

\[
G_m = \frac{g_m}{(R_{D1} + R_s) g_{ds1} + (1 + g_m R_s)}
\]

A discussion of \( R_s \) as affected by \( g_{ds2} \) follows.

8.7.2. Common-Gate Amplifier Stage

The circuit diagram of Fig. 8.5 is for the M2 portion of the differential amplifier. The input is applied at the source, \( V_{s2} \), and the output is taken at the drain, \( V_{d2} = V_{o2} \), while the gate is grounded. This is a common-gate configuration. Here we analyze the input resistance, for evaluating the effect on \( R_s \), and gain of the common-gate stage.

Figure 8.5. Circuit that includes the output resistance of M2. The circuit is for obtaining input resistance at the source of M2 and the gain of the common-gate stage of M2

Without \( g_{ds2} \), the input resistance at the source is just \( 1/g_m \). With \( g_{ds2} \) in place, there is a positive feedback from the drain output to the source input. This causes the input resistance to increase. With \( g_{ds2} \), the current into the source terminal is
Equation 8.35

\[ I_{d2} = g_{m2} V_{s2} - (I_{d2} R_{D2} - V_{s2}) g_{ds2} \]

It is noted that the \( g_{ds2} \) term reduces the input current, which has the effect of increasing the input resistance. From (8.35), the resulting input resistance at the source, \( R_{is2} = V_{s2}/I_{d2} \), is

Equation 8.36

\[ R_{is2} = \frac{1 + g_{ds2} R_{D2}}{g_{m2} + g_{ds2}} \]

The input resistance goes to \( 1/g_{m2} \), as noted above, for \( g_{ds2} = 0 \). The expression for the equivalent \( R_s \) is now \( R_s = R_{bias} || R_{is2} \), where \( R_{is2} \) is (8.36). In modern integrated circuits, \( R_{D2} \) may be replaced with a high-resistance transistor current source, and the input resistance is this case can be much greater than \( 1/g_{m2} \).

The gain of the common-gate stage is obtained as follows: The output voltage is

Equation 8.37

\[ V_{d2} = I_{d2} R_{D2} = \left( g_{m2} V_{s2} - I_{g_{ds2}} \right) R_{D2} = \left[ g_{m2} V_{s2} - (V_{d2} - V_{s2}) g_{ds2} \right] R_{D2} \]

which gives

Equation 8.38

\[ a_{wg} = \frac{(g_{m2} + g_{ds2}) R_{D2}}{1 + g_{ds2} R_{D2}} \]

Note that for \( g_{ds2} = 0 \), the gain has the same magnitude as the simple case for the common-source stage.
8.7.3. Voltage Gain for the Noninverting Output

The noninverting amplifier gain is based on a cascade of a source-follower stage \((M_1)\) and a common-gate stage \((M_2)\). The source-follower transconductance, \(I_{d1}/V_i\), is \((8.33)\). Using this with \(V_{s1} = I_{d1}R_s\) gives

Equation 8.39

\[
a_{vaf} = \frac{g_{mf}R_s}{(R_{D1} + R_s) g_{ds1} + (1 + g_{mf}R_s)}
\]

Note that the magnitude is about \(\frac{1}{2}\). Overall gain is the product of \((8.38)\) and \((8.39)\), which is

Equation 8.40

\[
a_{v2} = a_{vaf}a_{vg} = \frac{g_{mf}R_s}{(R_{D1} + R_s) g_{ds1} + (1 + g_{mf}R_s)} \frac{(g_{m2} + g_{ds2})R_{D2}}{1 + g_{ds2}R_{D2}}
\]

The equations from this unit are summarized below in Unit 8.11.

Recall from the discussion of MOSFET model parameters that \(g_{ds}\) is given by \((4.13)\), which is

\[
g_{ds} = \frac{I_D\lambda_n}{1 + \lambda_n V_{DS}}
\]

Thus, the gain expression depends on parameter \(\lambda\), and especially if \(\lambda\) is somewhat large. In Project 9 we measure the gains from the two drains and use the results to find the value of \(\lambda\) that makes the theory fit the measurements. In this way, we are getting a signal-derived experimental number to compare with that obtained in the parameter-determination project. This will be done using the PMOS configuration since the value of \(\lambda_p\) is large and the effect is significant. All of the gain expressions, which are based on NMOS transistors, apply exactly to the PMOS stage with substitution of subscripts; change \(n\) to \(p\) (parameters) and reverse the order for dc voltage variables.

For hand calculations, approximate forms must reasonably be used. This applies to approximate forms for device parameters and gain. The basic gain equations are, again, assuming that \(g_{ds} = 0\) and \(R_{bias} = \infty\), simply, as given by \((8.15)\) and \((8.17)\),
with $R_{D1} = R_{D2}$ and $g_{m1} = g_{m2}$. In the differential amplifier project, we will compare these with the more precision forms.

### 8.8. Body Effect and Voltage Gain

In Project 9 we are able to connect the sources of the transistors to the chip body. Certainly, in general this cannot be done such that there is a body effect associated with the differential-amplifier-stage transistors. The necessary alterations to the gain equations are determined in the following. At the end of this unit, we will have the complete, precision-gain calculation equations of Level 1 SPICE. It will be informative to consider numerical results that are based on various degrees of approximations, and this is done below.

#### 8.8.1. Common-Source Stage and Body Effect

With the body effect present, a component of current, $g_{mb1}V_s$ (Fig. 8.6), is subtracted from $g_{m1}V_{gs1}$ such that (8.28) for this case is modified to become

Equation 8.41

$$I_{d1} = \frac{1}{g_{ds1}^{-1} + R_{D1}^{-1} + R_s^{-1}} \left( g_{m1}V_{gs1} - g_{mb1}V_s \right)$$

**Figure 8.6.** Circuit for obtaining the inverting gain of the differential stage with body effect included. Body effect is accounted for by the current source added to the transistor signal (linear) equivalent circuit.
Additionally using $V_s = I_{d1}R_s$ and $V_{gs1} = V_i - I_{d1}R_s$ (8.30) in (8.41), a relation between $I_{d1}$ and $V_i$ is obtained, which is

**Equation 8.42**

$$I_{d1} = \frac{1}{1 + g_{ds1}(R_D + R_S)} \left[ g_{m1}(V_i - I_{d1}R_S) - g_{mb1}I_{d1}R_S \right]$$

Solving for $I_{d1}$, the circuit transconductance is, for the body-effect case,

**Equation 8.43**

$$g_{m1} = \frac{I_{d1}}{V_i} = \frac{g_{m1}}{1 + g_{ds1}(R_D + R_S) + g_{m1}R_S + g_{mb1}R_S}$$

It follows that the gain for the inverting mode, with the addition of body effect, is

**Equation 8.44**

$$a_{V1} = -\frac{g_{m1}R_D}{\left[1 + g_{ds1}(R_D + R_S)\right] + (1 + \eta_n)g_{m1}R_S}$$
The effect of $\eta_n$ in the denominator tends to make the gain smaller. However, the body effect, as shown below, will decrease $R_s$ such that the two effects tend to cancel one another.

### 8.8.2. Common-Gate Stage and Body Effect

The voltage applied to the common-gate stage is $V_{s2} = V_{sg2}$ (Fig. 8.7). Recall that in the g model for the transistor, as discussed for the common-source mode, current sources $g_{mb}V_{sb}$ and $g_mV_{gs}$ are in parallel but in opposite directions. Thus, the current sources $g_mV_{sg}$ and $g_{mb}V_{sb}$ are, for the common-gate mode, in the same direction since $V_{sb} = V_{sg} = -V_{gs}$; the common-gate has an effect transconductance of $(1 + \eta)g_m$. It follows that the input resistance of the common-gate stage is as obtained before the body effect was included [(8.38)], except for the addition of $\eta_n$, as in the following:

\[
R_{i2} = \frac{1 + g_{ds2}R_{d2}}{g_m (1 + \eta_n) + g_{ds2}}
\]

**Figure 8.7. Circuit that includes the voltage-dependent current source due to body effect associated with $M_2$. Body effect affects the input resistance into the source of $M_2$ and the gain of the common-gate stage of $M_2$.**

Similarly, the common-gate gain, (8.38), is readily modified with the addition of the multiplying factor $(1 + \eta_n)$. This is

\[
\text{Equation 8.46}
\]
Note that in the absence of $g_{ds2}$, the gain for the common-source stage reduces to $a_{vcd} = g_{m2} (1 + \eta_n) R_D2$, where, with body effect, the effective transconductance is, again, $(1 + \eta_n) g_{m2}$.

### 8.8.3. Source-Follower Stage with Body Effect

The transconductance relation obtained for the common-source stage given by (8.43) also applies to the source-follower stage. Combining this with $V_{s1} = I_d1 R_s$ leads to the source-follower gain associated with $M1$, which is

\[
a_{vSf} = \frac{g_{n1} R_s}{\left(R_D1 + R_s\right) g_{ds1} + \left[1 + g_{m1} (1 + \eta_n) R_s\right]}
\]

The overall gain is again

\[a_{v2} = a_{vSf} a_{vCG}\]

Note that the body effect for the source-follower stage increases the denominator of (8.49) while it increases the numerator in the common-gate result, (8.48). These tend to cancel, as in the case of the inverting gain.

### 8.9. Amplifier Gain with Differential and Common-Mode Inputs

For inputs at either or both gates, there exists a common-mode and differential-mode voltage. These are, for applied voltages $V_{g1}$ and $V_{g2}$, common mode

\[V_{cm} = \frac{V_{g1} + V_{g2}}{2}\]

and differential mode

\[\text{Equation 8.49}\]
\[ V_{\text{dm}} = V_{g1} - V_{g2} \]

Based on these definitions, the output, for example, \( V_{d1} \), for a given set of inputs is

Equation 8.50

\[ V_{d1} = a_{\text{vd1}} V_{\text{dm}} + a_{\text{vcm}} V_{\text{cm}} \]

where \( a_{\text{vd1}} \) and \( a_{\text{vcm}} \) are (8.23) and (8.26) (with \( R_{D1} \)), respectively. For the output \( V_{d2} \), \( a_{\text{vd2}} \) is substituted for \( a_{\text{vd1}} \). \( V_{\text{dm}} \) is a pure differential input and is not with respect to ground; the effect from the bias resistor is accounted for in the common-mode gain.

For the case of a single-ended input, for example, \( V_{g1} = V_i \) and \( V_{g2} = 0 \), the output is

Equation 8.51

\[ V_o = \left( a_{\text{vd1}} + \frac{a_{\text{vcm}}}{2} \right) V_i \]

This is identical to (8.20). The common-mode contribution can be significant, for example, in a resistance feedback amplifier (Unit 11). In this case, \( V_{\text{dm}} \) in (8.50) can be very small compared to \( V_{\text{cm}} \).

### 8.10. Comparison of Numerical Gain Results

Gain calculations were made using \( k_n = 1000 \ \mu A/V^2 \), \( \lambda_n = 0.05 \ \text{V}^{-1} \), \( R_D = 150 \ \text{k}\Omega \), \( R_{\text{bias}} = 100\text{k}\Omega \), \( \eta_n = 0.15 \), \( I_D = 50 \ \mu A \), and \( V_{\text{DS}} = 5 \ \text{V} \). The values are given in Table 8.1. For the comparison, \( g_m \) was calculated with the precision form [(4.5)] (\( \lambda_n \neq 0 \)) for all cases. Possibly a more valid consistency (hand calculation versus precision calculation) would be achieved with the use of the approximate form for \( g_m \) up to \( \lambda_n \neq 0 \). This would reduce some of the difference in the results. For example, for the first case, \( a_{v1} = -a_{v2} = -33.5 \), with the approximate form for \( g_m \) (\( \lambda_n \neq 0 \)).

| TABLE 8.1 |
|-------------|-----|-----|
| **Gain Magnitudes** | **\( a_{v1} \)** | **\( a_{v2} \)** |
| \( R_{\text{bias}} = \infty \), \( \lambda_n = 0 \), \( \eta_n = 0 \) | 37.5 | 37.5 |
| plus \( R_{\text{bias}} = 100\text{K}\Omega \) | 37.9 | 37.1 |
### Table 8.1

<table>
<thead>
<tr>
<th>Gain Magnitudes</th>
<th>$a_{v1}$</th>
<th>$a_{v2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>plus $\lambda_n = 0.05 , \text{V}^{-1}$</td>
<td>29.21</td>
<td>28.48</td>
</tr>
<tr>
<td>plus $\eta_n = 0.15$</td>
<td>29.17</td>
<td>28.53</td>
</tr>
</tbody>
</table>

It is notable that the various factors do not have a major effect on the results, even though the value of $\lambda_n$ is relatively large. This is especially true for the differential amplifier with resistive load, as considered here. The conclusion can be made that for initial hand-calculation purposes, the simplest form is satisfactory. Precision results can be obtained with a simulator.

### 8.11. Summary of Equations

- **Differential-stage bias equation.**
  
  $I_D = \frac{V_{SS} - V_{GS}}{2R_{bias}} = \frac{V_{SS} - \sqrt{I_D/\lambda_n} - V_{tn}}{2R_{bias}}$

- **Threshold voltage for $V_B = V_{SS}$ and thus $V_{SB} = 2I_D R_{bias}$.**
  
  $V_{tn} = V_{tno} + \gamma_n \left( \sqrt{2I_D R_{bias}} + \sqrt{2} \phi_F - \sqrt{2} \phi_F \right)$

- **Approximate relation for drain-current imbalance due to $k_{n1} \neq k_{n2}$ and $V_{tn1} \neq V_{tn2}$.**
  
  $\frac{I_{D2}}{I_{D1}} = \frac{k_{n2}}{k_{n1}} \left( \frac{1 - \frac{2V_{te}}{V_{eff}}}{V_{eff}} \right)$

- **Ideal voltage gain, $R_{bias} \rightarrow \infty$ and $g_{ds} = 0$, $g_{m1} = g_{m2} = g_m$.**
  
  $a_v = -\frac{1}{2} g_m R_{D1}$

  $a_{v1} = -\frac{1}{2} g_m R_{D1}$

  $a_{v2} = \frac{1}{2} g_m R_{D2}$

- **Gain $V_{d2}/V_{g1} = V_{o2}/V_1$ for noninverting output with finite $R_{bias}$.**
  
  $a_d = -\frac{1 + g_m R_{bias}}{1 + 2g_m R_{bias}} \frac{g_m R_{D1}}{g_{ds1} + (1 + g_m R_s)}$

- **Gain $V_{d1}/V_{g1} = V_{o1}/V_1$ for inverting output with finite $R_{bias}$.**
  
  $a_d = -\frac{g_m R_{bias}}{1 + 2g_m R_{bias}} \frac{g_m R_{D1}}{R_{D1} + R_s + (1 + g_m R_s)}$

- **Gain $V_{d1}/V_{g1} = V_{o1}/V_1$ for inverting output for source resistance, $R_s$, with $g_{ds} \neq 0$.**
  
  $R_s = R_{is2} || R_{bias}$

- **Input at the source of $M_2$ with $g_{ds} = 0$.**
  
  $R_{is2} = \frac{1 + g_m R_{D2}}{g_{m2} + g_{ds2}}$
<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D = \frac{V_{SS} - V_{GS}}{2R_{bias}} = \frac{V_{SS} - \sqrt{I_D/k_n} - V_{tn}}{2R_{bias}}$</td>
<td>Differential-stage bias equation.</td>
</tr>
<tr>
<td>$a_{vcg} = \frac{(g_{m2} + g_{ds2})R_{D2}}{1 + g_{ds2}R_{D2}}$</td>
<td>Gain $V_{d2}/V_{s2} = V_{o2}/V_{s2}$ for common-gate stage of $M_2$ for $g_{ds} \neq 0$.</td>
</tr>
<tr>
<td>$a_{af} = \frac{g_mR_s}{(R_{D1} + R_s)(g_{ds1} + 1 + g_mR_s)}$</td>
<td>Gain $V_{s1}/V_{g1} = V_{s1}/V_i$ of source-follower with input at gate of $M_1$ and output at source of $M_1$.</td>
</tr>
<tr>
<td>$a_{v2} = \frac{g_mR_s}{(R_{D1} + R_s)(g_{ds1} + 1 + g_mR_s)} \frac{(g_{m2} + g_{ds2})R_{D2}}{1 + g_{ds2}R_{D2}}$</td>
<td>Gain $V_{d2}/V_{g1} = V_{o2}/V_i$ for noninverting output and $g_{ds} \neq 0$.</td>
</tr>
<tr>
<td>$a_{vd12} = -g_mR_D$</td>
<td>Gain for differential input, differential output with $R_{D1} = R_{D2}$ and $g_{m1} = g_{m2}$.</td>
</tr>
<tr>
<td>$a_{vcm} = \frac{-g_mR_{D2}}{1 + 2g_mR_{bias}}$</td>
<td>Common-mode gain.</td>
</tr>
<tr>
<td>$a_{v1} = -\frac{g_mR_{D1}}{1 + g_{ds1}(R_{D1} + R_s) + (1 + \eta)g_mR_s}$</td>
<td>Inverting-input gain $V_{d1}/V_{g1} = V_{o1}/V_i$, including body effect.</td>
</tr>
<tr>
<td>$R_S = R_{is2} \parallel R_{bias}$</td>
<td></td>
</tr>
<tr>
<td>$R_{is2} = \frac{1 + g_{ds2}R_{D2}}{g_{m2}(1 + \eta) + g_{ds2}}$</td>
<td>Input at the source of $M_2$, including body effect and $g_{ds} \neq 0$.</td>
</tr>
<tr>
<td>$a_{vcg} = \frac{[g_{m2}(1 + \eta) + g_{is2}]R_{D2}}{1 + g_{ds2}R_{D2}}$</td>
<td>Common-gate gain $V_{d2}/V_{s2} = V_{o2}/V_{s2}$ of $M_2$, including body effect.</td>
</tr>
<tr>
<td>$a_{af} = \frac{g_mR_s}{(R_{D1} + R_s)g_{ds1} + (1 + g_m(1 + \eta)R_s)}$</td>
<td>Source-follower gain $V_{s1}/V_{g1} = V_{s1}/V_i$ of $M_1$, including body effect.</td>
</tr>
<tr>
<td>$a_{v2} = a_{vsf}a_{vcg}$</td>
<td>Gain $V_{d2}/V_{g1} = V_{o2}/V_i$, including body effect, $g_{ds} \neq 0$.</td>
</tr>
</tbody>
</table>

### 8.12. Exercises and Projects

- **Project Mathcad Files**: Exercise09.mcd - Project09.mcd
- **Laboratory Project 9**: [MOSFET Differential Amplifier Stage](#)
- **P9.2**: [DC Evaluation of the Single-Power-Supply Differential Amplifier](#)
- **P9.3**: [Determination of the PMOS Parameters](#)
- **P9.4**: [Amplifier Gain Measurement](#)
- **P9.5**: [Transistor Parameters and DC Imbalance](#)
Unit 9. MOSFET Current Sources

With the evolution of integrated circuits, it was necessary to reduce the number of resistors in the circuit, and the solution was the transistor current source. An added bonus was that the circuit was generally greatly improved as well. Here, the basic principle is introduced, followed by a discussion of the standard method of increasing the current output resistance with source degeneration. The application of a current-source configuration for balancing a differential amplifier stage is discussed.

9.1. Basic Current Source

An example of a current source based on PMOS transistors is shown here in Fig. 9.1. It consists of the reference circuit, consisting of transistor $M_3$ and bias resistor $R_{bias}$. The reference-circuit transistor is diode connected. The induced $V_{SG3} = V_{SD3}$ is applied to the current-source transistor $M_2$. Thus, the drain current, or current-source current of $M_2$ is the mirror of the reference current. In an integrated circuit, any number of current sources can be referenced to the reference current or voltage. Current ratios are implemented with the selection of the relative gate widths of the transistors.

*Figure 9.1. PMOS current source. The current set up by the reference circuit of $M_3$ and $R_{bias}$ is mirrored as the current of $M_2$.*

The design of the reference circuit is based on a dc solution to the reference current, $I_{D3}$. The solution is obtained from the loop equation

Equation 9.1
\[ I_{D3} = \frac{V_{DD} + |V_{SS}| - V_{SG3}}{R_{bias}} \]

and transistor equation

**Equation 9.2**

\[ V_{SG3} = \sqrt{\frac{i_{D3}}{k_{p3} \left( 1 + \lambda_p V_{SG3} \right) + V_{tpo}}} \]

The current in M2 is

**Equation 9.3**

\[ I_{D2} = k_{p2} \left( V_{SG3} - V_{tpo} \right)^2 \left( 1 + \lambda_p V_{SD2} \right) \]

where

\[ k_{p2} = \frac{kP_p}{2} \frac{W_2}{L} \]

and

\[ k_{p3} = \frac{kP_p}{2} \frac{W_3}{L} \]

\( W_2 \) and \( W_3 \) are the transistor gate widths of M2 and M3, respectively, and L is the channel length. In general, the ratio of currents is

**Equation 9.4**

\[
\frac{I_{D2}}{I_{D3}} = \frac{\frac{W_2}{2} \left( 1 + \lambda_p V_{SD2} \right)}{\frac{W_3}{2} \left( 1 + \lambda_p V_{SG3} \right)} \approx \frac{W_2}{W_3}
\]
where the approximation can often be used for simplicity with long-channel devices. This avoids the necessity of knowing the source – drain voltages. The signal output resistance at the drain of $M_2$ is

\[
\frac{1 + \lambda_p V_{SD2}}{\lambda_p I_{D2}} \approx \frac{1}{\lambda_p I_{D2}}
\]

In the project of the current source, we will scan $V_{SD2}$ and compare the source current with the reference current.

### 9.2. Current Source with Source Degeneration

It is normally desirable to have the output resistance of a current source as large as possible. It can be improved over the circuit of Fig. 9.1 by adding resistance in the source branch, as shown in Fig. 9.2, to establish source degeneration (negative feedback). In the discussion of the signal circuit, it is necessary to represent the diode-connected transistor with its linear equivalent, which is just a resistance of magnitude, $1/g_m$. This can be seen by inspection of the circuit of Fig. 9.3. The voltage, $V_d$, is applied directly to the gate such that $V_{gs} = V_d$ and the drain current is $I_d = g_m V_d$. Thus the resistance of the diode is just $V_d/I_d = 1/g_m$. The result is the same for the PMOS and NMOS as is always true for signal linear models.

*Figure 9.2. Current-source circuit with source resistors to improve output resistance at drain of current-source transistor, $M_2$.***
The new output resistance at the drain of $M_2$ for the current-source circuit with source resistors (Fig. 9.2) can be derived based on the signal circuits shown in Fig. 9.4. The output resistance is defined as $R_o = V_o/I_o$, where $I_o$ is the drain current flowing in conjunction with the application of the test voltage $V_o$. Figure 9.4(b) replaces $M_3$ with the signal model equivalent and $M_2$ with the ideal, intrinsic transistor model (current source) along with output resistance, $1/g_{ds2}$. The transistor symbol represents the ideal transistor with output current $g_{m2}V_{sg2}$, positive in the direction shown.
The current $I_o$ flowing through the transistor and up through the resistor, $R_{S2}$, develops a voltage across the resistor, $V_{RS2} = I_o R_{S2}$. Since $I_{g2} = 0$, an input circuit loop equation is simply $V_{gs2} = -I_o R_{S2}$. The transistor linear-model current source, $g_{m2} V_{gs2}$, thus is down, as shown in the signal-circuit diagram of Fig. 9.4(b). The sum of currents through $1/g_{ds}$ is

Equation 9.6

$$I_{gds} = I_o \left(1 + g_m R_{S2} \right)$$

The voltage $V_o$ is thus

Equation 9.7

$$V_o = \frac{I_o \left(1 + g_m R_{S2} \right)}{g_{ds}} + I_o R_S$$

and the output resistance is

Equation 9.8
The magnitude can be assessed with the use of (4.5), which is $g_m = 2I_D/V_{effp}$. Eliminating $g_m$ in (9.8) results in

Equation 9.9

$$R_O = V_O \frac{1 + g_m R_S}{I_O} g_{ds2} + R_S$$

If the magnitude of the voltage across $R_{S2}$ is several volts, then $R_O$ is much greater than $1/g_{ds2}$, since $V_{eff2}$ is typically a fraction of a volt. In integrated circuits, $R_S$ may be replaced with an additional current source, in which case the expression becomes

Equation 9.10

$$R_O \approx \frac{2}{V_{eff2} \lambda p} \frac{1}{g_{ds2}}$$

where the output resistance of the added current source is approximately $1/I_D \lambda p$ ([4.13]).

**9.3. Differential Amplifier Balancing Circuit**

The principle of the balancing of the differential-amplifier stage (e.g., in an opamp) is often based on a circuit similar to that in Fig. 9.2, as shown in Fig. 9.5. Imbalance could be due, for example, to $V_{tp1} \neq V_{tp2}$ and $k_{p1} \neq k_{p2}$. Balancing is implemented by adjusting $R_1 \neq R_2$, where $R_1 = R_{S1}//R_x$ and $R_2 = R_{S2}//R_y$.

*Figure 9.5. Balancing circuit. Voltage $V_{D2}$ is controlled by selecting the relative values of $R_x$ and $R_y$.***
The relationship among the currents, parameters, and resistors is obtained by writing the loop equation around the source resistors and the gate–source terminals, which is

Equation 9.11

\[ I_D R_1 + \frac{I_D}{\sqrt{k_{p1}(1 + \lambda_p V_{SD1})}} + V_{tpo1} = I_D R_2 + \frac{I_D}{\sqrt{k_{p2}(1 + \lambda_p V_{SD2})}} + V_{tpo2} \]

A solution for \( V_{SD2} \) can be obtained from (9.11) for a given set of parameters, resistors, and bias variables; on the other hand, \( R_x \) and \( R_y \) are adjusted to obtain a certain \( V_{SD2} \).

For the special case of \( I_{D1} = I_{D2} = I_D \), the difference between the resistors in (9.11) is

Equation 9.12

\[ \delta R = R_1 - R_2 = \frac{V_{tpo2} - V_{tpo1} + \sqrt{\frac{I_D}{k_{p1}(1 + \lambda_p V_{SD1})}} - \sqrt{\frac{I_D}{k_{p2}(1 + \lambda_p V_{SD2})}}}{I_D} \]

For a numerical example, suppose the goal is to set \( V_{SD2} = V_{SD1} \) (\( V_{D2} = V_{D1} \)). By design, in (9.12),

Equation 9.13
\[
V_{SG1} = V_{SD1} = \frac{I_D}{k_p1(1+\lambda_p V_{SG1})} + V_{tno1} = V_{SD2}
\]

Any slight possible difference in \(\lambda_p\) is neglected.

In a practical opamp with this balancing configuration, the source nodes are connected to external pins. These pins are connected through external resistors \(R_x\) and \(R_y\) to \(V_{DD}\) as shown in Fig. 9.5. For adequate adjustment sensitivity, \(R_x\) and \(R_y\) are greater than \(R_{S1} \approx R_{S2}\) by at least a factor of 10. In practice, the external resistances are implemented with a potentiometer.

Assume that the transistor parameter values are \(V_{tpo1} = 1.49\) V, \(V_{tpo2} = 1.51\) V, \(k_p1 = 345\) \(\mu A/V^2\), \(k_p2 = 335\) \(\mu A/V^2\), and \(\lambda_p = 0.02\) V

\(\cdot\)

\(\mu A\). Also assume that the bias current \(I_D = 100\) \(\mu A\). We select \(R_{S1} = R_{S2} = R_S = 3\) k\(\Omega\) (Voltage \(I_D R_x = 0.3\) V) and we use \(R_x + R_y = R_{pot} = 25\) k\(\Omega\); the two resistors are segments of a 25-k\(\Omega\) potentiometer. The segments of the potentiometer are then determined from a solution to

Equation 9.14

\[
\frac{R_x}{R_x + R_S} - \frac{R_{pot} - R_x}{R_{pot} - R_x + R_S} = \frac{\delta R}{R_S}
\]

where \(\delta R\) is obtained from (9.12) with \(V_{SD2} = V_{SG1}\) as obtained from (9.13). The resistor values are \(R_x = 16\) k\(\Omega\) and \(R_y = 9\) k\(\Omega\) to give \(R_1 = 2.53\) k\(\Omega\) and \(R_2 = 2.25\) k\(\Omega\).

An evaluation of \(V_{SD2}\) without the balancing circuit can be made by setting \(\delta R = 0\) in (9.12) and for solving \(V_{SD2}\) to obtain

Equation 9.15

\[
V_{SD2} = \left[ \frac{I_D}{k_p2\left( V_{SG1} - V_{tpo2}\right)^2} \right] - 1 \frac{1}{\lambda_p}
\]

\(V_{SG1}\) is again obtained from (9.13).
With the numbers from the example above, \( V_{SD2} = 7.87 \text{ V} \). We note that with \( \lambda_p = 0.01 \text{ V}^{-1} \), the solution is \( V_{SD2} = 13.2 \text{ V} \) and the circuit might well have exceeded the powersupply limits. If \( V_{tpo1} = 1.45 \text{ V} \), \( V_{tpo2} = 1.55 \text{ V} \), and \( \lambda_p = 0.02 \text{ V}^{-1} \) that is, for an extreme case of the difference of threshold voltage, the balancing circuit will still function but now \( R_x = 21.8 \text{ k}\Omega \) and \( R_y = 3.24 \text{ k}\Omega \) with a small \( R_2 = 1.56 \text{ k}\Omega \).

### 9.4. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{I_{D2}}{I_{D3}} = \frac{\mu_2}{\mu_3} \frac{1 + \lambda_p V_{SD2}}{1 + \lambda_p V_{SG3}} \approx \frac{\mu_2}{\mu_3} )</td>
<td>Reference current, ( I_{D3} ), and current-source current, ( I_{D2} ), relation.</td>
</tr>
<tr>
<td>( R_O = \frac{V_O}{I_O} = \frac{1 + g_m R_{S2}}{g_{ds2}} + R_{S2} )</td>
<td>Output resistance of current-source with source degeneration.</td>
</tr>
<tr>
<td>( R_O = \left( \frac{2 I_{D2} R_{S2}}{V_{eff2}} \right) \frac{1}{g_{ds2}} + R_{S2} )</td>
<td>Output resistance of current-source with source degeneration and ( g_m = 2I_D/V_{effp} ).</td>
</tr>
<tr>
<td>( \delta R = \frac{V_{tpo2} - V_{tpo1} + \left[ \frac{I_D}{k_p (1 + \lambda_p V_{SD2})} \right] - \left[ \frac{I_D}{k_p (1 + \lambda_p V_{SG3})} \right]}{I_D} )</td>
<td>Relation for setting ( V_{D2} ) in balancing circuit with ( R_1 = R_{S1}/R_x ) and ( R_2 = R_{S2}</td>
</tr>
<tr>
<td>( \delta R = R_1 - R_2 )</td>
<td></td>
</tr>
<tr>
<td>( V_{SD1} = \frac{I_D}{k_p (1 + \lambda_p V_{SD1})} + V_{no1} = V_{SD2} )</td>
<td>Relation for ( V_{D2} = V_{D1} ) for ( I_{D1} ) ( I_{D2} = I_D ).</td>
</tr>
<tr>
<td>( V_{SD2} = \left( \frac{I_D}{k_p (V_{SG3} - V_{tpo2})^2} - 1 \right) \frac{1}{\lambda_p} )</td>
<td>( V_{SD2} ) for unbalanced circuit with ( \delta R = 0 ) and ( I_{D1} = I_{D2} = I_D ).</td>
</tr>
</tbody>
</table>

### Unit 10. Common-Source Amplifier with Current-Source Load

The amplifier in this part is the same, in principle, as the basic common-source amplifiers of Figs. 2.4 and 5.1. However, now the actual resistor \( R_D \) is replaced with a current-source load as shown in the circuit of Fig. 10.1. As noted in Unit 9, a benefit of replacing bias resistors with current sources is a reduced requirement for resistors in the circuit; the reference voltage associated with \( M_3 \) can be used elsewhere in a typical circuit. Additionally, as will be shown, the gain of the common-source stage is substantially improved over that with actual bias resistor \( R_D \). The specific circuit of Fig. 10.1 is that for the project amplifier. The bias and gain of the amplifier are evaluated in the following.

**Figure 10.1.** Common-source amplifier with driver transistor \( M_1 \) and current-source load from drain of \( M_2 \). In the amplifier project, an output channel sets
$V_{G1}$ for a given current and another output channel will search for the $V_{SS}$ to set up bias $V_O = V_{DD}/2$. For the signal measurements, a signal voltage is superimposed on the dc $V_{G1}$.

10.1. DC (Bias) Circuit

The bias circuit is critical in terms of getting the dc output voltage at a value near the project design value of $V_O = V_{DD}/2$ (for maximum output magnitude and linearity). The relation, from the dc circuit analysis, for obtaining this condition is based on $I_{D1} = I_{D2}$. This is, in terms of the transistor characteristic equations, (3.8),

Equation 10.1

\[
k_{p2} (V_{GS} - V_{tpo})^2 (1 + \lambda_p V_{DD} / 2) = k_{n1} (V_{GS} - V_{tno})^2 (1 + \lambda_n V_{DD} / 2)
\]

Note that the source-gate voltage of $M_2$ is referenced to $M_3$. A certain combination of $V_{GS1}$ and $V_{SS}$ will satisfy $V_o = V_{DD}/2$. In the project on the amplifier, a LabVIEW VI sends out a $V_{G1} = V_{GS1}$ to set up a given $I_{D1} = I_{D2}$ and then adjusts $V_{SS}$ to obtain the desired bias output voltage.

Figure 10.2 shows a SPICE plot of the current for the PMOS and NMOS transistors as a function of $V_{DS1}$. The source – drain voltage for the PMOS is $V_{SD2} = V_{DD} - V_{DS1}$. Both transistors have a specific gate – source voltage. The solution for the output voltage for this case is about 3 V. A slight decrease in $V_{GS1}$ or a slight increase in $V_{SG2}$ is required to bring $V_{DS1}$ to 5 V, the design result in this example. The increase in $V_{SG2}$ would be implemented by making $V_{SS}$ more negative to increase the reference current. The steeper slope in the active region of the PMOS device is consistent with $\lambda_p > \lambda_n$, as in the project amplifier.
Figure 10.2. Plot of driver and load transistor output characteristics on common voltage scale. Since $I_{D1} = I_{Dn} = I_{D2} = I_{Dp}$, $V_{DS1} = V_O$ is where currents intersect. The current from the current source load needs, in this example, to be slightly increased to set $V_{DS1} = V_O$, with $V_{DD} = 5V$.

10.2. Signal Voltage Gain

The expression for the gain of the basic common-source amplifier, (5.4), which includes the output resistance of the driver transistor, is

$$a_v = -g_m \frac{R_D}{1 + g_{ds}R_D}$$

In the signal circuit, as shown in Fig. 10.3, $R_D$ is replaced by $1/g_{ds2}$. The new equation for this circuit is

Equation 10.2

$$a_v = -\frac{g_m}{g_{ds1} + g_{ds2}}$$

Figure 10.3. Linear circuit of the common-source amplifier. The load is now the output resistance of the current source load, $1/g_{ds2}$. 
or with \( g_m = 2I_D/V_{eff} \), (4.5), and \( g_{ds} \approx I_D \lambda_n \), (4.13),

Equation 10.3

\[
a_v \approx -\frac{g_{m1}}{\left(\lambda_n + \lambda_p\right)I_{D1}} \approx -\frac{2}{\left(\lambda_n + \lambda_p\right)V_{eff1}}
\]

The result shows that the gain increases for decreasing \( V_{eff1} \). This is limited by the fact that the MOSFET ceases to behave in the normal manner at some lower limit on \( V_{eff} \).

Using \( g_{m1} \approx 2\sqrt{n_1}I_{D1} \) an alternative form is obtained, which reveals the \( I_{D1} \) dependence of the gain. This is

Equation 10.4

\[
a_v \approx -\frac{2}{\lambda_n + \lambda_p} \frac{n_1}{\sqrt{I_{D1}}}
\]

Increasing gain is achieved with decreasing the level of bias current. The lower limit is, as noted above, associated with a lower limit on \( V_{eff} \). Also, there is an approximate inverse trade-off between frequency response limitations, on the high end of the spectrum, and gain.

The gain, though, for the amplifier with current source load, will generally be several times as large as that with the resistive load. An amplifier with even higher gain can be obtained by replacing the current source load with one with source degeneration as discussed in Unit 9.2, and as discussed extensively for the case of the BJT in Unit C.
10.3. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ k_{\text{p2}} (V_{\text{GS}} - V_{\text{Ip0}}) (1 + \lambda_p V_{\text{DD}} / 2) = k_{\text{m1}} (V_{\text{GSL}} - V_{\text{Ino}}) (1 + \lambda_n V_{\text{DD}} / 2) ]</td>
<td>Output drain-current balance equation.</td>
</tr>
<tr>
<td>[ a_v = - \frac{g_{\text{m1}}}{g_{\text{es1}} + g_{\text{ds2}}} ]</td>
<td>Voltage-gain equation.</td>
</tr>
<tr>
<td>[ a_v \approx - \frac{g_{\text{m1}}}{(\lambda_n + \lambda_p) I_D} \approx - \frac{2}{(\lambda_n + \lambda_p) V_{\text{efn1}}} ]</td>
<td>Voltage-gain equation in terms of ( \lambda )'s and ( V_{\text{efn1}} ).</td>
</tr>
<tr>
<td>[ a_v \approx - \frac{2}{\lambda_n + \lambda_p} \sqrt{I_D} ]</td>
<td>Voltage-gain equation in terms of ( \lambda )'s and ( I_D ).</td>
</tr>
</tbody>
</table>

10.4. Exercises and Projects

Project Mathcad Files

Exercise10.mcd - Project10.mcd

Laboratory Project

10 Current Mirror and Common-Source Amplifier with Current-Source Load

P10.2 Evaluation of the Current-Source Circuit

P10.3 Evaluation of the Mirror-Current Circuit

P10.4 Evaluation of the Bias Setup

P10.5 Measurement of the Amplifier Gain versus Drain Current

Unit 11. Operational Amplifiers with Resistor Negative Feedback

In the following units we consider the operational amplifier in the basic resistive feedback amplifier configurations. We discuss gain, dc offset, and frequency response. In projects, the opamp is implemented in the noninverting amplifier mode to evaluate voltage again, opamp offset, bias stabilization, and amplifier and opamp frequency response.

11.1. Operational Amplifiers with Resistance Feedback

In this unit, the gain characteristics of the operational amplifiers with resistive feedback are discussed. These are dc amplifiers that are configured for specific gain and input and output resistance characteristics. The operational amplifier without feedback is in the open-loop mode. The dc (bias) configuration is shown in Fig. 11.1. Due to imbalances in the amplifier circuit, which are a result of variations in the parameters of the transistors and circuit components from the values used in the design, the output will probably be latched at either the plus or minus power supply.
Figure 11.1. Open-loop amplifier. Inputs, output, and power-supply pins are connected. Circuit will be bias unstable. Dc $V_O$ is likely to be latched at near $V_{DD}$ or $V_{SS}$.

The circuit can be set into a stable, active mode with the output approximately at zero volts by providing resistive negative feedback as shown in the circuit diagram of Fig. 11.2.

Figure 11.2. Opamp resistor network, including feedback resistor for bias stabilization. Signal output voltage is $V_o = a_vV_e$.

The resistor connected between the output, $V_O$, and the inverting (minus) input effectively applies the output voltage to the opamp input and it is of such a polarity as to drive the output toward zero volts, where it tends to stay. That is, attaching the resistor completes the negative feedback loop from $V_e$ to $V_{RY}$. The quantitative aspects of stabilization with the feedback resistor are discussed in Unit 11.6.

This circuit becomes a dc amplifier by installing a signal at either input. These two possibilities are discussed in the following units.
11.1.1. Voltage Gain of the Noninverting Resistor Feedback Amplifier

In the circuit diagram of Fig. 11.3, an input signal voltage $V_s$ is attached to resistor $R_x$. By definition, the output terminal voltage is positive for a plus input. Hence, this is the noninverting amplifier. Here we obtain the relationship between the amplifier gain, $a_{vo} = \frac{V_o}{V_s}$, and the open-loop gain (opamp gain), $a_{vo} = \frac{V_o}{V_e}$, and the circuit resistors.

*Figure 11.3. Non-inverting or voltage amplifier (series-shunt). The input resistance is essentially infinite.*

With a signal applied to the plus input terminal, the responding output voltage is fed back to the resistor $R_y$. The voltage across $R_y$, $V_f$, and $V_o$ (signal) are related by

**Equation 11.1**

$$V_f = \frac{R_y}{R_y + R_f} V_o$$

This is just the voltage-divider relation, which applies in this case, as negligible current flows into the input terminals of the opamp. Variable $V_f$ is used in lieu of $V_{R_y}$ to distinguish it from the dc value of the voltage across $R_y$. This use is also consistent with the fact that $V_f$ is technically a signal feedback voltage.

The input signal voltage $V_s$ adds up to

**Equation 11.2**

$$V_e = V_s + V_f = \frac{V_o}{a_{vo}} + \frac{R_y}{R_y + R_f} V_o$$
where (11.1) is used to eliminate $V_f$. (The voltage drop across $R_x$ is essentially zero.) This leads directly to the relation for amplifier gain, which is

Equation 11.3

$$A_v = \frac{V_o}{V_s} = \frac{1}{1 + \frac{1}{a_v \cdot \frac{R_f}{R_y}}} = \frac{A_{vNI}}{1 + \frac{A_{vNI}}{a_v \cdot \frac{R_f}{R_y}}}$$

with (ideal noninverting gain).

Equation 11.4

$$A_{vNI} = 1 + \frac{R_f}{R_y}$$

$A_{vNI}$ is the limiting form of the noninverting amplifier gain for $a_{vo} \to \infty$. This is consistent with the fact that in the limit, $V_\xi \to 0$ and $V_s = V_{RY}$. Thus, the output and input voltages are simply related by the voltage-divider relation. The result, (11.3), indicates that for $a_{vo} \gg A_{vNI}$, the voltage gain can simply be expressed in terms of the resistors and therefore is very predictable. If we make, for example, $R_f = 10R_y$, $A_{vNI} = 11$, and (11.3) gives $A_v = 10.998$, with $a_{vo} = 40,000$. The value for the opamp gain is typical for our project opamp. Note that due to the high resistance at the opamp input terminals, $R_x$ has no influence on the gain.

The noninverting amplifier has a very high input resistance and a low output resistance, as discussed in Unit 11.4. The amplifier technically falls into the category of a series – shunt feedback configuration or a voltage amplifier.

11.1.2. Voltage Gain of the Inverting Resistor Feedback Amplifier

To obtain the inverting amplifier, the signal is applied to the negative or inverting terminal as shown in Fig. 11.4. A positive signal results in a negative output voltage. The gain expression can be obtained with the loop equation from output to input:

Equation 11.5

$$V_s - V_o = I_s R_y + I_s R_f$$
and the loop equation at the input (voltage drop across $R_x$ is zero)

Equation 11.6

$$V_s = I_s R_y + V_z = I_s R_y + \frac{V_o}{a_v}$$

Eliminating $I_s$ between (11.5) and (11.6) gives

Equation 11.7

$$V_s = \frac{V_o}{a_v} + \frac{V_s - V_o - R_y}{R_y + R_f}$$

This expression can be manipulated to give the gain as

Equation 11.8

$$\frac{V_o}{V_s} = \frac{R_f}{R_y} \cdot \frac{1}{\frac{1}{a_v} - \frac{1}{R_y + R_f}}$$
which is

Equation 11.9

\[ A_v = A_{ol} \frac{1}{1 - \frac{A_{vI}}{A_{ol}}} \]

where

Equation 11.10

\[ A_{vI} = -\frac{R_f}{R_y} \]

\( A_{vI} \) is the gain of the ideal inverting amplifier.

The ideal gain, as in the case of the noninverting amplifier, depends only on resistor values. The approximate form is based on the approximation \( V \epsilon = 0 \), in which case the negative input terminal is at virtual ground. Thus, \( |v_o| \) and \( V_s \) are proportional to \( R_f \) and \( R_y \), respectively. The inverting-amplifier gain result includes the fact that the current into the negative terminal is zero. The circuit is a shunt – shunt feedback configuration or a transresistance amplifier.

11.2. Output Resistance of the Resistor Feedback Amplifier

The negative feedback of the amplifiers will alter the output resistance of the circuit. In the case of series – shunt feedback (noninverting amplifier) and the shunt – shunt (inverting amplifier), the output resistance will be reduced from that of the open-loop amplifier. This can be explained with the use of the circuit of Fig. 11.5, which shows a linear-model circuit for the amplifiers of Figs. 11.3 and 11.4, with the inputs set to zero.

Figure 11.5. Linear equivalent circuit for deriving opamp output resistance. Test voltage, \( V_o \), is applied at the opamp output. The inputs are grounded for deriving the output resistance.
For the present purposes, a voltage-dependent voltage source equivalent circuit for the opamp is chosen. The parameter \( r_o \) is the output resistance of the open-loop opamp. For example, the output resistance would be about \( 1/g_m \) in a CMOS opamp with a source-follower stage-output stage.

A test voltage, \( V_o \), is applied at the output terminal with the input grounded. This results in an input to the opamp of magnitude \( V\mathcal{E} = V_o/A_{vNI} \). The voltage-dependent voltage source of the opamp is thus \( (a_{vo}/A_{vNI})V_o \). The total current, \( I_o \), flowing from the test voltage is then

Equation 11.11

\[
I_o = \left( \frac{1}{R_f + R_y} + \frac{1 + a_{vo}/A_{vNI}}{r_o} \right) V_o = \left( \frac{r_o}{R_f + R_y} + \frac{1 + a_{vo}/A_{vNI}}{r_o} \right) \frac{V_o}{r_o}
\]

Therefore, the output resistance is

Equation 11.12

\[
R_o = \frac{V_o}{I_o} = \frac{r_o}{\frac{r_o}{R_y + R_f} + \frac{1 + a_{vo}/A_{vNI}}{1 + T}} \approx \frac{r_o}{1 + T}
\]

where \( T = a_{vo}/A_{vNI} \) (i.e., the loop gain of the feedback amplifier). The approximate form comes from the expectation that \( r_o \ll R_y + R_f \); it neglects the current through the feedback resistors. \( R_o \approx r_o/T \) is a valid approximation in most cases and \( R_o \ll r_o \). For example, for \( A_{vNI} \approx 10 \) and \( a_{vo} \approx 40,000 \), \( T = 4000 \), and \( R_o \approx r_o/4000 \).
11.3. Operational Amplifier Offset

Ideally, an opamp is balanced such that the dc output is zero (with dual power supply) with zero input voltage (as in Fig. 11.1). In practice, this is not realized, due to the variation of parameters between similar transistors and components. As mentioned above, the opamp configuration of Fig. 11.1 will probably be locked at near the positive or negative rail voltage. Thus, a given opamp requires an input voltage \( V_{\text{in}} \) to set the output to zero. The magnitude of this voltage is defined as offset voltage \( V_{\text{off}} \).

An equivalent circuit that includes the offset voltage is given in Fig. 11.6. The imperfections of the amplifier are reflected into the offset voltage and the opamp is ideal. If \( V_i \) is made equal to \( V_{\text{off}} \), the output \( V_O \) will be zero. Suppose that \( V_i = 0 \). In this case we have the equivalent of \( V_{\text{off}} \) applied to the input and the output is driven toward the plus or minus power-supply voltages (depending on the polarity of \( V_{\text{off}} \)). \( V_{\text{off}} \) is usually large enough to cause the amplifier to be driven out of the active mode. For example, a typical \( V_{\text{off}} \) is \( V_{\text{off}} = 1 \) mV. Thus, if \( a_{\text{vo}} = 40,000 \), the output will attempt to become \(-40 \) V, which is probably greater than the supply voltage value; the output is set at the negative limit. In our project opamp, this will be roughly \( V_{SS} + 50 \) mV if driven negative or \( V_{DD} - 1V \) if driven toward the positive supply.

Figure 11.6. Ideal opamp with offset voltage. With dc input voltage \( V_i = V_{\text{off}}, V_O = 0 \). With \( V_i = 0 \) (grounded input), \( V_O \approx V_{DD} \) or \( V_{SS} \) with \( |a_{\text{vo}}V_{\text{off}}| > V_{DD} \) or \( |V_{SS}| \) for \( V_{\text{off}} \) negative or positive, respectively.

11.4. DC Stabilization with the Feedback Resistor

The dc output voltage can be set close to zero with negative feedback for normal operation as a linear amplifier as illustrated in Fig. 11.7. A portion of the output voltage is applied back to the input as the voltage across \( R_y \). This is

Equation 11.13

\[
V_{R_y} = \frac{R_y}{R_y + R_F} V_O
\]
Figure 11.7. Opamp dc stabilized with feedback resistor network. The output voltage is applied back to the input to then drive the output toward a smaller value. The voltage across $R_y$ will be about equal to $V_{off}$ and $V_O$ is forced to near zero.

(Dc $V_O$ is used, as this is a no-signal or bias state under consideration.) This voltage will cancel most of $V_{off}$, such as to drive $V_O$ close to zero if $R_f$ is small enough compared to $R_y$. The value of $V_O$ for a given $R_f$ can be obtained as follows: A loop equation at the input side (Fig. 11.7) gives

Equation 11.14

$$\frac{R_y}{R_y + R_f} V_O + V_z + V_{off} = 0$$

The opamp circuit is a dc amplifier. Therefore, the input – output relation holds for dc as well as for signals. Thus, $V_c = V_O/a_{vo}$ such that

Equation 11.15

$$\frac{R_y}{R_y + R_f} V_O + \frac{V_O}{a_{vo}} + V_{off} = 0$$

and

Equation 11.16
where the approximation usually applies and is equivalent to $V_e = 0$.

For example, with $V_{off} = 1 \, \text{mV}$ and $A_{VN1} = 100$, $V_o \approx -0.1 \, \text{V}$. This would be a very satisfactory dc state for using the circuit as an amplifier. Also, the approximation of the right-hand side of (11.16) is quite valid. Note that without the feedback network, $V_o = -a_{vo} V_{off} = -40,000 \cdot 1 \, \text{mV} = -40 \, \text{V}$. Assuming that the power-supply voltage is, for example, $\pm 15 \, \text{V}$, the output is locked at $V_o \approx -15 \, \text{V}$ and the linear gain relation does not apply. In our project with the opamp, we determine $V_{off}$ from a measurement of $V_o$ and the application of (11.16).

### 11.5. Frequency Response of the Operational Amplifier and Resistor Feedback Amplifier

The MOSFET has a number of capacitances, including those associated with the gate structure and source and drain pn junctions as well as other parasitic capacitors of the transistor and the circuit. Therefore, the open-loop opamp will tend to be unstable due to the poles and zeros associated with the capacitors. Opamps are usually stabilized with the addition of a capacitor. The added pole is well below the lowest naturally occurring pole. This pole will dominate the frequency response of the opamp. In a lab project, the pole frequency will be measured.

We will obtain the frequency response of the feedback amplifier based on the single-pole response. The form of the response of the open-loop opamp is

Equation 11.17

$$a_v(f) = \frac{a_{vo}}{1 + j \frac{f}{f_{3dB \, \text{opamp}}}}$$

The response function has value $a_{vo}$ at low frequencies and has magnitude $a_{vo} / \sqrt{2}$ at $f = f_{3dB \, \text{opamp}}$, where $f_{3dB \, \text{opamp}}$ is the characteristic frequency of the opamp. This is indirectly, $f_{3dB \, \text{opamp}} = \frac{GBP}{a_{vo}}$, where GBP is the gain – bandwidth product of the opamp as given in the datasheet. Datasheet value $a_{vo}$ is also given ($A_{vd}$, large-signal voltage gain).

The noninverting feedback amplifier has a gain as given by (11.3). That expression is used here along with (11.17) in place of $a_v$. The frequency response of the feedback amplifier is thus
Equation 11.18

\[ A_v(f) = \frac{A_{\text{vNI}}}{1 + \frac{A_{\text{vNI}}}{A_v(f)}} \]

which is

Equation 11.19

\[ A_v(f) = A_{\text{vNI}} \left( \frac{1}{1 + j\frac{f}{f_{\text{3dB}} \text{opamp}}} \right) = \frac{A_{\text{vNI}}}{1 + \frac{A_{\text{vNI}}}{a_v \left( \frac{1}{1 + j\frac{f}{f_{\text{3dB}} \text{opamp}}} \right)}} \]

This can be simplified to

Equation 11.20

\[ A_v(f) = \frac{A_{\text{vNI}}}{1 + \frac{A_{\text{vNI}}}{a_v \left( 1 + j\frac{f}{f_{BW}} \right)}} = \frac{A_v(0)}{1 + j\frac{f}{f_{BW}}} \]

where \( A_v(0) \) is the amplifier gain at low frequencies and where

Equation 11.21

\[ f_{BW} = f_{\text{3dB \text{opamp}}} \left( 1 + \frac{a_v}{A_{\text{vNI}}} \right) = f_{\text{3dB \text{opamp}}} \left( 1 + a_v \frac{R_y}{R_y + R_f} \right) \]

Frequency parameter \( f_{BW} \) is the bandwidth of the amplifier for a specific \( A_{\text{vNI}} \). Parameter \( f_{BW} \), by definition of bandwidth, is also \( f_{\text{3dB}} \) of the amplifier. Adding feedback by reducing \( R_f \) always increases bandwidth at the expense of gain. Note that for \( R_f \) very small, \( f_{BW} \) can be relatively high and the frequency response is complicated by the fact that other poles of the opamp come into play.

Given in Table 11.1 is a segment from the manufacturer's datasheet for the opamp (TS271C) used in our project. As mentioned above, the parameter for large-signal voltage
gain is designated as $A_{vd}$ and is identical to $a_{vo}$. The GBP indicated is 700 kHz. Thus for a low-frequency amplifier gain of, for example, $A_v = 5000$, the bandwidth is $f_{BW} = 700$ kHz/5K = 140 Hz, which can be readily measured using LabVIEW and the DAQ in the computer.

<table>
<thead>
<tr>
<th>TABLE 11.1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Symbol</strong></td>
</tr>
<tr>
<td>$A_{vd}$</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>GBP</td>
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</tbody>
</table>

Note that for the limiting case of $R_f \to \infty$, the bandwidth of the open-loop amplifier is only $f_{3dB} = 700$ kHz/50K = 14 Hz, where the typical (Typ.) number, $A_{vd} = 50$ k has been used.

### 11.6. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_v = \frac{A_{vNI}}{1 + \frac{A_{vNI}}{a_{vo}}}$</td>
<td>Noninverting feedback amplifier voltage gain.</td>
</tr>
<tr>
<td>$A_{vNI} = 1 + \frac{R_f}{R_y}$</td>
<td>Ideal noninverting amplifier voltage gain.</td>
</tr>
<tr>
<td>$A_v = A_{vI} \left( 1 - \frac{1 - A_{vI}}{a_{vo}} \right)$</td>
<td>Inverting feedback amplifier voltage gain.</td>
</tr>
<tr>
<td>$A_{vI} = -\frac{R_f}{R_y}$</td>
<td>Ideal inverting amplifier voltage gain.</td>
</tr>
<tr>
<td>$R_o = \frac{\frac{r_o}{r_y + R_f}}{1 + \frac{a_{vo}}{A_{vNI}}}$</td>
<td>Output resistance of the resistance-feedback opamp amplifier.</td>
</tr>
<tr>
<td>$T = a_{vo}/A_{vNI}$</td>
<td>Loop gain of resistance-feedback opamp amplifier.</td>
</tr>
</tbody>
</table>
Noninverting feedback amplifier voltage gain.

\[ A_v = \frac{A_{vNI}}{1 + \frac{A_{vNI}}{a_{vo}}} \]

<table>
<thead>
<tr>
<th>Noninverting feedback amplifier voltage gain.</th>
</tr>
</thead>
</table>

Output voltage of resistance-feedback opamp with offset voltage, \( V_{off} \).

\[ V_o = \frac{-A_{vNI}}{1 + \frac{A_{vNI}}{a_{vo}}} V_{off} = \frac{-A_{vNI}V_{off}}{1 + \frac{A_{vNI}}{a_{vo}}} \]

<table>
<thead>
<tr>
<th>Output voltage of resistance-feedback opamp with offset voltage, ( V_{off} ).</th>
</tr>
</thead>
</table>

Frequency-response function of resistance-feedback opamp amplifier.

\[ A_v(f) = \frac{A_{vNI}}{1 + \frac{A_{vNI}}{a_{vo}}} \left( \frac{1}{1 + j \frac{f}{f_{BW}}} \right) = A_{vo} \left( \frac{1}{1 + j \frac{f}{f_{BW}}} \right) \]

<table>
<thead>
<tr>
<th>Frequency-response function of resistance-feedback opamp amplifier.</th>
</tr>
</thead>
</table>

Bandwidth (corner frequency) of opamp amplifier with opamp open-loop corner frequency, \( f_{3dB} \).

\[ f_{BW} = f_{3dB} \left( 1 + \frac{a_{vo}}{A_{vNI}} \right) = f_{3dB} \left( 1 + a_{vo} \frac{R_y}{R_y + R_f} \right) \]

<table>
<thead>
<tr>
<th>Bandwidth (corner frequency) of opamp amplifier with opamp open-loop corner frequency, ( f_{3dB} ).</th>
</tr>
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</table>

### 11.7. Exercises and Projects

Project Mathcad Files  Exercise11.mcd - Project11.mcd

Laboratory Project 11  Operational Amplifier with Resistor Feedback

P11.2  Bias Circuit Setup

P11.3  Opamp Offset Voltage

P11.4  Evaluation of the Bias Balancing Circuit

P11.5  Evaluation of the Gain and Signal Limits with Swept Input

P11.6  Evaluation of the Gain with Sine-Wave and Square-Wave Signals

P11.7  Determination of the Opamp Frequency Response

### Unit 12. Operational Amplifier Applications with Capacitors

In this unit we consider the most common applications of operational amplifiers where the circuit uses a capacitor as the key component. Included are the opamp integrator and a basic opamp square-wave oscillator. Both forms are investigated in projects.

#### 12.1. Operational Amplifier Integrator

The noninverting or inverting resistance-feedback amplifier can be converted into an integrator with the addition of a feedback capacitor, \( C_f \), as shown in Fig. 12.1.

Specifically, the feedback resistor is replaced with \( C_f \), except that the resistor \( R_f \) must remain for dc stabilization purposes.
Figure 12.1. Opamp integrator. The resistor $R_f$ in shunt with $C_f$ is for opamp stabilization purposes.

The operation of the integrator can be explained as follows. For the initial discussion, assume that $R_f$ is infinite. Upon application of a constant voltage $V_s$, a current is induced in $R_y$, which is

Equation 12.1

$$i_{R_f} = i_{C_f} = \frac{V_s - V_{es}}{R_y} \frac{V_s}{R_y}$$

The approximation relies on the fact that $V_{es} \approx 0$, which can be expected. The resulting output voltage is

Equation 12.2

$$v_o(t) = V_s + \frac{1}{C_f} \int I_y \, dt = V_s + \frac{1}{R_y C_f} \int v_s \, dt$$

To a good approximation, $v_o(t)$ is proportional to the integral of the input. Performing the integration, the result is

Equation 12.3

$$v_o(t) = V_s + \frac{V_s}{R_y C_f} t$$
If $V_s$ is the magnitude of a square-wave, the output will be a triangular wave. In the integrator project we explore the integrator by using it to generate a triangular wave. The project design calls for a peak of the triangular wave equal to a few volts, that is, a significant portion of the power-supply voltage. The time of integration for the plus or minus segment of the square-wave input is $T/2$, where $T$ is the period and $T = 1/f$, that is, the inverse of the square-wave frequency. The peak of the triangular wave then is based on

Equation 12.4

$$2V_{\text{peak}} \approx \frac{V_s T}{2 R_y C_f}$$

The $2V_{\text{peak}}$ is due to the fact that the integration is from minus $V_{\text{peak}}$ to plus $V_{\text{peak}}$. The voltage drop across $R_y$ has been neglected in the output.

Suppose we choose $C_f$ as the design parameter where $V_s$, $T$, $V_{\text{peak}}$, and $R_y$ (from Unit 11) are given. The capacitor is then selected according to

Equation 12.5

$$C_f = \frac{V_s T}{2 \cdot 2V_{\text{peak}} R_y}$$

For example, for $V_s = 1 \text{ mV}$, $V_{\text{peak}} = 5 \text{ V}$, $R_y = 220 \Omega$ and $T = 1 \text{ mS}$ ($f = 1 \text{ kHz}$), $C_f = 23 \text{ nF}$.

In the integrator project, a sine-wave source is used. The integrated output for this case is

Equation 12.6

$$v_o(t) = V_s \sin \left( \frac{2\pi t}{T} \right) + \frac{T}{2\pi R_y C_f} V_s \cos \left( \frac{2\pi t}{T} \right)$$

The sine term can be neglected and the resulting formulation can be used to predict the peak of the cosine for a given $C_f$ and peak $V_s$. 
A more general solution for the output voltage for the noninverting integrator includes the current through the resistor $R_f$. If we neglect the voltage across $R_y$, (12.2) becomes, for this case (constant input or square-wave input):

Equation 12.7

$$v_o(t) = \frac{1}{C_f} \int \left( \frac{V_s}{R_y} - \frac{v_o(t)}{R_f} \right) dt$$

The solution is

Equation 12.8

$$v_o(t) = \frac{V_s}{R_y C_f} \left( 1 - e^{-t/R_f C_f} \right)$$

Replacing the exponential with the first three terms of an infinite series gives

Equation 12.9

$$v_o(t) = \frac{V_s}{R_y C_f} \left( 1 - \frac{t}{R_f C_f} + \frac{t^2}{2R_f C_f^2} \right)$$

This demonstrates that for the circuit to function properly as an integrator, the choice of $R_f$ should satisfy $R_f C_f >> T/2$. In the above example, $C_f = 23$ nF. With this capacitor and $R_f = 1$ MΩ, for example, $R_f C_f = 23$ ms, compared with $T/2 = 0.5$ ms. The magnitude of $R_f$ must also satisfy the requirement of sustaining the operational amplifier in the active mode. The solution for the periodic square-wave input, giving an approximate triangular-wave output, unlike (12.8), includes the fact that the transient does not start at zero volts. This case is considered in Exercise12.mcd, Part 2. The output voltage function equivalent to (12.2) for the inverting-mode integrator is

Equation 12.10

$$v_o(t) = -\frac{1}{R_y C_f} \int V_s dt$$
This would apply to the circuit of Fig. 12.1 with the plus input grounded and the source, $V_s$, attached at the grounded end of $R_y$.

### 12.2. Operational Amplifier Oscillator

The opamp can serve as a square-wave oscillator by adding positive feedback with $R_1$ and $R_3$ and replacing $R_y$ with a capacitor $C_o$, as shown in Fig. 12.2. The frequency of the operation can be computed on the basis of the following derivation. With positive feedback, the circuit is unstable and the output voltage is either $V_{op}$ or $-V_{om}$, that is, the positive or negative limit. The limits are close to $V_{DD}$ or $V_{SS}$. These voltage values are applied to the input through the positive feedback network such that the plus input terminal is either at

**Equation 12.11**

$$V_{op} = \frac{R_3}{R_3 + R_1} V_{op}$$

or

**Equation 12.12**

$$V_{om} = -\frac{R_3}{R_3 + R_1} V_{om}$$

*Figure 12.2. Opamp oscillator. The frequency is determined by the value of resistors and the capacitor.*
where $V_{om}$ is positive.

However, the negative-feedback circuit consisting of $R_f$ and $C_o$ will cause the capacitor to charge up toward the voltage at the output. For example, suppose that for an interval of time, $v_o(t) = V_{op} \approx V_{DD}$. Also assume that $R_3 = R_1$ such that the plus input is at $V_{op}/2$. When the capacitor charges up to and just beyond $V_{op}/2$, the opamp input $V_C$ changes sign and the output will switch over to $v_o(t) = -V_{om}$. At this point, the capacitor begins charging toward the opposite polarity, and so forth.

For a given output, the time-dependent capacitor voltage is a simple RC transient. For example, for $v_o(t) = V_{op}$,

Equation 12.13

$$v_{c_o}(t) = K e^{\frac{-t}{R_fC_o}} + V_{op}$$

with a steady-state value of $V_{op}$. As an oscillator, the capacitor voltage will never reach the steady-state value; the transient terminates at the value given by (12.11).

The output is switching back and forth from $V_{op}$ to $-V_{om}$. Therefore, the initial value of the capacitor voltage in (12.13) is

Equation 12.14

$$v_{c_o}(0) = \frac{-R_3}{R_3 + R_1} V_{om}$$

Using this to obtain a complete solution for (12.13) results in

Equation 12.15

$$v_{c_o} + (t) = \left( -V_{op} - \frac{R_3}{R_3 + R_1} V_{om} \right) e^{\frac{-t}{R_fC_o}} + V_{op}$$

We define $t = T_{plus}$ as the positive time segment of the square-wave period. As noted, this corresponds to the time where the output switches to $-V_{om}$; that is,
Equation 12.16

\[ v_{C_0} + \left( T_{\text{plus}} \right) = \frac{R_3}{R_3 + R_1} v_{O_{p}} \]

Using (12.16) in the left-hand side of (12.15) gives an equation for \( T_{\text{plus}} \) as follows:

Equation 12.17

\[ \frac{R_3}{R_3 + R_1} v_{O_{p}} = \left( -v_{O_{p}} - \frac{R_3}{R_3 + R_1} v_{O_{m}} \right) e^{-\frac{T_{\text{plus}}}{R_f L_{C_0}}} + v_{O_{p}} \]

Then, solving for \( T_{\text{plus}} \) results in

Equation 12.18

\[ T_{\text{plus}} = -R_f C_0 \ln \left( \frac{v_{O_{p}} + \frac{R_3}{R_3 + R_1} v_{O_{m}}}{\frac{R_1}{R_3 + R_1} v_{O_{p}}} \right) \]

Following the reasoning that led to (12.15), the falling capacitor-voltage transient is

Equation 12.19

\[ v_{C_0}(t) = \left( v_{O_{m}} + \frac{R_3}{R_3 + R_1} v_{O_{p}} \right) e^{-\frac{t}{R_f C_0}} - v_{O_{m}} \]

The total time interval (negative segment of the square-wave period) of the falling transient, \( t = T_{\text{minus}} \), corresponds to the capacitor voltage, decreasing to

Equation 12.20

\[ v_{C_{\text{o}}}(T_{\text{minus}}) = -\frac{R_3}{R_3 + R_1} v_{O_{m}} \]
Using (12.20) in (12.19) gives the equation for $T_{\text{minus}}$, which is

Equation 12.21

$$\frac{-R_3}{R_3 + R_1} V_{\text{om}} = \left( V_{\text{om}} + \frac{R_3}{R_3 + R_1} V_{\text{op}} \right) \frac{-T_{\text{minus}}}{R_f C_0} - V_{\text{om}}$$

This leads to

Equation 12.22

$$T_{\text{minus}} = R_f C_0 \ln \left( \frac{V_{\text{om}} + \frac{R_3}{R_3 + R_1} V_{\text{op}}}{\frac{R_1}{R_3 + R_1} V_{\text{om}}} \right)$$

A special case is for $R_1 = R_3$, where (12.18) and (12.22) become

Equation 12.23

$$T_{\text{plus}} = R_f C_0 \ln \left( \frac{2V_{\text{op}} + V_{\text{om}}}{V_{\text{op}}} \right)$$

and

Equation 12.24

$$T_{\text{minus}} = R_f C_0 \ln \left( \frac{2V_{\text{om}} + V_{\text{op}}}{V_{\text{om}}} \right)$$

The oscillator period is $T = T_{\text{plus}} + T_{\text{minus}}$ or, for this special case,

Equation 12.25
A good estimate comes from the approximation $V_{op} \approx V_{om}$. The result is

Equation 12.26

$$T = R_f C_o \left[ \ln \left( \frac{2V_{op} + V_{om}}{V_{op}} \right) + \ln \left( \frac{2V_{om} + V_{op}}{V_{om}} \right) \right]$$

Note that although $T_{\text{minus}}$ and $T_{\text{plus}}$ can be significantly different [from (12.18) and (12.22)], the sum is well represented by (12.26). Note also that the waveform is strictly a square-wave only if $V_{op} = V_{om}$.

LabVIEW uses (12.25) to calculate the actual value of the capacitor used in the project on the oscillator. In the project, period $T$ is a measured value. Shown in Fig. 12.3 is a project result of the measurement of the output voltage and capacitor voltage for the oscillator. Power-supply voltages were set at plus and minus eight volts and $R_1 = R_3$.

**Figure 12.3. Oscillator $v_o(t)$ and $v_{co}(t)$ versus $t$ (ms). Note that the switching takes place where the capacitor voltage reaches about one-half of the square-wave peak magnitude. This is for $R_1 = R_3$.**

### 12.3. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2V_{\text{peak}} = \frac{V_s}{R_f C_f} \frac{T}{2}$</td>
<td>Opamp-integrator equation for determining triangular-wave peak amplitude for applied square-wave with peak $V_s$ and period $T$.</td>
</tr>
<tr>
<td>$v_o(t) = V_s \sin \left( \frac{2\pi t}{T} \right) + \frac{T}{2\pi R_f C_f} V_s \cos \left( \frac{2\pi t}{T} \right)$</td>
<td>Opamp-integrator equation for determining output waveform for sine-wave input with peak $V_s$ and period $T$.</td>
</tr>
</tbody>
</table>
\[ 2V_{\text{peak}} = \frac{V_s}{R_f C_f} \cdot \frac{T}{2} \quad \text{Opamp-integrator equation for determining triangular-wave peak amplitude for applied square-wave with peak } V_s \text{ and period } T. \]

\[ T = R_f C_o \left[ \ln \left( \frac{2V_{o, p} + V_{o, m}}{V_{o, p}} \right) + \ln \left( \frac{2V_{o, m} + V_{o, p}}{V_{o, m}} \right) \right] \quad \text{Equation for the opamp-oscillator period, for the case of } R_1 = R_3. \]

\[ T = \Delta R_f C_o \ln(3) \approx 2.6 \Delta R_f C_o \quad \text{Equation for opamp-oscillator period, for the case of } R_1 = R_3 \text{ and equal positive and negative peak magnitudes.} \]

### 12.4. Exercises and Projects

- **Project Mathcad Files**
  - Exercise12.mcd - Project12.mcd

- **Laboratory Project 12**
  - Operational Amplifier Integrator and Oscillator
  - Opamp Integrator
  - Opamp Oscillator

### Unit 13. Cascaded Amplifier Stages

The cascade electronic circuit configuration is that formed by connecting the output of one stage to the input of the one following. In analog amplifiers, such as the operational amplifier, high gain is achieved through cascading a number of stages. Mixing NMOS and PMOS circuits provides the major advantage of direct coupling between stages. The amplifier investigated is the cascade of a differential stage and a common-source stage. Circuit bias stability is explored as an example of problems in general with direct stage coupling.

### 13.1. Combining NMOS and PMOS Circuits in Cascade

The circuit of Fig. 13.1 illustrates the concept of combining NMOS circuits with PMOS circuits for enabling direct coupling of the stages. The added feature of a dual power supply is included, which provides for having the input and outputs at ground potential. One of the important advantages of this is that connecting input sources and output loads does not affect the bias.

*Figure 13.1. Cascade of a differential stage and a common-source stage. No coupling capacitors or bypass capacitors are required. This is therefore a dc amplifier.*
The input can be set equal to zero volts, as it is the gate of a differential amplifier stage in a dual-power-supply configuration. The output can be set equal to zero volts by selecting the drop across the bias resistor $R_{D3}$ to be equal to $|V_{SS}|$. This flexibility is provided by the PMOS as the output stage; it is approximately a current course with termination at the negative power supply. With $V_O = 0$, the available output signal range is nearly equal to the magnitude of the power-supply voltage; the drain voltage of $M_3$ can swing anywhere from near $V_{DD}$ down to $V_{SS}$. Note that this would not be possible if the common-source stage transistor were based on an NMOS.

The output from $M_2$ of the differential-amplifier stage is used arbitrarily. Since the common-source stage is an inverting stage, the gates of $M_1$ and $M_2$ are the inverting ($-$) and noninverting ($+$) inputs, respectively. A dc stabilization resistor would be connected between the output (drain of $M_3$) and the input at the gate of $M_1$. This type of feedback would, of course, represent an additional load on the output stage.

### 13.2. Amplifier Gain of Differential Amplifier and Common-Source Stage in Cascade

In the example of Fig. 13.1, a differential stage and a common-source stage are connected in a cascade configuration; the input of the common-source stage is the output of the differential stage. The overall voltage gain is defined as $a_v = \frac{V_o}{V_i} = \frac{V_{d3}}{V_{g1}}$. But this is also

Equation 13.1

$$a_v = \frac{V_{d3}}{V_{g1}} \cdot \frac{V_{d3}}{V_{g3}} = a_{v_d} a_{v_{cs}}$$
Therefore, the gain can be calculated by using the separate expressions considered previously for the differential amplifier stage \[(8.15)\] and the common-source stage \[(5.5)\]. This leads to

Equation 13.2

\[ a_v = \left( \frac{1}{2} g_m R_{D2} \right) \left( -g_m R_{D3} \frac{1 + \lambda p I_{D3} R_{D3}}{1 + \lambda p I_{D3} R_{D3}} \right) \]

or using, from \((4.5)\), \( g_m = 2I_D/V_{eff} \),

Equation 13.3

\[ a_v = -\frac{I_{D3} R_{D2}}{V_{eff1}} \frac{2I_{D3} R_{D3}}{V_{eff2}} \frac{1}{1 + \lambda p I_{D3} R_{D3}} \]

\[ a_v = -\frac{1}{V_{eff1}} \frac{2V_{p3}}{V_{p2}} \frac{1}{1 + \lambda p R_{p2}} \]

Throughout this unit, the assumption is made that \( g_{m1} = g_{m2} \) and \( V_{effn1} = V_{effn2} \).

The gain expression neglects the transistor output resistance in the differential amplifier gain for simplicity without a great loss of accuracy, due to the relatively small value of \( R_{D2} \). It also neglects the effect on the gain of the differential stage of \( R_{bias} \). [\( R_{bias} \) and the output resistance are included in gain result \((8.40)\), for comparison.] For a calculation of a numerical value of a representative gain, assume that \( V_{effn1} = V_{effp3} = 0.3 \) V, \( V_{tno} = V_{tpo} = 1.0 \) V (giving \( V_{RD2} = 1.3 \) V), \( V_{RD3} = 5 \) V (for \( V_{ss} = -5 \) V) and \( \lambda p = 0.05 \) V\(^{-1} \). The voltage-gain magnitude is \( |a_v| = 4.33 \cdot 26.7 = 116 \). We compare this below with an amplifier that has better bias stability but which loses gain in a trade-off.

**13.3. Stabilization of Signal Gain and Bias Current with a Source Resistor**

The amplifier of Fig. 13.1 is not a good design in terms of bias stability. Bias current \( I_{D3} \) (of M3) in the circuit of Fig. 13.1 is very sensitive to the voltage across \( R_{D2} \), which, in a relative sense, is only marginally predictable, given the normal variation in device parameters and circuit components. Also, as in the bias-stability discussion of Unit 5.5 on the design of the NMOS common-source amplifier, for a constant \( V_{GS3} \), bias current \( I_{D3} \) is sensitive to changes in transistor parameters. (Note that the differential-amplifier-stage bias current is relatively stable, as it is a current-source bias current.)
13.3.1. Gain and Gain Stabilization

As noted, it was shown in Unit 5.5 that a degree of bias stability is provided with a source resistor as in the circuit of Fig. 13.2 (in this case, R_{S3}). This is an additional example of providing some stabilization with the addition of ac and dc negative feedback in a circuit. The addition of the resistor results in an increase in the gain of the differential amplifier stage but a decrease in the gain of the common-source stage. The net result is a reduction of gain as a trade-off between the gain and bias stability.

Figure 13.2. Amplifier circuit with the addition of a source resistor, R_{S3}, which serves to improve the gain and bias stability. This again demonstrates a general principle, often used in electronic circuits, wherein a linear component is installed to dominate the voltage of voltages in series.

The gain expression for the circuit with R_{S3} is

Equation 13.4

\[ a_v = -\frac{1}{2} g_m R_{D2} \frac{g_{m3} R_{D3}}{1 + g_{m3} R_{S3}} \]

where (5.15) is now used for the gain of the common-source stage. It is useful again to express the result in terms of V_{effn} and V_{effp} and the voltages across resistors to make a quantitative assessment of the gain. Using \( g_m = 2I_D/V_{eff} \) [(4.5)], the gain expression is

Equation 13.5
For example, we set $V_{RS3} = 1$ V, with a new $V_{RD2} = 2.3$ V. The gain magnitude is now $|a_v| = 7.67 \cdot 4.35 = 33.3$, compared with 116 for the circuit of Fig. 13.1. Note that the contribution from the differential stage increases from 4.3 to 7.7.

The output-resistance effect on the gain of the common-source stage is neglected [as in (5.15)]. This is justified as the output resistance at the drain of $M_3$ is increased significantly with $R_{S3}$. [Precision gain equation (8.34) gives 4.21 compared with 4.35 using (5.15)]. This is discussed further below in conjunction with the common-source amplifier with source resistor from the viewpoint of a feedback circuit.

If resistor $V_{RS3}$ is sufficiently large, $g_{m3}R_{S3} >> 1$. In this limit the gain is

$$a_v \approx - \frac{V_{R_{D2}}}{V_{eff1}} \frac{R_{D3}}{R_{S3}} = - \sqrt{k_{p3}I_{D2}R_{D2}} \frac{R_{D3}}{R_{S3}}$$

The magnitude of gain given by (13.6) is about 38, a fair approximation to the value of 33 from (13.5). It is apparent from the form of (13.6) that a significant degree of gain stabilization has been achieved, as the gain depends primarily only on the bias currents $I_{D1} = I_{D2}$, which is quite stable in the differential amplifier circuit.

### 13.3.2. Transistor Parameter Variation and $I_{D3}$ Bias Stability

The benefit to $I_{D3}$ bias stability associated with transistor parameter variation can be assessed by a consideration of (5.18) applied to this case, which is

$$I_{D3} = \frac{I_{D2}R_{D2} - \frac{I_{D2}}{\sqrt{k_{p3}}} - V_{tpo3}}{R_{S3}}$$

For a quantitative example, suppose that $I_{D3} = 100$ μA. To be consistent with the numbers used in Unit 13.2, $k_{p3} = 1110$ μA/V$^2$ with $V_{eff3} = 0.3$ V.
Assume that \( V_{RD2} = I_{D2}R_{D2} \) is constant. Now make \( k_{p3} \) 5% larger and \( V_{tpo3} \) 50 mV smaller. For the \( V_{RD2} = 2.3 \) V, we have a new \( I_{D3} = 105 \) \( \mu A \) for \( V_{D3} = 0.25 \) V, which is an acceptable bias value. For the circuit of Fig. 13.1, and the same parameter changes, the new bias current is \( I_{D3} = 143 \) \( \mu A \) for \( V_{D3} = 2.15 \) V, significantly away from the design zero volts.

### 13.3.3. Bias Stability of \( I_{D3} \) Due to Changes in \( I_{D2} \)

The actual differential-stage bias current will vary from the basic design due to the variation in circuit components, transistor parameters, and power-supply voltage. Suppose that in lieu of the value of \( V_{RD2} = 2.3 \) V as in the example above, \( V_{RD2} \) is 5% higher or 2.42 V. Assume that the transistor parameters of the common-source stage are at the original design values.

An estimate of the new output voltage (different from 0V) can be made using the linear relation between the input and output of the common-source stage, that is, the common-source contribution of (13.4). The "signal" is the change of voltage across \( R_{D2} \), which is –0.12 V. (The gate voltage \( v_{G3} \) decreases.) The common-source gain from (13.4) for the original parameters associated with \( M_3 \) is –4.35. The output bias voltage is now (–4.35)(–0.12V) = 0.5 V (instead of 0 V). Therefore, the circuit is reasonably bias stable.

The gain of the unstabilized circuit of Fig. 13.1 is –27, which leads to an output voltage, for the same change of voltage across \( R_{D2} \), of 3.2 V, using the linear approximation. Note that the linear approximation is marginally valid only for such a large value of the common-source input "signal" voltage, as in this case of no source resistor. (A dc calculation gives a bias output voltage of 4.8 V.)

### 13.4. Common-Source Stage as a Series – Series Feedback Circuit

The circuit of Fig. 13.2 with the source resistor is technically a feedback circuit. It falls into the category of series – series feedback, or the feedback network samples the output current and feeds back a voltage in series (and the same polarity, negative feedback) with the input to the common-source stage, that is, \( V_{gs3} \). The series – series feedback amplifier is referred to as a transconductance amplifier. The noninverting and inverting opamp configurations are series – shunt (voltage amplifier) and shunt – shunt (transresistance amplifier), respectively. An additional alternative is shunt – series (current amplifier). An example of this type of feedback amplifier is discussed in Unit 13.5.

In Unit 9.9, an expression for the output resistance of the current source (drain current) with source degeneration was obtained [(9.9)]. This is

\[
R_o = (1 + g_mR_S) \frac{1}{g_{ds}} + R_S
\]
The perspective of the common-source amplifier in a series – series feedback mode is shown in Fig. 13.3. The circuit configuration is for determining the output resistance. A voltage $V_o$ is applied at the output terminals with the input grounded. In this series – series circuit, a feedback voltage, $V_f$, which is proportional to the current $I_o$, is induced as indicated in the circuit diagram. With the input grounded, voltage $V_f$ is applied to the input terminals of the transistor. The loop equation at the output is then

Equation 13.7

$$V_o = (I_o + g_m V_f) r_{ds} + V_f$$

Figure 13.3. Linear circuit for deriving the output resistance for the series – series feedback circuit. The feedback voltage is proportional to the output current.

By comparison of the feedback circuit of Fig. 13.3 with the circuit of Fig. 13.2, $V_f = I_o R_S$. Thus,

Equation 13.8

$$V_o = \left[1 + g_m R_S\right] r_{ds} + R_S \approx (1 + g_m R_S) r_{ds} I_o$$

This produces (9.9) from $R_o = V_o/I_o$ and with $r_{ds} = 1/g_{ds}$. Intuitively, the feedback is such as to cause a much larger current through $r_{ds}$ than $I_o$, and therefore a much larger $V_o$ is required for a given $I_o$.

Dropping the $R_S$ as in the right-hand side of (13.8) renders the result equivalent to the ideal series – series feedback amplifier, as shown in Fig. 13.4. In the ideal series – series amplifier, the sense function has zero resistance; that is, the output voltage is directly
across $r_{ds}$. With $g_{m}/g_{ds} >> 1$, the ideal circuit provides a very good approximation to the actual circuit. For example, with $V_{\text{effn}} = 0.5$ V and $\lambda_n = 1/50$ V, the ratio is 100.

**Figure 13.4. An ideal series – series feedback amplifier. $V_o$ is applied directly across the output resistance and $V_f$ is applied to the grounded input.**

For both feedback amplifier types with series as the second term (series – series and shunt – series), the output resistance is increased by a factor $(1 + T)$, where $T$ is the loop gain, as in the discussion of the opamp feedback amplifiers in Unit 11. The loop gain for the common-source circuit of **Fig. 13.2** is, by definition, $T = V_f/V_{gs3}$. By inspection of (9.9) we conclude that $T = g_{m3}R_{S3}$. In terms of $T$, the output resistance is then

Equation 13.9

$$R_O = (1 + T)r_{ds3} + R_{S3}$$

**13.5. Shunt – Series Cascade Amplifier**

The cascading of two common-source amplifier stages will now be explored. This will expand the discussion on feedback amplifiers to include the shunt – series (current) amplifier. As shown in **Fig. 13.5**, the current $I_o$ is sensed, with the feedback network consisting of $R_{S2}$ and $R_f$, and a fraction of $I_o$ is summed at the gate input node along with the input source current. Gate resistor $R_{G1}$ provides for an addition bias design variable but otherwise is simply combined with the source resistance, $R_s$, in the amplifier performance analysis or design.

**Figure 13.5. Shunt-series feedback amplifier. This is a current amplifier with feedback amplifier gain, $A_i = I_o/I_i$.**
13.5.1. DC Design

For the design, assume that a choice has been made for $I_{D1}$ and $I_{D2}$ and $V_{G2} = V_{D1}$. The latter must be such that $V_{G2} > V_{GS1} + V_{GS2}$. Then, for $R_{D1}$, use

Equation 13.10

$$R_{D1} = \frac{V_{DD} - V_G}{I_{D1}}$$

As will be indicated below, the ideal current gain is

Equation 13.11

$$A_{II} = 1 + \frac{R_f}{R_{S2}}$$

Use this, based on the feedback-amplifier design current gain goal, to obtain a relation between $R_f$ and $R_{S2}$. This gives

Equation 13.12

$$R_f = (A_{II} - 1)R_{\infty}$$
Now determine the value of \( R_S2 \) which satisfies the design value of \( I_{D2} \). This is obtained from

Equation 13.13

\[
I_{D2} = \frac{V_{S2}}{R_{S2}} + \frac{V_{S2} - V_{GS1}}{(A_{II} - 1)R_{S2}}
\]

where 13.12 has been used for \( R_f \) and where \( V_{S2} = V_{G1} - V_{GS2} \) and

Equation 13.14

\[
V_{GS1} = \sqrt{\frac{I_{DF}}{K_{P1}}} + V_{tn0}
\]

and

Equation 13.15

\[
V_{GS2} = \sqrt{\frac{I_{DF}}{K_{P2}}} + V_{tn0}
\]

Finally, select \( R_{G1} \) to satisfy the \( V_{GS1} \) requirement from

Equation 13.16

\[
V_{GS1} = \frac{R_{G1}}{R_{G1} + R_f} V_{S2}
\]

13.5.2. DC Stability

The feedback network provides significant bias stabilization and the effect can be assessed by the same formulation as for the opamp. In Unit 11.4, it was shown that the output voltage for a given offset voltage is \([11.16]\)
As applied to our shunt-series circuit (by equivalency), $A_{VN1} = 1 + \frac{R_f}{R_{G1}}$, and $a_{vo}$ is the voltage-gain magnitude (minus terminal equivalent) from the gate, $V_{g1}$, to the source $V_{s2}$, that is, the gain of the case of a common-source stage ($M_1$) and a source-follower stage ($M_2$). Also, for this case, $\Delta V_o \equiv \Delta V_{S2}$. Note that for this case, $\Delta V_o$ is a bias-voltage change, whereas for the opamp, it is the output voltage (different from zero volts).

Suppose that the dc (bias) is at a set state. Then the bias is altered such as by a change of a transistor parameter (either by temperature change or substituting one transistor for a new one). For example, a change in $V_{tno}$ of $M_1$ is equivalent to installing an offset voltage, and [(11.16)] can be applied directly to this case. Make $R_{G1} = R_f$ for $A_{VN1} = 2$. Also assume a typical $a_{vo} = 40$ (common-source stage). For a change of $\delta V_{tno} \equiv V_{off} = -0.1$ V, $\Delta V_o \approx 2 \cdot 0.1$ V = 0.2 V. Note that based on $a_{vo} = 40$, with no feedback stabilization, the change in output would be approximately $a_{vo} \delta V_{tno} = 4$ V.

### 13.5.3. Signal Current Gain

We first compute the open-loop transconductance and then the open-loop current gain. This is done, for a good approximation, by disconnecting the right side of $R_f$ from the source of $M_2$ and connecting it to ground. (This disables the shunt-series feedback and otherwise alters the circuit only slightly.) The result is

Equation 13.17

$$a_i = R_f G_m$$

where $R_i = R_s||R_{G1}||R_f$. (This assumes that $R_f >> R_{S2}$ which is consistent with $A_{ii} >> 1$.) Transconductance $G_m$ is for the complete cascade circuit (open loop), that is,

Equation 13.18

$$G_m = \frac{I_o}{V_i} = \frac{1}{g_{m2}}$$

where $g_{m2} = g_{m1}R_{G1}$ and $g_{m2}R_{S2}$.
Note that the series – series feedback effect is retained in the open-loop computation and that $R_{S2}$ has been used as an approximation for $R_{S2}|R_f$. This once again assumes that $R_f \gg R_{S2}$. The loop gain is

$$T = \frac{a_i R_{S2}}{R_{S2} + R_f}$$

Following the discussion in Unit 11, which led to (11.3), the current gain with feedback is then

$$A_i = \frac{a_i}{1 + T} = \frac{A_{ii}}{1 + \frac{1}{T}}$$

where (ideal current gain of the feedback amplifier)

$$A_{ii} = 1 + \frac{R_f}{R_{S2}}$$

As a design example, suppose the design goal is $A_{II} = 10$. Assume that the transistors have $V_{tno} = 1 \text{ V}$, $k_{n1} = 1000 \mu\text{A}/\text{V}^2$, and $k_{n2} = 2000 \mu\text{A}/\text{V}^2$. We select $I_{D1} = 100 \mu\text{A}$, $I_{D2} = 200 \mu\text{A}$, $V_{DD} = 10 \text{ V}$, and $V_{G2} = 3.5 \text{ V}$. From (13.12) and (13.13) we obtain $R_{S2} = 11.4 \text{ k}\Omega$ and $R_f = 103 \text{ k}\Omega$. Based on (13.16), the value of $R_{G1}$ is $R_{G1} = 156 \text{ k}\Omega$. To satisfy the drain voltage requirements, $R_{D1} = 65 \text{ k}\Omega$ and $R_{D2} = 25 \text{ k}\Omega$. The latter is based on $V_{D2} = \frac{V_{DD}}{2}$. Also, we assume that $R_s = 100 \text{ k}\Omega$.

The open-loop transconductance is $G_m = 3372 \mu\text{A}/\text{V}$ and $R_i = 38 \text{ k}\Omega$ for $a_i = 129$. Loop gain $T = 12.9$ such that $A_i = 9.28$. We note that since $A_i \approx A_{II} = 10$, the current gain is very predictable, despite bias and parameter variations.
13.6. Summary of Equations

\[ a_v = \left( \frac{1}{2} g_m R_{D2} \right) \left( -g_m \frac{R_{D3}}{1 + \lambda p I_{D3} R_{D3}} \right) \]

Gain of cascade of differential stage and common-source stage, including output resistance of M3.

\[ a_v = -\frac{1}{2} g_m R_{D2} \frac{g_m R_{D3}}{1 + g_m R_{S3}} \]

Gain of cascade circuit for case of common-source stage with source resistor.

\[ a_v \approx -\sqrt{k_p I_{D2} R_{D2}} \frac{R_{D3}}{R_{S3}} \]

Approximate form for gain which assumes that \( g_m R_{S3} >> 1 \).

\[ a_v \approx -\frac{V_{R3R2}}{V_{eff2}} \frac{R_{D3}}{R_{S3}} \]

Bias equation for transistor M3.

\[ I_{D2} = R_{D2} - \frac{I_{D3}}{1 + k_p \frac{V_{D2} - V_{fp}}{R_{S3}}} \]

Shunt – series amplifier dc design equations.

\[ R_{D1} = \frac{V_{D2} - V_{GS}}{I_{D1}} \]

\[ R_{G2} = \frac{V_{GS} - V_{GS}}{R_{G2} + R_f} \]

Shunt – series amplifier dc stability relation.

\[ I_{D2} = \frac{V_{S2} - V_{GS}}{R_{S2}} + \left( \frac{A_{II}}{1 + A_{II}} \right) \frac{V_{S2} - V_{GS}}{R_{S2}} \]

Shunt – series amplifier open-loop current gain relations.

\[ T \approx a_v \frac{R_{S2}}{R_{S3} + R_f} \]

Feedback amplifier current-gain relations.

\[ A_{II} = \frac{a_v}{1 + T} = \frac{A_{II}}{1 + T} \]

\[ A_{II} = 1 + \frac{R_f}{R_{S2}} \]
Unit 14. Development of a Basic CMOS Operational Amplifier

In this unit, we start with the basic components of amplifiers that have been discussed and progress, stepwise, toward an actual integrated-circuit operational amplifier. The final amplifier consists of two gain stages and a buffer stage. The gain stages are the equivalent of the cascade of a differential stage and a common-source stage of Unit 13, except with improvements consisting of current-source bias in place of bias resistors.

14.1. Current-Source Bias for the Differential Amplifier Stage

The drain-current bias resistor, $R_{bias}$, of the basic differential amplifier stage as introduced in Fig. 8.1 will now be replaced by a current source as shown in the circuit of Fig. 14.1. The bias resistor is replaced by two transistors, $M_{10}$ and $M_{11}$, and one resistor, $R_1$. This seems like an unfavorable exchange but it is not. This is because the reference voltage $V_{GS10}$ formed by the reference circuit of $R_1$ and $M_{10}$ can be used for additional current sources in the complete circuit, thereby eliminating the need for a number of other bias resistors.

Figure 14.1. Differential amplifier stage with bias resistor, $R_{bias}$ (Fig. 13.1), replaced with a current source. Bias circuit consists of $R_1$, $M_{10}$, and $M_{11}$.

![Differential amplifier stage with bias resistor](image)

Resistors in an integrated circuit cost much more in chip space than do transistors. Also, the output resistance of a current-source transistor, $M_{11}$, will be much higher than the resistor equivalent, leading to improved amplifier characteristics, as discussed below.

Following the discussion of transistor current sources in Unit 9, the ratio of the reference current and the current-source current is
The ratio of the gate widths will thus be selected to satisfy the design of the differential-stage bias. The current ratio will deviate from the simple ratio due to the $\lambda_n$ terms, but this is not critical, as the design will not call for an exact value for $I_{D1} \approx I_{D2}$.

### 14.2. Current-Source Output Resistance and Common-Mode Gain

As discussed in [Unit 8](#), the common-mode gain is the gain for the same signal being applied to both inputs. In [Unit 8.6](#) the common-mode voltage gain expression, (8.26), was obtained for the bias resistor, $R_{bias}$. This is

$$
a_{vcm} = \frac{-g_m R_{D2}}{1 + 2g_m R_{bias}}
$$

To apply the common-mode gain equation to the circuit of [Fig. 14.1](#), resistor $R_{bias}$ is replaced by $r_{ds11}$. The result for the common-mode gain is

Equation 14.2

$$
a_{vcm} = - \frac{g_m R_{D2}}{1 + g_m \cdot 2r_{ds11}} \approx - \frac{R_{D2}}{2r_{ds11}}
$$

The approximate form is consistent with neglecting the change of the gate – source voltage compared to the change of voltage at the drain of the current-source transistor, $M_{11}$. Intuitively, (14.2) indicates that for $r_{ds11} \longrightarrow \infty$, transistor $M_{11}$, is a pure current source, and $I_{D1} = I_{D2} = I_{D1} = I_{D2}$ regardless of the magnitude of common voltage applied to both gates. In this case, signals $I_{d1} = I_{d2} = 0$ for any (realistic) common-mode input signal.

Common-mode inputs can be a form of noise, and therefore the ideal opamp would reject these signals entirely. An important consideration is the extent of rejection based on the common-mode gain relative to the differential amplifier gain. This is quantitatively assessed with the common-mode rejection ratio, which is the ratio of the differential amplifier gain with differential output divided by the common-mode gain, (14.2). The gain for this case was obtained in [Unit 8.5](#) as (8.24), which is $a_{vdl2} = -g_m R_D$. 

---

**Equation 14.1**

$$
\frac{I_{D11}}{I_{D10}} = \frac{w_{11}}{w_{10}} \frac{1 + \lambda_n V_{DS11}}{1 + \lambda_n V_{DS10}} \approx \frac{w_{11}}{w_{10}}
$$

---
Using (8.24) and (14.2), the common-mode rejection ratio is

Equation 14.3

$$\text{CMRR} = \frac{3\, v_{\text{di1}}}{a_{\text{vcm}}} = 1 + g_{m1}^2 r_{\text{ds11}} \approx 2g_{m1} r_{\text{ds11}}$$

With $g_{m1} = 2I_{D1}/V_{\text{eff1}}$ [(4.5)], and for the output resistance of $M_{11}$, $r_{\text{ds11}} \approx 1/\lambda_n 2I_{D1}$ [(4.15)], the common-mode rejection ratio is

Equation 14.4

$$\text{CMRR} = \frac{4}{V_{\text{eff1}} \lambda_n}$$

By comparison, for resistor bias, the equivalent result is

Equation 14.5

$$\text{CMRR} = \frac{4V_{R_{bias}}}{V_{\text{eff1}}}$$

where $R_{bias}$ is the bias resistor of, for example, the circuits of Figs. 13.1 and 13.2.

14.3. Current-Source Load for the Common-Source Stage

We now add to the differential stage the common-source stage to obtain a two-stage amplifier as in Unit 13 (Fig. 14.2). Transistor $M_{12}$, which replaces bias resistor $R_{D3}$, provides a current-source load as in the circuit of Fig. 10.1. Note that current $I_{D12}$ mirrors $I_{D10}$ and no additional resistors are required with the addition of the common-source stage. That is, $M_{11}$ and $M_{12}$ both use the reference voltage provided by the diode-connected $M_{10}$.

*Figure 14.2. Cascade of the differential amplifier stage and common-source stage. $M_{12}$ provides a current-source load for the common-source stage. This circuit remains inadequate in terms of dc bias stability of $I_{D3}$. This is improved in the modification that follows.*
The bias design for the common-source stage consists of picking \( W_{12} \) to obtain a specified \( I_{D_{12}} \) relative to \( I_{D_{10}} \) and making \( I_{D_3} = I_{D_{12}} \). Parameter \( W_{12} \) is determined from Equation 14.6

\[
\frac{I_{D_{12}}}{I_{D_{10}}} = \frac{W_{12}}{W_{10}} \frac{1 + \lambda_n V_{DS_{12}}}{1 + \lambda_n V_{DS_{10}}} = \frac{W_{12}}{W_{10}}
\]

The approximation is sufficient, as the current magnitude, again, is not critical.

The circuit is adjusted to make \( I_{D_3} = I_{D_{12}} \) by equating the relations for the two currents. This is

Equation 14.7

\[
k_{p3} V_{\text{eff}_3}^2 (1 + \lambda_p V_{DD}) = k_{n12} V_{\text{eff}_{12}}^2 (1 + \lambda_n |V_{SS}|)
\]

A much simpler equation replaces this rather complicated one when \( R_{D2} \) is finally replaced by a transistor as well. \( V_{\text{eff}_{12}} \) is known from \( V_{\text{eff}_{12}} = V_{\text{eff}_{10}} \). Thus, the current balance can be obtained by a selection of the various remaining parameters.

The load on the common-source stage is now \( r_{ds_{12}} = 1/g_{ds_{12}} \). The gain is, including the output resistance of \( M_3 \).

Equation 14.8
The overall amplifier gain, \( a_v = \frac{V_o}{V_i} \), is now

Equation 14.9

\[
a_v = -\frac{1}{2} g_m R_D \frac{g_m}{g_{ds3} + g_{ds12}}
\]

This can be evaluated with

Equation 14.10

\[
a_v = \frac{I_D R_D}{V_{eff1}} \frac{2}{V_{eff3} \left( \lambda_n + \lambda_p \right)}
\]

Using the numbers from the previous calculation for the amplifier of Fig. 13.1 with \( R_{D3} \), and adding \( \lambda_n = \lambda_p \), the gain magnitude for the circuit of Fig. 14.2 is 289. This compares with the value of 116 for the cascade amplifier of Fig. 13.1. In the next unit, the differential stage will be modified to include a current source load with a considerable additional improvement in gain.

### 14.4. Current-Source Load for the Differential Stage

The load resistor (or bias resistor) of the differential stage will now be replaced with a current-source load. In addition to eliminating the need again for a resistor, it provides for much better dc stability and a significant gain improvement, including the elimination of the factor of \( \frac{1}{2} \) associated with the differential stage gain as in (8.15) and (8.17).

As shown in the new circuit in Fig. 14.3, the resistor \( R_{D2} \) is replaced by transistors M4 and M5. Transistor M5 provides a current-source load for transistor M2. The diode-connected transistor, M4, provides the dc reference voltage for M5. The reference current is \( I_{D1} = I_{D4} \).

**Figure 14.3. Differential amplifier stage with current-source load.**
The dc output voltage (of the differential stage) is set automatically at $V_{DD} - V_{SG4}$ due to the relation $V_{SD4} = V_{SG4} = V_{SG5} = V_{SD5}$. This is an idealization that assumes that the parameters of transistors M4 and M5 and M1 and M2 are identical and that $I_{D1} = I_{D2}$.

Recall that in the differential stage with drain resistor, $R_{D2}$, the noninverting output signal voltage was induced across $R_{D2}$ due to the signal current $I_{d2}$. In the new circuit, the output current is the composite of signal currents $I_{d2}$ and $I_{d5}$. That is, signal current $I_{d1}$ is mirrored at the output as $I_{d5}$. This is a result of the coupling from M1 through M4 to the gate of M5. The circuit from the gate of M1 to the drain of M5 can be regarded as a cascade of two common-source stages (M1 and M5) with a shunt resistor between them of magnitude $1/gm4$ (the signal resistance of the diode-connected transistor).

The gain for this circuit can be explained starting from the transconductance for the two currents $I_{d2}$ and $I_{d5}$. Assume for a moment that the output voltage is held constant at the dc bias value. This is equivalent to a signal short circuit at the output. As in the case of the resistor-bias differential amplifier stage, we have

Equation 14.11

$$I_{d2} = -\frac{1}{2} g_{m1} V_{g1}$$

where the effect of the output resistance of $M_{11}$ is neglected. But also, as in the resistor-load case,

Equation 14.12
But \( I_{d1} = -I_{d4} \) and \( I_{d4} \) is mirrored as \( I_{d5} \), which leads to \( I_{d5} = -I_{d1} \). This assumes that \( M4 \) and \( M5 \) are identical. Thus,

**Equation 14.13**

\[
I_{d5} = -\frac{1}{2} g_m V_{g1}
\]

All signal drain currents are defined as positive into the respective drains.

The output currents summed at the output node, \( V_o \), are (defined positive into the node)

**Equation 14.14**

\[
I_o = I_{d2} + I_{d5} = -g_m V_{g1}
\]

The result is valid for \( v_o = V_o \) or \( V_o = 0 \), as stipulated above. One could imagine attaching a dc supply exactly equal to \( V_o \) at the output node. In this case, the output current could readily flow into the node according to (14.14).

For the opposite extreme of having an open circuit at the output, as in **Fig. 14.3**, the currents \( I_{d2} \) and \( I_{d5} \) are dependent on \( v_{D2} = v_{D5} = v_o \). The deviation of \( I_o \) from (14.14) is, as usual, taken care of by including the effect of the output resistance at the output node.

The output resistance is somewhat complicated by feedback effects, which are inherent in this circuit. For assessing the circuit output resistance, a signal circuit is shown in **Fig. 14.4** with a test voltage, \( V_o \), applied at the output with both inputs grounded. Resulting currents \( I_{d2} \) and \( I_{d5} \) will be considered separately and will be superimposed.

**Figure 14.4.** Signal (linear) circuit for determining the output resistance at the drains of \( M2 \) and \( M5 \). Currents shown are associated with the assessment of the output resistance associated with \( M2 \) only. The bias transistor (\( M_{11} \)) output resistance is neglected.
The currents indicated in Fig. 14.4 are for the case of $I_{d2}$ of $M_2$. Looking back into the drain of $M_2$, the output resistance is affected by emitter degeneration because of the resistance $1/g_{m1}$ between the emitter of $M_2$ and ground. That is, the resistance looking back into the emitter of $M_1$ is $1/g_{m1}$. Thus, the resistance looking only back into $M_2$ is $2r_{ds2}$. However, $I_{d2}$ feeds through and around the loop composed of $M_2$, $M_1$, $M_4$, and $M_5$ such that the total current flowing into the node (exclusive of the separate $I_{d5}$ contribution) is $2I_{d2}$. The test voltage is $V_o = I_{d2}2r_{ds2}$, due to current $I_{d2}$ flowing down into the resistance $2r_{ds2}$ of the drain of $M_2$. The output resistance associated with the drain of $M_2$, $R_{oM2}$, is based on a total current of $2I_{d2}$ such that it is

Equation 14.15

$$R_{oM2} = \frac{V_o}{2I_{d2}} = \frac{2I_{d2}r_{ds2}}{2I_{d2}} = r_{d2}$$

The drain resistance $2r_{ds2}$ combined with a test current of $2I_{d2}$ results in an effective drain resistance $r_{ds2}$ despite the emitter degeneration.

Separately, by superposition, for applied $V_o$, a current $I_{d5}$ of value $I_{d5} = V_o/r_{ds5}$ flows into the drain of $M_5$ such that the output resistance associated with $M_5$ is $R_{oM5} = r_{ds5} = 1/g_{ds5}$. This is based on the fact that the output resistance is that of a common-source stage with grounded source. The two contributions are in parallel such that finally, the output resistance is

Equation 14.16

$$R_{o25} = \frac{1}{g_{ds2} + g_{ds5}}$$
Combining this with the effective amplifier transconductance obtained above, (14.14), the gain is

Equation 14.17

\[ a_{v2} = \frac{g_m}{g_{ds2} + g_{ds5}} \]

or

Equation 14.18

\[ a_{v2} = \frac{2}{V_{eff1} \left( v_n + \lambda_p \right)} \]

An external load, \( R_L \), appears in parallel with \( R_o \). Hence with an external load, the gain is

Equation 14.19

\[ a_{v2} = \frac{g_m R_L}{g_{ds2} + g_{ds5} + \frac{1}{R_L}} = \frac{g_m R_L}{1 + (g_{ds2} + g_{ds5}) R_L} \]

In the discussion leading to (14.14), it was noted that the output current given by (14.14) is for a short-circuit condition at the output, and the effect of finite \( V_{d2} = V_{d5} \) is taken care of through the concept of the output resistance of the circuit. A clarification of this statement is provided by the analytical formulation, which includes a load, \( R_L \), given by

Equation 14.20

\[ \frac{\partial I_O}{\partial v_{g1}} = \frac{\partial I_{D2}}{\partial v_{D2}} v_{D2} + \frac{\partial I_{D5}}{\partial v_{D2}} v_{D2} + \frac{v_{D2}}{R_L} \]

where \( v_{D5} = v_{D2} \), as they are the same node. The linear form is

Equation 14.21
and this leads to \((14.19)\), where, again, \(a_{v2} = V_{d2}/V_{g1}\). A voltage source attached to the output is equivalent to \(R_L \rightarrow 0\), in which case \(V_{d2} \rightarrow 0\) and \(v_{D2} \rightarrow V_{D2} = V_O\), that is, the bias value. The finite output current magnitude into the short circuit is consistent with \(V_{d2}/R_{L,|vds, RL \rightarrow 0} = g_{m1} V_{g1}\).

### 14.4.1. Common-Mode Gain of the Differential Stage with Current-Source Load

As may be deduced from the common-mode gain equation, \((14.2)\), in Unit 14.2, the common-mode transconductance for the differential stage with current-source biasing is \(G_m = g_{m1}/(1 + g_{m1}2r_{DS11})\). The incremental load at the drain of M1 for the case of the circuit shown in Fig. 14.3, however, is the resistance of the diode-connected transistor M4 of Fig. 14.3, which is \(1/g_{m4}\). Due to symmetry, this is also the effective load at the drain of M2. The common-mode gain is thus

**Equation 14.22**

\[
\alpha_{vcm} = \frac{1}{1 + g_{m1}/g_{m4}}
\]

and the common-mode rejection ratio is, from \((4.17)\) (for single-ended output) and \((14.22)\),

**Equation 14.23**

\[
CMRR = \left(1 + \frac{g_{m1}}{g_{ds11}}\right) \cdot \frac{g_{ds2} + g_{ds5}}{g_{m4}} \approx \frac{2g_{m1}g_{m4}}{(g_{ds2} + g_{ds5})g_{ds11}}
\]

This is greater than \((14.3)\) by the factor \(g_{m4}/(g_{ds2} + g_{ds5}) \approx \left[V_{eff}\left(\lambda_n + \lambda_p\right)\right]^{-1}\).

### 14.5. Two-Stage Amplifier with Current-Source Biasing

The cascade amplifier that includes all features discussed up to this point is given in Fig. 14.5. Note that the only (internal) resistor is that of the reference-current circuit. Bias currents for this circuit can be set up using gate-width proportions. We note that \(I_{D3} \propto I_{D5}\) since \(M_3\) and \(M_5\) have a common bias voltage, \(V_{SG4}\). Thus
Equation 14.24

\[
\frac{I_{D3}}{I_{D5}} \approx \frac{W_3}{W_5}
\]

**Figure 14.5. Two-stage amplifier with current-source biasing.** $R_1$ is the only resistor in the internal circuit. $R_G$ is externally connected.

Also, $M_{11}$ and $M_{12}$ are referred to the same reference voltage such that

Equation 14.25

\[
\frac{I_{D12}}{I_{D11}} = \frac{W_{12}}{W_{11}}
\]

Using $I_{D3} = I_{D12}$ and $I_{D11} = 2I_{D5}$, we obtain

Equation 14.26

\[
\frac{I_{D3}}{I_{D5}} = 2 \frac{W_{12}}{W_{11}}
\]
Combining (14.24) and (14.26) leads to

Equation 14.27

\[ W_9 = 2\lambda_n\frac{W_{12}}{W_{11}} \]

Assume that \( W_{11} \) has been picked to satisfy the design \( I_{D11} \). \( W_{12} \) is then selected to give the design \( I_{D12} \) using \( I_{D12}/I_{D10} = W_{12}/W_{10} \). \( W_5 \) is selected on the basis of signal considerations. This leaves the computation of \( W_3 \) [from (14.27)].

A precision calculation includes the lambda effects and is from

Equation 14.28

\[ W_9 = 2W_{L} \frac{1 + \lambda_p V_{DS2}}{1 + \lambda_p V_{DS3}} \frac{W_{12}}{W_{11}} \left(1 + \lambda_n V_{DS2}\right) \]

The simple form should normally suffice. The dc output voltage \( V_O \) is very sensitive to some of the parameters and the approximate calculation from (14.27) will not result in \( V_O = 0 \). However, uncertainties in transistor parameters preclude the justification of using (14.28) in practice.

The overall signal gain is now obtainable using (14.17) for the differential stage and (14.8) for the common-source stage with a current-source load. The result is

Equation 14.29

\[ a_v = -\frac{g_{m1}}{g_{ds2} + g_{ds5}} \frac{g_{m3}}{g_{ds12} + g_{ds3}} \]

A useful form for making a quantitative gain assessment is

Equation 14.30

\[ a_v = -\frac{2}{V_{eff1} \left(\lambda_n + \lambda_p\right)} \frac{2}{V_{eff3} \left(\lambda_n + \lambda_p\right)} \]
Based on the same parameters as used previously for gain calculations ($\lambda_n = \lambda_p = 1/20 \text{ V}$ and $V_{\text{effn}} = V_{\text{effp}} = 0.3 \text{ V}$), the gain magnitude is 4440. The value compares with 116 for the all-resistor circuit for Fig. 13.1 and 289 for the circuit of Fig. 14.3. In this special case, both stages contribute the same value.

### 14.6. Output Buffer Stage

It is evident from the gain result, (14.29), that the high gain depends on having a high resistance at the output; a relatively small load resistor can reduce the gain substantially. For example, suppose that the amplifier is to be used as a resistance feedback amplifier as shown in Fig. 14.6. The input is at the gate of $M_2$, and the feedback resistor is connected back to the gate of $M_1$. The load at the output is $R_f + R_2 \parallel R_O$.

**Figure 14.6. Opamp with feedback resistor $R_f$. The feedback circuit adds load $R_f + R_2$ in parallel with external load, $R_O$, at the output.**

For a specific example, assume that $R_O >> R_f >> R_2$ such that the load is approximately $R_f$. With the additional load, the gain (14.30) becomes

Equation 14.31

$$a_v = -\frac{2}{V_{\text{eff1}}(\lambda_n + \lambda_p)} \frac{2}{V_{\text{eff3}}(\lambda_n + \lambda_p)} \frac{1}{1 + 1/I_{DS}R_f}$$

which is the result of $R_f$ being in parallel with the output resistance of the common-source stage. Suppose that $R_f = 10 \text{ k}\Omega$ and $I_{DS} = 100 \mu\text{A}$. In this case the gain would drop to about 400 (from about 4400), which would be unacceptable, as proper operation of opamps assumes a very high gain.

This loading problem is substantially eliminated with the addition of a buffer stage to isolate the load from the output node of the common-source stage, as shown in the circuit
of Fig. 14.7. The source-follower buffer stage is made up of M₆ and M₁₃. The current-source bias transistor M₁₃ also uses the reference voltage provided by M₁₀. The load on the common-source stage of M₃ is now infinite. The feedback network is included in the circuit for comparing with the diagrammatic version of the circuit of Fig. 14.6.

**Figure 14.7. Three-stage amplifier with the addition of the source-follower (buffer) stage.**

The gain expression of the source follower requires that the body effect be taken into consideration, as the body of M₆ will be at signal ground. [The body of M₆ will be attached to the negative supply voltage (not shown).] From Unit 7 it was shown that the source-follower stage gain, with resistor bias [(7.12)] for this case is

$$a_{vsf} = \frac{g_m}{g_m (1 + \eta) + \frac{1}{R_S} + g_{ds}}$$

For the present case of current-source bias for the source-follower stage, the gain expression becomes, with inclusion now of the feedback network and the external load resistance of Fig. 14.7,

Equation 14.32

$$a_{vsf} = \frac{g_m \theta}{g_m (1 + \eta) + g_{ds13} + g_{ds6} + \frac{1}{(R_f + R_e) R_o}}$$
To obtain a quantitative sense of the body effect on the gain of the source follower, suppose that $\eta = 0.15$. Thus, in the limit for $g_{m6} \to \infty$, $a_{vsf} = 0.87$. This is the best possible result, given the body effect.

For a more general assessment, we can substitute the relations $g_m = 2I_D/V_{eff}$, \([4.5]\), and $g_{ds} = I_D\lambda_n$ \([14.15]\) into \((14.32)\) to obtain

Equation 14.33

$$a_{vsf} = \frac{1}{(1 + \eta) + \frac{V_{eff}\lambda_n}{2} + \frac{V_{eff+1\lambda_n}}{2} + \frac{V_{eff6}}{[R_f + R_G] [R_O]}}$$

We note that the terms associated with $g_{ds6}$ and $g_{ds13}$ are negligible. Minimization of the resistance term requires making $g_{m6}[R_f + R_G] >> 1$ (making the output resistance of the source follower much less than the load resistance). This involves a combination of a large $I_{D6}$ and $k_{n6}$.

Suppose that $I_{D6} = 400 \mu A$, $W_6 = 500 \mu m$, $K_P = 100 \mu A/V^2$, and that the gate length is $L = 10 \mu m$. Recalling that $k_n = (K_P/2)(W/L)$ \((Table 3.1)\), we obtain $k_n = 2500 \mu A/V^2$ and $1/g_{m6} = 500 \Omega$. Thus, for example, for $R_O = 10 \Omega$, $R_f = 10 \Omega$, and $R_f >> R_G$, $a_{vsf} = 0.80$, compared with the limiting value of $a_{vsf} = 0.87$. Thus the source follower functions very well to isolate the load from the high-gain common-source stage.

Finally, we write the overall gain expression, including a general load resistance, $R_L$, by combining \((14.29)\) and \((14.32)\) as

Equation 14.34

$$a_v = \frac{g_{m1}}{g_{ds2} + g_{ds5} + g_{ds12} + g_{ds3}} \cdot \frac{g_{m3}}{g_{m6} (1 + \eta) + g_{ds13} + g_{ds6} + \frac{1}{R_L}}$$

A good approximation for the case of a sufficiently large $g_{m6}$ is

Equation 14.35

$$a_v = \frac{g_{m1}}{g_{ds2} + g_{ds5} + g_{ds12} + g_{ds3}} \cdot \frac{g_{m3}}{g_{ds7} + g_{ds17} + g_{ds7} \cdot 1 + \eta}$$
14.7. Output Resistance of the Feedback Amplifier and Effect on Gain from Loading

The output resistance of the resistance feedback amplifier was considered in Unit 11.4. There it was shown to be $R_o = r_o/(1 + T)$ ([11.12]), where $r_o$ is the output resistance of the open-loop amplifier and $T$ is the loop gain of the feedback amplifier. Therefore, with the expectation that $T \gg 1$, the output resistance of the feedback amplifier is very small. For example, consider the amplifier of Fig. 14.7, with no external load on the output and neglecting the effect of the feedback resistors. The open-loop output resistance is

$$r_o \approx \frac{1}{(1 + n)g_m b}$$

The output resistance of the feedback amplifier is

$$R_o = \frac{R_o}{1 + T} \approx \frac{1}{a_v R_G/R_f (1 + n)g_m b}$$

where the loop gain is $T = a_v R_G/(R_G + R_f)$.

Suppose that in order to get a high gain from the amplifier, we redesign the MOSFETs to have $\lambda_p = \lambda_n = 0.01 \text{ V}^{-1}$ for a new $a_v = 96,000$ [from (14.35), no loading]. Also, let $R_f = 10 \text{ k}\Omega$ and $R_G = 100 \text{ }\Omega$. Using the same numbers as in the calculation of a sample source-follower stage gain [(14.33)], $r_o = 435 \\Omega$ and $R_o = 0.45 \text{ }\Omega$.

The gain of the feedback amplifier is (11.3), which is

$$A_v = \frac{A_{\text{vNI}}}{1 + \frac{A_{\text{vNI}}}{a_v}}$$

with (11.4)
Here, gain $A_v$ is for the case of no external load (including the omission of the load from the feedback resistors). The value is $A_v = 100.9$ for $A_{vNI} = 101$.

Now we include an external load of $R_O = 100 \, \Omega$ and combine this in parallel with $R_f = 10 \, k\Omega$ for load $R_L = 99 \, \Omega$. The loading effect reduces the open-loop gain to $a_v = 18,000$. The reduction is all attributed to the loading on the source-follower stage. The amplifier gain [from (11.3)] is now $A_{vLoad} = 100.4$. However, with $R_o$ known, an alternative means of obtaining the gain with loading is to use

Equation 14.38

$$A_{vLoad} = A_v \frac{R_L}{R_L + R_o}$$

$A_v$ and $R_o$ are calculated once, using (14.35) and (14.37), respectively. Thus, the effect of loading can be obtained with one calculation using (14.38). As in the sample calculation above for the amplifier gain with loading included, $A_{vLoad} = 100.4$.

14.8. Output Circuit of the TS271 Opamp

The TS271 operational amplifier is designed to operate at very low current levels. This would include the current of the source follower of the output stage. In this case, the output resistance of an amplifier with a simple source-follower stage for an output stage, such as in Fig. 14.7, would be unacceptably high. In the TS271 operational amplifier, the 9-transistor circuit of Fig. 14.8 replaces the simple source-follower stage consisting of $M_6$ and $M_{13}$ of Fig. 14.7. Note that the circuit of Fig. 14.8 uses different transistor designators. In Fig. 14.7, $M_6$ and $M_{13}$ are equivalent to $M_1$ and $M_{n1}$ of Fig. 14.8.

*Figure 14.8. The output stage of the TS271 opamp. The new source follower consisting of $M_1$ and $M_{n1}$ is equivalent to the stage of $M_6$ and $M_{13}$ of the amplifier of Fig. 14.7.*
The circuit of Fig. 14.8 has an additional source-follower stage consisting of $M_2$ and $M_{n2}$. The output from the common-source stage (drain of $M_3$ of Fig. 14.7) is applied to the gates of both source-follower stages. The sources (outputs) of $M_1$ and $M_2$ are connected to the inputs of the differential-stage gates of $M_3$ and $M_4$, respectively. There is no load at the source of $M_1$ such that the gain of the source follower can be considered unity. Thus, $V_{g3} \approx V_{g2} = V_{g1}$ (incremental voltages). By contrast, the source of $M_2$ is connected to $R_L$ such that, in general, $V_o = V_{s2} < V_{g2}$.

From another perspective, suppose $V_{g2} = 1\text{V}$, that is the source-follower gates are raised by 1\text{V} above the bias level. With a load, $R_L$, the current increase will be greater for $M_2$ compared to $M_1$. This will cause the source voltage of $M_2$ to be slightly lower (than that of $M_1$) such that the input to the differential amplifier is nonzero and the output voltage (drain of $M_3$) will drop. The result is a reduction of the gate voltage of $M_{n2}$ and thus a reduction of the drain current in $M_{n2}$. The incremental drain current of $M_{n2}$ provides most of the current through the load; the load current is dominated by the change in the current of $M_{n2}$ instead of $M_2$.

Fig. 14.9 is a reasonable equivalent, incremental, circuit. The differential stage ($M_3$, minus, $M_4$, plus, and the drain of $M_3$ as the output) is represented by an opamp symbol.

*Figure 14.9. Equivalent circuit of the output stage of Fig. 14.8. The opamp symbol represents the differential-amplifier stage of $M_3$ and $M_4$.*
Since the source follower of M1 has a transfer function of nearly unity, incremental $V_{g2} (= V_{g1})$ is moved directly to gate of M3 (minus input of the differential amplifier) as in Fig. 14.9. Thus

Equation 14.39

$$V_{g2} = V_{gsn2} / a_{vda}$$

where $a_{vda}$ is the gain of the opamp and the output of the opamp is $V_{gsn2}$. The amplifier (output stage) output voltage is therefore

Equation 14.40

$$V_o = (I_{d2} - I_{dh2})R_L = \left( g_{m2} V_{gs2} + g_{mn2} V_{gsn2} \right) R_L = (1+a_{vda}) g_{m2} R_L V_{gs2}$$

where we now assume that $g_{m2} = g_{mn2}$. It follows that the relation between $V_{gs2}$ and $V_o$ is

Equation 14.41

$$V_{gs2} = \frac{V_o}{1+a_{vda} g_{m2} R_L}$$

Combining this with

Equation 14.42

$$V_g = V_{gs2} + V_o$$
gives the transfer function, input to output, as

\[
\frac{V_o}{V_{in}} = \frac{G_m R_L}{1 + G_m R_L}
\]

where

\[
G_m = (1 + a_{vda}) g_{m2}
\]

The output resistance of the circuit of Fig. 14.8 is $1/G_m$. The output resistance of the circuit of Fig. 14.8 is thus reduced by a factor of about $1/a_{vda}$ compared to the circuit of Fig. 14.7 for the same $g_m$ of the source follower transistors. From (14.18), the gain of the differential-amplifier stage is

\[
a_{vda} = \frac{2}{V_{eff3} \left( \lambda_n + \lambda_p \right)}
\]

This would typically be on the order of 100. Thus a significant benefit over the simple source-follower stage output is realized with the circuit of Fig. 14.8. It is also significant that there is no body effect associated with $M_{n2}$.

### 14.9. Summary of Equations

<table>
<thead>
<tr>
<th>$I_{D11}$</th>
<th>$I_{D10}$</th>
<th>$W_{11}$</th>
<th>$1 + \lambda_n V_{DS1}$</th>
<th>$W_{10}$</th>
<th>$1 + \lambda_n V_{DS0}$</th>
<th>Bias equation for differential amplifier stage.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{D01}$</td>
<td>$I_{D00}$</td>
<td>$W_{11}$</td>
<td>$1 + \lambda_n V_{DS1}$</td>
<td>$W_{10}$</td>
<td>$1 + \lambda_n V_{DS0}$</td>
<td>---</td>
</tr>
</tbody>
</table>

\[
a_{vcm} = -\frac{g_{m1} R_{D2}}{1 + g_{m1} 2r_{ds11}} \approx -\frac{R_{D2}}{2r_{ds11}}
\]

Differential-stage common-mode gain equation for case of drain bias resistor, $R_{D2}$.

\[
CMRR = 1 + g_{m1} 2r_{ds11}
\]

Common-mode rejection ratio for case of drain bias resistor, $R_{D2}$.

<table>
<thead>
<tr>
<th>$I_{D12}$</th>
<th>$I_{D10}$</th>
<th>$W_{12}$</th>
<th>$1 + \lambda_n V_{DS2}$</th>
<th>$W_{10}$</th>
<th>$1 + \lambda_n V_{DS0}$</th>
<th>Bias equation for common-source stage.</th>
</tr>
</thead>
</table>
### Bias equation for differential amplifier stage.

\[
\frac{I_{D11}}{I_{D10}} = \frac{W_{I11} \left( 1 + \lambda_n V_{DS11} \right)}{W_{I10} \left( 1 + \lambda_n V_{DS10} \right)} \approx \frac{W_{I11}}{W_{I10}}
\]

- **Bias equation for differential amplifier stage.**

### Common-source stage gain with current-source load.

\[
a_{vcs} = -\frac{g_{m3}}{g_{ds12} + g_{ds3}}
\]

### Amplifier gain for case of differential-stage drain bias resistor, \(R_{D2}\), and common-source stage gain with current-source load.

\[
a_v = -\frac{I_{DE} R_{D2}}{V_{eff1} V_{eff2} \left( \lambda_n + \lambda_p \right)}
\]

### Output resistance of differential stage with current-source load.

\[
R_{o2s} = \frac{1}{g_{ds2} + g_{ds5}}
\]

### Differential-stage gain with current-source load and external load resistor, \(R_L\).

\[
a_w2 = \frac{g_{m1}}{g_{ds2} + g_{ds5} + \frac{1}{R_1}} = \frac{g_{m1} R_L}{1 + (g_{ds2} + g_{ds5}) R_L}
\]

### Relation to determine \(M_3\) gate width, \(W_3\).

\[
W_3 = 2W_L \frac{W_{L2}}{W_{L1}}
\]

### Precision relation to determine \(M_3\) gate width, \(R_{D2}\).

\[
W_3 = 2W_L \frac{1 + \lambda_p V_{SD5} W_{L2} \left( 1 + \lambda_n V_{DS12} \right)}{1 + \lambda_p V_{SD8} W_{L1} \left( 1 + \lambda_n V_{DS11} \right)}
\]

### Gain for two-stage amplifier, both stages with current-source loads.

\[
a_v = -\frac{g_{m1} + g_{m3}}{g_{ds2} + g_{ds5} + g_{ds12} + g_{ds3}}
\]

### Gain of the source-follower stage for the case of load \(R_f + R_G \parallel R_O\) (feedback resistors and external load, \(R_o\)).

\[
a_{vaf} = \frac{g_{m6}}{g_{m6} \left( 1 + \eta \right) + g_{ds13} + g_{ds6} + \frac{1}{\left( R_f + R_G \right) \parallel R_O}}
\]

### Output resistance of source-follower stage.

\[
r_O \approx \frac{1}{(1 + \eta) g_{m6}}
\]

### Output resistance of resistance feedback amplifier.

\[
W_3 = 2W_s \frac{W_{L2}}{W_{L1}}
\]

### TS271 output resistance, where \(g_{m2}\) is for the source-follower stage and \(a_{vda}\) is the gain of the differential amplifier stage.

\[
W_3 = 2W_s \frac{1 + \lambda_p V_{SD5} W_{L2} \left( 1 + \lambda_n V_{DS12} \right)}{1 + \lambda_p V_{SD3} W_{L1} \left( 1 + \lambda_n V_{DS11} \right)}
\]

### Unit A. Communicating with the Circuit Board: LabVIEW Programming and Measurement Exercises

Communicating between the computer and a circuit board (sending and receiving voltages from the computer) is accomplished with the data acquisition card (DAQ). The DAQ is normally connected from the computer to the circuit board with a 68-pin cable. In general, all 68 pins are used for such things as analog inputs and outputs, triggering,
digital inputs and outputs, a 5-V dc supply, and counters. In our projects, we use, for the most part, only analog inputs and outputs. A digital output could also be used if we required an additional output, which of course is limited to on or off.

Since the analog inputs and outputs involve digital-to-analog and analog-to-digital conversions, special consideration must be given to the discrete nature of the conversion relations. These are discussed in the following along with a series of basic programming and measurement exercises. A sequence of VIs (virtual instruments) is programmed. In Unit A.2 and beyond, preprogrammed VIs are used.

The LabVIEW library, ProjectA.llb, of Project A contains the preprogrammed VIs, along with samples of all of the VIs in the exercises. Project A complements this unit. It is recommended that the parts of Project A be completed at the end of a given programming segment in the unit. The appropriate project part is flagged as with the following:

```
Project PA.x (Title of Project Segment)
```

**A.1. Basics of Sending and Receiving Circuit Voltages**

The following is based on a National Instruments PCI-MIO-16E-4 DAQ card (or equivalent). The sample rate is not critical. The DAQ card has eight differential analog input channels and two analog output channels. We generally use only channels 0, 1, and 2 for receiving in our projects.

LabVIEW provides some preprogrammed VIs for readily sending voltages to the circuit board and sampling a signal for reading into a LabVIEW program. The most important of these for analog circuit measurements are AI Acquire Waveform.vi and AO Update Channel.vi. Some measurements will be made next using these two VIs.

As the name suggests, the VI, AI Acquire Waveform.vi samples the stipulated voltage a number of specified times. For dc measurements, the samples are simply averaged. This provides for a more precision measurement than from a single sample. LabVIEW has a single-point DAQ function, AI Sample Channel.vi. This function does not take advantage of computer-based data acquisition.

**A.1.1. Programming Exercise: Installing, Sending, and Receiving VIs in the Program**

Open a new VI in LabVIEW and save it with a personal name. Here the VI is referred to as Measure.vi. The VI has a Front Panel and a Diagram. The Diagram is shown in Fig. A.1. Moving from the Diagram to the Front Panel or the opposite can be performed under menu Window>>Show Diagram (or Ctrl/E) and Window>>Show Panel (or Ctrl/E). The inputs and outputs, including graphics, appear in the Front Panel and the program is set up in the Diagram. For programming, three palettes are used: Tools Palette, Controls
Palette, and Functions Palette. The methods for getting these palettes are outlined in Table A.1.

**Figure A.1. LabVIEW Diagram with icon for AI Acquire Waveform.vi.** To place the icon in the Diagram, Right Click on the Diagram to get Functions. Click the stickpin. Then follow through the sequence: Data Acquisition >> Analog Input >> AI Acquire Waveform.vi. Go to Options in the Functions Tool Bar to Change Palette Set if desired.

Place AI Acquire Waveform.vi in the Diagram of Measure.vi. It is located in the Functions Palette and under Data Acquisition >> Analog Input (Fig. A.1). Note that the Functions Palette has various Options, that is, more or less features. To get the version shown in Fig. A.1 (if is not already in this form), go through Options in the Functions Tool Bar (Fig. A.1).

<table>
<thead>
<tr>
<th>TABLE A.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diagram</td>
</tr>
<tr>
<td>---------</td>
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<tr>
<td></td>
</tr>
</tbody>
</table>
When installed, AI Acquire Waveform.vi appears as in Fig. A.1. Now Double Click on the icon (or Right Click and Open Front Panel) to bring up the Front Panel of AI Acquire Waveform.vi. It will appear similar to the example shown in Fig. A.2, which has some cosmetic changes.

**Figure A.2. Front Panel of LabVIEW VI AI Acquire Waveform.vi. Digital Controls provide for various inputs including the number of samples to be taken, in this example, 1000. The output is the designated waveform and is an array of sample values of index 0 through 999 in this case.**

The Digital Controls in the Front Panel of AI Acquire Waveform.vi provide for installing the machine device number (e.g., 1), the input channel, number of samples, and sample rate in addition to the ADC (analog-to-digital converter) Digital Controls high limit and low limit. The default, 0 V, as in the example, is equivalent to 10 V and –10 V for high limit and low limit, respectively.

The device number of the DAQ card is set using the National Instruments Measurement & Automation utility. Go to Start>>Programs>>National Instruments>>Measurement &
Automation. This opens a window called Max. Then under My System, locate Devices and Interfaces and Right Click on the name of the DAQ card to bring up Properties. The device number can be set from the Properties window. The sample programs in ProjectA.llb use Device 4 (or as set on your PC). Close Max.

We will want to send out some voltages to be read by the input channel. For this, add output channel function AO Update Channel.vi to the Diagram of your VI. It is under Functions>>Data Acquisition>>Analog Output. Install this VI in your VI diagram as shown in Fig. A.3. Position the icons with the Positioning Tool (arrow). It is obtained by cycling through the Tools by striking the Tab key or Space Bar, or, again, get the Tools Palette with Shift/Right Click from the Front Panel or Diagram.

*Figure A.3. LabVIEW VI Diagram with the addition of output channel VI AO Update Channel.vi. The two VIs represented by the icons can be opened with Right Click and open Front Panel or with Double Click.*

Project PA.1 Sending and Receiving Voltages with the Sending and Receiving VIs (Measure.vi, version 1)

A.1.2. Programming Exercise: Using a Sequence Structure

The two VIs represented by the icons of the Diagram are subVIs of Measure.vi. That is, they will run when we run Measure.vi. In this case, it is necessary that they execute in the proper order. For example, we would want to send out the voltage before reading the response.

For ensuring proper execution order, install a Sequence Structure as shown in Fig. A.4. Obtain the Sequence Structure from the Diagram under the menu series Functions>>Structures>>Sequence. Recall that to obtain the Functions Palette, Right Click on the Diagram.

*Figure A.4. LabVIEW VI Diagram with Sequence Structure. This Structure executes in order of index at the top of the Frames. Frame 1 shown contains the VI for reading voltage. Frame 0 contains the VI for sending voltage. Click on*
Initially, the Sequence Structure is too small. To enlarge, get the Positioning Tool (arrow) by pressing the Space Bar, by sequencing through the Tools with Tab, or by using Shift/Right Click to bring up the Tools Palette. Position the Tool at the lower-right-hand corner of the Sequence Structure, Left Click, and drag to enlarge the Structure.

Right Click on the edge of the Frame of the Sequence Structure and go to Add Frame After (Fig. A.4). The result will be two Frames with index 0 and index 1. Now place (e.g., drag) the send and receive VIs into Frame 0 and Frame 1, respectively. Left Click on the left and right arrows at the top of the Sequence Structure to move between Frames. The result will be as shown in Fig. A.4. The Diagram shows Frame 1. The program will execute the VI in numerical Frame order. Thus, the output voltage will always be sent before the input channel attempts to read.

A.1.3. Programming Exercise: Digital Controls and Digital Indicators

The Front Panel of Measure.vi will now be configured to permit assigning the voltage to be sent out and reading the input voltage from the Front Panel. The Front Panel of the new configuration is shown in Fig. A.5. From the Front Panel and then from the Controls Palette, go to Controls>>Numeric (Fig. A.5), and from this selection, get a Digital Control and a Digital Indicator. You might want to color the Front Panel. For this, Shift/Right Click and get the Coloring Tool from the bottom of the Palette. Then, with the Coloring Tool, Right Click on the Front Panel and pick a color. You can also color the Diagram. Change the labels over the Digital Control and Digital Indicator using the
Edit Text Tool (Fig. A.5). Obtain the Tools Palette with Shift/Right Click and the Edit Text Tool. The labels are defaulted as Numeric. Use the Edit Text Tool from the Tools Palette to relabel as in the example (or similar).

**Figure A.5. Front Panel with addition of Digital Control (send) and Digital Indicator (receive). These are obtained with a Right Click on Front Panel for Controls Palette and then Numeric and Digital Control and Digital Indicator. Also shown is the Edit Text Tool for changing the labels on the Controls from the default Numeric.**

Now go to the Diagram (under Menu Window>>Show Diagram or use Ctrl E) for wiring the program in the diagram. This will include Terminals and Numerics and Strings. Start by connecting the sending VI icon (Frame 0) value to the Digital Control terminal (Fig. A.6). To locate the terminal for the Digital Control, go back to the Front Panel, Right Click the Digital Control for Send Volts, and move the pointer to Find Terminal. The Diagram will open and the proper terminal will be highlighted. Note that the terminal for Digital Control is darker than those for Digital Indicator. This provides for an alternative means of locating the proper terminal.

**Figure A.6. Top Diagrams: Locating the value terminal on the icon and moving the Wiring Tool to the Digital Control terminal. Bottom Diagrams: Completed wiring for Frame 0 and Frame 1. Completion of Frame 1 is discussed below.**
Get the Wiring Tool (appears like a roll of solder) by striking the Space Bar. To wire, first find the correct terminal on the icon. There are three in this case. The terminal for this connection, value, is the bottom third of the icon. To locate the region of the connection, sweep the Wiring Tool over the icon and find the value. A given terminal displays a black-and-white blinking while the Wiring Tool is in contact with this terminal. Now, with the Wiring Tool, Left Click on the value connection region, Release, and move the Wiring Tool to the terminal of the Digital Control. Left Click again to finish.

For an alternative view of where the connections are made, you can Right Click on the icon, and get Visible Items>>Terminals. Recall again that the Digital Control terminal is darker than the Digital Indicator terminal. This adds additional clarification as to the correct terminal.

Complete the connections to the icon with a Numeric Constant for the device (Right Click, then Functions>>Numeric>>Numeric Constant) and a String Constant for the channel (Right Click, then Functions>>String>>String Constant). Use the Pointing Tool (finger) to write in the constant values. Obtain the various Tools by striking the Tab key.

Now sequence to Frame 1 to connect to the AI Acquire Waveform.vi icon. (Click on the arrows at the top of the Sequence Structure.) Complete all wiring, as shown in Fig. A.6, except for the waveform terminal (connection on the right side of the icon in Frame 1). This includes device (numeric constant, 4), channel (string constant, 0), number of
samples (numeric constant, 100), high limit (numeric constant, 10), and low limit (numeric constant, 0). The low limit can be set to 0 because no negative numbers are to be read.

As a reminder for using the Wiring Tool: In the Diagram, use Shift/Right Click to get the Tools Palette and obtain the Wiring Tool. The Wiring Tool is also obtainable by pressing the Space Bar, while the Diagram is the active window, to sequence between the Wiring Tool and the Positioning Tool. Left Click on the terminal to be wired (do not hold) and move the Tool to the other termination and Left Click again.

A.1.4. Programming Exercise: Using the Array Average Value VI from Probability and Statistics for Averaging the Samples Received

To complete connections to the terminals associated with Frame 1, we must add the VI Mean.vi (Fig. A.7). It is used to obtain the average of all of the number of samples (as selected) in the reading (receiving) function. Note that Mean.vi is connected between the waveform terminal of the AI Acquire Waveform.vi and the Digital Indicator terminal. The output from AI Acquire Waveform.vi (waveform) in this case is a cluster of information including a data array. In the Diagram, a much broader line than that for a single data point represents the connection.

**Figure A.7. Diagram showing Frame 1. The VI Mean.vi has been added to average the data samples.**

Mean.vi is obtainable from two different locations in the Functions palette: Functions>Analyzer>Mathematics>Probability and Statistics>Mean.vi; Functions>Mathematics>Probability and Statistics>Mean.vi. Connect the waveform of the Frame 1 icon to Mean.vi to the Digital Indicator Terminal. Connect the output in Mean.vi, mean, to the Terminal of the Digital Indicator. This measurement, which is the average of a large number of samples, is superior to obtaining a single point that might very well fluctuate due to noise.
Project PA.2 Sending and Receiving Voltages from the Front Panel (Measure.vi, version 2)

A.1.5. Programming Exercise: Installing and Using the Waveform Graph

A given dc voltage is sent out via an output channel (e.g., frame 0 of Fig. A.7). A circuit node response is measured, in our projects, by sampling the voltage a number of times. With LabVIEW, we can easily obtain a graphical presentation of the sample data points to provide an indication of the noise that exists on the dc voltage being measured and in the measurement system. For this, obtain a new VI by saving a Save As copy and giving it a new name. Here it is named PlotSamples.vi. The new VI will initially appear something like that in Fig. A.8.

Figure A.8. Front Panel with addition of a Waveform graph. The graph is obtainable from the Front Panel under Controls>>Graph>>Waveform Graph.

To install the Waveform graph, in the Front Panel, Right Click and get Controls>>Graphs>>Waveform Graph and place it on the Front Panel. Shift/Right Click on the face of the graph to get the Coloring Tool and pick a color for your graph background field and Frame. Figure A.8 shows a new graph installation with some color changes.

A new installation of a graph has the Plot Legend open (Plot 0 in the example). In general, this feature and others can be hidden or made to appear by a Right Click anywhere on the graph and then selecting Visible Items as shown in the example of Fig. A.9.
**Figure A.9.** Various graph features are obtained under Visible Items as shown. This includes the Plot Legend for setting up the plot style.

In the box of the Plot Legend, Right Click, go to Color and pick a color for the plotting points or lines. Also, select Points under Common Plots. Hiding the Plot Legend might be in order, now although this is optional. (Right Click on the graph face and select Visible Items>>Plot Legend.)

For the present application, it is preferred to have no grid. To accomplish this, Right Click on a number on the Y-scale of the Frame of the graph, go to Formatting... and Grid Options (Fig. A.10). Select the no grid (Left Click) condition as illustrated in Fig. A.10. Repeat for the X-axis. Note that a given axis can be selected from the Formatting window at the top under Select Scale.

**Figure A.10.** Y-scale Formatting showing the section of no grid from Grid Options. Selection of Digits of Precision is also made in this window.
Now use the Edit Text Tool to edit the X and Y designators. Then Right Click on the graph face and get Find Terminal. Complete the wiring to the graph terminal as in Fig. A.11. The final Front Panel (Fig. A.11) has the label hidden and the X- and Y-axis designators edited to be Sample Value(V) and Time (sec). The graph data are from a sample measurement from Project A.

**Figure A.11. Completed Front Panel and Diagram showing connection to the terminal of the Waveform graph.**

![Completed Front Panel and Diagram showing connection to the terminal of the Waveform graph.](image)

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**Project PA.3** Plotting Measured Samples (PlotSamples.vi)

### A.2. ADC and the Autoranging Voltmeter

Very often in measuring circuit characteristics, it is necessary to plot some voltage response over a wide range of input-voltage stimulation. An automatic means of adjusting the voltmeter sensitivity through the sweep is thus required. When set for the full measurement range (limit), the 12-bit analog-to-digital conversion (ADC) in the DAQ has either a 2.44 mV (unipolar, 10 V full range) or a 4.88 mV (bipolar, 20 V full range) resolution.

However, the range of the DAQ is software selectable. So, for example, suppose that in the sweep we are measuring 5 mV and only positive voltages. The DAQ can be programmed for a high limit of, for example, 100 mV and a low limit of 0 V (unipolar), such that the resolution is 24.4 μV.

The Project A LabVIEW library, ProjectA.llb, contains a preprogrammed VI for setting automatically the range. The Diagram of the VI, Voltmeter.vi, is shown in Fig. A.12. As indicated, the range is set through the high- and low-limit inputs to AI Acquire.
Waveform.vi, for example, 10 V (high limit) and 0 V (low limit) in the diagram of our autoranging voltmeter as shown in Fig. A.12.

**Figure A.12. Diagram of autoranging dc voltmeter, Voltmeter.vi. The While Loop runs until the comparison finds the measured value less than the lowest possible limit.**

The autoranging voltmeter is programmed as follows. First, a copy of AI Acquire Waveform.vi is Saved As..., modified for dc only and renamed as AI Acquire Avg.vi. The modification consists of taking the average of the array of samples and providing for a single-point output of the average value of the samples. AI Acquire Avg.vi is programmed to operate in selectable bipolar or unipolar mode. Thus, this feature is included in Voltmeter.vi.

This VI is then used as a subVI in the autoranging dc voltmeter. Upon running Voltmeter.vi, the execution starts with the subVI AI Acquire Avg.vi on the left; the high limit set at 10 V, and with the bipolar mode, the lower limit is –10 V. Thus the voltage being measured is first sampled with minimum sensitivity but this is sufficient to obtain an approximate value of the voltage. The initial measurement value is then processed through a selection scheme to decide which limit should be set into the final measurement subVI that is again AI Acquire Avg.vi. The limit choices are given in Table A.2. These are stored in an Array Digital Control as seen on the left in the diagram. The While Loop compares the measured value with each limit value starting at the top. The loop halts when the comparison finds the smallest possible limit. Bipolar or unipolar are set according to the sign of the initially measured value.
A factor of 2 of improved resolution is available with the unipolar case. As noted, the valid limit settings and associated resolutions are shown in Table A.1. With the autoranging voltmeter, during a sweep, the resolution is maintained, through the sweep, at roughly a fixed percentage of the value of the numbers being measured.

**Table A.2**

<table>
<thead>
<tr>
<th>Unipolar</th>
<th>Range</th>
<th>Resolution</th>
<th>Bipolar</th>
<th>Range</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 to +10 V</td>
<td>2.44 mV</td>
<td></td>
<td>-10 to +10 V</td>
<td>4.88 mV</td>
</tr>
<tr>
<td></td>
<td>0 to +5 V</td>
<td>1.22 mV</td>
<td></td>
<td>-5 to +5 V</td>
<td>2.44 mV</td>
</tr>
<tr>
<td></td>
<td>0 to +2 V</td>
<td>488 μV</td>
<td></td>
<td>-2 to +2 V</td>
<td>1.22 mV</td>
</tr>
<tr>
<td></td>
<td>0 to +1 V</td>
<td>244 μV</td>
<td></td>
<td>-1 to +1 V</td>
<td>488 μV</td>
</tr>
<tr>
<td></td>
<td>0 to +500 mV</td>
<td>122 μV</td>
<td></td>
<td>-500 to +500 mV</td>
<td>244 μV</td>
</tr>
<tr>
<td></td>
<td>0 to +200 mV</td>
<td>48.8 μV</td>
<td></td>
<td>-200 to +200 mV</td>
<td>122 μV</td>
</tr>
<tr>
<td></td>
<td>0 to +100 mV</td>
<td>24.4 μV</td>
<td></td>
<td>-100 to +100 mV</td>
<td>48.8 μV</td>
</tr>
<tr>
<td></td>
<td>-50 to +50 mV</td>
<td>24.4 μV</td>
<td></td>
<td>-50 to +50 mV</td>
<td>24.4 μV</td>
</tr>
</tbody>
</table>

*Figure A.13* shows a measurement of a sine-wave from a function generator. This was obtained in LabVIEW using the ac voltmeter that is discussed in a following unit. The voltage waveform is sampled at the two limit settings, 100 mV (a) and 2 V (b). The peak of the sine-wave is 10 mV. It is clear that the resolution is not adequate at the higher limit setting. In an autoranging version of the ac voltmeter, the best limit setting is automatically assigned.

*Figure A.13. LabVIEW measurement of a sine-wave voltage with peak of 10 mV. The sinewave is sampled at two limit settings of (a) 100 mV and (b) 2 V. The resolutions are (a) 48.8 μV and (b) 1.22 mV.*

Project PA.4 Using the Autoranging Voltmeter
A.3. LabVIEW Oscilloscope and Voltmeter (ac)

An example of an oscilloscope is shown in Fig. A.14. This special version displays three waveforms. These are the total waveform (ac + D), the sine-wave minus the dc (average value) and the absolute value of the sine-wave (|ac|).

**Figure A.14. Front Panel for a possible LabVIEW oscilloscope. Digital Controls provide for inputs of Frequency, Count (number of samples), and #cycles. Digital Indicators show Samples/Sec, Sec/Sample, VDC, and Vac Peak. The limits are set in the Diagram.**

![Oscilloscope Front Panel](image)

The voltmeter is designed to measure peak or RMS values for periodic waveforms, thus, to be an ac voltmeter. Total sampling time must occur in exact multiples of cycles. This provides for obtaining the waveform (sine-wave) peak or RMS value based on an average of all the samples.

The required sample rate, SR, is obtained from

\[
SR = \left[ \frac{\#Samples}{\#Cycles \times \text{Frequency}} \right] \times \text{Samples/Sec}
\]

The values for all the numbers on the right-hand side are set in Digital Controls on the Front Panel (Fig. A.14). The #Samples is also referred to as the Count.

SR and #Samples are then sent to the subVI, AI Acquire Waveform.vi. For example, assume that the #Cycles is 4 and the #Samples is 256. Once cycle will be sampled 64
times. Assume also that f = 1000 Hz. Sample rate SR will be 64000 samples/sec or about 16 μsec/sample. The total sampling time is T · #Cycles, where T is the period and is T = 1/f. In this example this is 4msec.

Digital Indicators in the Front Panel display the dc voltage, VDC, and the peak, Vac Peak. Vac peak is calculated as the average value of |ac| multiplied by π/2. The programming sequence for obtaining the three waveforms is shown in Fig. A.15. In the Sequence Frame is also shown the programming configuration for connecting to the graph on the Front Panel and the computation of the peak value, Vac Peak.

**Figure A.15. Frame of Sequence Structure showing series of events for obtaining ac peak value. The mean is subtracted from the array with the result converted to the absolute value, and the average is multiplied by π/2.**

![Diagram of Sequence Structure](image)

**Project PA.5** Observing the Oscilloscope Output Graph

**A.4. Measuring the Discrete Characteristics of Sending and Receiving Voltages**

In the discussion above of the autoranging voltmeter, the discrete nature of the ADC and DAC was demonstrated. LabVIEW VIs that plot the input voltage versus output voltages for both ADC and DAC demonstrate the effect further.

**Figure A.16** shows the Front Panel of the VI Discrete.vi. This VI is for demonstrating the discrete nature of the sending and receiving functions. We first consider that of the sending function, as in the case of Discrete.vi in **Fig. A.16**.

**Figure A.16. DAC in the bipolar mode. Plot of the programmed voltage sent out (0.1-mV steps) versus measured actual output voltage. The graph on the right is a plot of the input voltage samples for a single output sweep.**
The graph on the left shows the voltage actually sent out (Y-axis) for a quasi-continuous range of requested (programmed) voltage to be sent out (X-axis). In the example, the program called for the output voltage to be swept over a range from –10 to 10 mV in steps of 100 \( \mu \)V. The actual voltage sent out is discrete in steps of 4.88 mV; thus only four steps over the entire range are sent out. The graph on the right is a plot of the input voltage samples from one (the last) measurement. The plot illustrates the inherent scatter in this type of measurement.

Project PA.6 Discrete Output Voltage from The DAQ

In Fig. A.17 is shown the result of measuring a high-resolution output sweep with a less precision input mode of measurement. The high resolution is obtained with a resistance voltage divider. The graph on the left shows the discrete nature of the receiving function for a low-resolution mode. For the limit settings, the receiving resolution is 4.88 mV.

Figure A.17. The full range of the output sweep is 10 mV. (The X-axis is before the 100:1 voltage division.) The input channel has low resolution, as revealed by the steps in the plot.
The transition regions are nonabrupt due to the bit uncertainty (due to noise) in these regions. In Fig. A.18 is shown input voltage samples (for one output voltage) for a point in a plateau region (a) and for a point in the transition region (b). Note that the plot in the graph on the right in Fig. A.17 is for a plateau region (last point in the sweep in the plot on the left) and shows no scatter.

**Figure A.18.** (a) Chan0_in samples for a voltage in a plateau region in the plot of **Fig. A.17**. (b) Samples for a voltage from the transition region.
A.5. Sending and Receiving Waveforms

Measuring circuit response to waveform input signals requires simultaneous sending and receiving data with the DAQ. An example was demonstrated above with the oscilloscope measurement project (Fig. A.14). The function generator VI used for that measurement is FG_A.vi. The main subVI of the function generator VI is SR_A.vi. The Front Panel and Diagram of the VI are shown in Fig. A.19. The VI sends and receives voltage arrays from one output channel and one input channel.

Figure A.19. The Front Panel and Diagram of SR_A.vi. LabVIEW AO Write receives the array of the numerical values of the waveform and sends them out on the output channel. The oscilloscope is launched in sequence and measures the response voltage of the input channel while the output array is still being executed.

Information supplied from the top VI, FG_A.vi, includes sine-wave (or square-wave) frequency (Frequency), number of cycles (Cycles), and number of samples per cycle (Samples/Cycle). The information is used to facilitate the computation Sample Rate =
Frequency · Sample/Cycle and the size of the waveform data array (Cycle · Samples/Cycle).

The subVI, SR_A.vi, receives this information along with the waveform data array, as required by the functions in the Diagram of SR_A.vi (Fig. A.19). The waveform data array is calculated by a subVI, Sine-wave.vi (on the same level as SR_A.vi). (An alternative waveform, SquareWave.vi, is selectable from FG_A.vi). The execution sequence is AO Config.vi, AO Write.vi, AO Start.vi, OscilloscopeA.vi, AO Wait.vi, and AO Clear.vi.

The Number of Cycles is adjusted automatically in the top VI and increases for higher frequencies. The increase provides assurance that the outgoing waveform is still executing during the oscilloscope measurement phase. The duration of the waveform sent out is Cycles · T.

Project PA.8 Using the Simultaneous Sending/Receiving Function

A.6. Summary of Programming Projects

- PA.1 Sending and Receiving Voltages with the Sending and Receiving VIs
- PA.2 Sending and Receiving Voltages from the Front Panel
- PA.3 Plotting Measured Samples
- PA.4 Using the Autoranging Voltmeter
- PA.5 Observing the Oscilloscope Output Graph
- PA.6 Discrete Output Voltage from the DAQ
- PA.7 Discrete Input Voltage from the Circuit Board
- PA.8 Using the Simultaneous Sending/Receiving Function

Unit B. Characterization of the Bipolar Junction Transistor for Circuit Simulation

The inclusion of transistors in circuit simulation requires a model for the transistor. That is, the simulator needs to know how the transistor behaves. Specifically, the simulator requires knowledge of the terminal characteristics of the transistor. For example, for a given dc voltage $V_{BE}$ applied between terminals B (base) and E (emitter), what will be the current into B ($I_B$)? The mathematical relations are obtained from theory or experimental observation. Often, the theory is very complicated, but much more simple relations serve very well as good approximations.

| TABLE B.1 |
The parameters for the BJT, which are to be determined in the projects as described in the following, are given in Table B.1. The parameters are obtained by fitting the mathematical expressions as used by SPICE to measured current – voltage relations.

### B.1. Fundamentals of Bipolar Junction Transistor Action

A bipolar junction transistor is made up of a sandwich of two semiconductor pn junctions. Transistors are either npn or pnp. In the active-mode transistor state, one junction, the input junction, is forward biased, and the opposite junction, the output junction, is reverse biased. The behavior of the individual pn junction diode will first be considered to clarify forward and reverse bias.

A semiconductor pn-junction diode in diagrammatic form is shown in Fig. B.1. The current and voltage of an ideal pn-junction diode are related by

\[
I_D = I_{SD} \left( e^{V_D/V_T} - 1 \right)
\]

*Figure B.1. Diagrammatic pn-junction diode. Applied voltage \( V_D \) is shown for forward bias for which current freely flows. Opposite polarity is reverse bias, where the diode is essentially cut off and \( I_D = -I_S \).*
where $V_D$ is the voltage applied between the p and n regions (positive at the p terminal), $I_D$ is the responding current, and $I_{SD}$ is the saturation current. The thermal voltage, $V_T$, is defined as $V_T = kT/q$, where $T$ is the temperature, $k$ is the Boltzmann constant and $q$ is the electron charge. At $27^\circ C$, $V_T \approx 26 \text{ mV}$. $V_D$ is positive for forward bias and negative for reverse bias.

As illustrated by the arrows in the junction of Fig. B.1, for forward bias, the diode current consists of injection of holes from the p region (positive free carriers) into the n region and injection of electrons from the n region (negative free carriers) into the p region. The exponential factor in (B.1) is associated with the statistics of the free carriers, holes and electrons, and the effect on the lowering of the barrier to free-carrier flow of the application of the positive applied voltage.

The magnitude of $I_{SD}$ is dependent on semiconductor electronic properties such as doping levels and free-carrier lifetime and mobility. The magnitude of current flow for a given $V_D$ is dictated by a combination of the barrier-lowering factor (in the exponential) and the rate of free-carrier recombination; that is, carriers are annihilated by recombining with the opposite type of carrier on the opposite side of the junction from which they are injected.

A typical value for saturation current, $I_{SD}$, is $10^{-11}$ mA, such that, for example, for $V_D = 0.6 \text{ V}$, $I_D \approx 0.1 \text{ mA}$ and increases by an order of magnitude for each additional increment of $\delta V_D \approx 60 \text{ mV}$ (at room temperature). The equation would suggest that for negative $V_D$ and $|V_D| >> V_T$, $I_D = -I_{SD}$ and therefore is very small compared to the current under forward bias. In real pn-junction diodes, the current is larger and is not independent of the value of the reverse applied voltage. Nonetheless, it is still very small compared to the value of current for normal forward bias.

As mentioned above, the bipolar junction transistor is made up to two junctions, which share a common region. A pnp example is shown in Fig. B.2. The individual pn junctions of a transistor also exhibit diode characteristics, and the junction currents are related to the junction voltages by equations similar to (B.1). There is an essential difference that can be explained for the case of one junction being forward biased while the other junction is zero or reverse biased. Specifically, suppose that the transistor is a pnp (the
other possibility being the npn) and the pn junction on the left (input junction) is forward biased and the pn junction on the right (output junction), is made to have zero bias by connecting a wire across this junction, as shown in Fig. B.2.

**Figure B.2. Diagrammatic semiconductor pnp transistor. The input junction on the left has forward bias voltage $V_D$, and the output junction on the right is shorted for zero bias. The input pn-junction diode current $I_D$ couples with the output pn junction to flow into the output p region.**

![Diagram of a pnp transistor with forward bias voltage $V_D$.]

Even though the forward-biased pn junction on the left shares the n region with another pn junction (on the right), it behaves like a pn-junction diode such that the current – voltage relation for the junction still has the form of (B.1) and is

Equation B.2

$$I_D = I_S \left( e^{V_D/V_T} - 1 \right)$$

The saturation current is now designated $I_s$, since $I_s \neq I_{sd}$. [If the width of the n region is very large, the holes injected into the n region will recombine with electrons in the n region, and the associated current will flow entirely out through the contact to the n region. In this limiting case, the current – voltage relation for the junction on the left reverts to (B.1). The presence of the p region on the right will play no role.]

In a transistor, the n-region width is made small and the statistical chance of an injected hole surviving the transit across this region, without recombining with an electron, is very high. Upon entering the p region on the right, the holes are accommodated by the exit of an equal number of holes moving out at the contact to this p region. (Actually, they are converted to electrons at the interface of the contact and semiconductor to be consistent with having only electron flow in the metal contact and device connecting metal.)
In an ideal transistor, this is the only current mechanism. The various other current components of the real transistor are discussed below. These include electron injection that would be expected from the n region into the p region of the forward-biased junction on the left (as in Fig. B.2). In practice, special fabrication techniques are employed to make this component of current very small.

In the application of a transistor in the active mode, as for example, in an analog amplifier stage, the output junction is reverse biased, as shown in Fig. B.3. The junction configuration now represents a transistor; the regions are accordingly designated as emitter (E), base (B), and collector (C). Consistent with these assignments, the current into the transistor on the left is the emitter current, \( I_E \), and the output current on the right is the collector current, \( I_C \), and according to the mechanism described above for the ideal transistor, \( I_C = I_E \).

\[ \text{Equation B.3} \]

With forward bias (voltage) across the emitter – base junction and reverse bias across the collector – base junction, the emitter – base current equation, (B.2), is slightly altered, to become

**Equation B.3**

\[ I_E = I_C = I_S \exp \left( \frac{V_{EB}}{V_T} \right) \]

Variable subscripts have been changed to reflect the fact that the pnp structure is now specifically a transistor. (The parameter \( I_S \) is the same in SPICE for the diode and the transistor models. \( I_{sd} \) was used above for this discussion alone to differentiate between the two.) For reverse bias of the collector – base junction, the \(-1\) of (B.2) is eliminated.
In this simplified version of the transistor, the output current is independent of the collector–base voltage. The possibility of infinite voltage gain is thus provided, because the output circuit behaves like a pure current source; that is, it will force current into an external resistance, which can be large without limit. This conclusion remains subject to additional alterations for the real transistor. However, in principle, the transistor mechanism as discussed is applicable short of certain limitations.

An example of obtaining gain from a transistor in an amplifier circuit is shown in Fig. B.4. A ground has been added at the n-region terminal to establish a reference. Therefore, the output voltage, $V_O$, is defined with respect to this reference. To the transistor circuit of Fig. B.3, we have added an input signal $V_{eb}$ and a load resistor, $R_L$. Note that since the input and output are referred to the base, the circuit is a common-base amplifier.

**Figure B.4. Amplifier circuit incorporating a pnp transistor. The output voltage is with respect to ground at the n-region terminal. The base is common to the input and output and hence, this is the common-base amplifier configuration.**

Suppose that initially, $V_{eb} = 0$ and $V_{EB}$ is selected to give $I_C = 1$ mA. This is, in an amplifier, the bias current. The output supply voltage is chosen to be $V_{CC} = 12$ V. We select $R_L = 5 \, k\Omega$ giving a bias output voltage $V_O = I_C R_L = 5$ V. Note now that the collector-base bias voltage is $V_{BC} = V_{CC} - V_{RL} = 7$ V and the junction is reverse biased.

We now apply an input voltage (signal, ac, or incremental voltage) $V_{eb} = 18$ mV. This increment added to $V_{EB}$ will cause $I_C$ to double (i.e., $I_C = 2$ mA). The result is a new output voltage of $V_{O}(sig) = 10$ V. Thus the incremental (or signal) output voltage is $\delta V_O = V_{O}(sig) - V_O = V_e = 5$ V. Base–collector voltage is now $V_{BC} = V_{RL} = 2$ V and the junction remains in a reverse-bias state.

The incremental (ac or signal) ratio of output and input voltage is $V_o/V_{bc} = 5V/18 \, mV = 278$. Note that the gain is power-supply limited. Employment of a larger power supply permits the use of a larger $R_L$, which results in a higher gain. We will later show that the
gain is in fact $V_{RL}/V_T$ based on an approximate linear representation between the input and output voltage. Note that in this case, the linear approximation is $V_{RL}/V_T = 192$, which indicates, for the example above, that the linear relation provides a fair estimate.

An alternative bias arrangement is shown in Fig. B.5. The input terminal is now that of the n region and the p terminal is a common node to the input and the output. This is the common-emitter configuration. Note that the voltage applied to the input junction has not changed, and the output junction now has a bias voltage of $V_{EC} - V_{EB}$ and remains reverse biased as long as $V_{EC}>V_{EB}$.

**Figure B.5. Common-emitter transistor amplifier configuration.** The common terminal is now the p-emitter region and the input is at the base (n region). The output is between the common emitter and the collector. This diagram includes a possible $I_B$ and thus $I_C < I_E$, as is discussed in Unit B.3.

In electronic amplifiers, all three terminal configurations are possible: common base, common emitter, and common collector (emitter follower). The most frequently employed amplifier stage is based on the common-emitter mode, but the other two serve important roles in electronic amplifiers. In all three, the emitter – base voltage is the input control-terminal voltage. In the common-emitter and common-base, the output current is the collector current and in the common collector, it is the emitter current. The common-collector configuration is usually referred to as the emitter follower.

In the subunits that follow, the detailed SPICE relations that generally relate the branch currents to the terminal voltages are developed. This includes the addition of many aspects of the real transistor which were not included in the discussion above of the highly idealized transistor.

Initially, the forward-active mode is explored, and this is followed by a discussion of the reverse-active mode. The reverse-active mode is where the situation in Fig. B.3 is reversed. Thus, $V_{CB}$ is positive (base – collector junction forward biased), while $V_{EB}$ is
zero or negative. In the reverse-active mode, $V_{CB}$ becomes the input voltage, and the output current is the emitter current, $I_E$.

Although the transistor is not operated in the reverse-active mode, the relationships developed for this case can be combined with those from the forward-active mode. The combination produces the general equations for relating currents and terminal voltages in transistors for all bias possibilities (i.e., where the transistor is biased out of the active mode).

**B.2. Base-Width Dependence on Junction Voltage**

In real transistors, the base width depends on the voltage applied across a pn junction. The effect is known as base-width modulation. A diagrammatic representation of the effect is illustrated in Fig. B.6. Not shown in the diagrams in Unit B.1 of the npn structure are the depletion regions, which are shown shaded in Fig. B.6. These are the transition regions that are depleted of free carriers, and in which the barrier is formed that impedes electron and hole flow to the p regions and n region, respectively. The base width (n region) is actually the width between the depletion regions. In the diagram of Fig. B.6, we define $w_{Bo}$ for $V_{BC} = 0$ and $w_B$ for $V_{BC} > 0$.

**Figure B.6. Diagrammatic npn structure showing the effect of base – collector voltage on base width.**

The magnitude of saturation current, $I_S$, in (B.3) is specifically defined for $V_{BC} = 0$ or $w_{Bo}$. In a circuit application, though, $V_{BC}$ will in general be nonzero and the base width can vary as shown; in the example of Fig. B.6, the base width is $w_B$ for a given applied $V_{BC}$. To a reasonable approximation, the relationship between the effective saturation current with a nonzero $V_{BC}$ can be accounted for with the form.

**Equation B.4**
where $I'_S$ is the effective saturation current for a reverse-applied base–collector voltage. The approximate form assumes that $V_{BC} \ll V_{AF}$. The expression in the denominator, $1 - \frac{V_{BC}}{V_{AF}}$, comes from the fact that $I'_S$ is approximately inversely proportional to the base width, and the base width is roughly

**Equation B.5**

$$w_B = w_{B0} \left(1 - \frac{V_{BC}}{V_{AF}}\right)$$

The parameter $V_{AF}$ is called the Early voltage for forward-active operation. It has a counterpart for reverse-active operation, $V_{AR}$. The base-width dependence on junction voltage is included in the nonideal factors taken up in **Unit B.3**.

**B.3. BJT Base, Emitter, and Collector Currents in the Active Mode**

The discussion of the transistor mechanism of **Unit B.1** is extended here to include base-current mechanisms, which exist in the real transistor, and the effect of base-width modulation as discussed in **Unit B.2**. Initially, the case of active-mode operation is discussed, and this is followed by the general-bias case, which includes the possibility of both pn junctions becoming forward biased.

In the device model for the bipolar junction transistor, the parameter $\beta_{DC}$ is

**Equation B.6**

$$\beta_{DC} = \frac{I_C}{I_B}$$

where $I_B$ is the composite of all contributions to the base current. (The use of "dc" is consistent with SPICE.) This relates the output current, $I_C$, to the input current, $I_B$, for the transistor operated in the common-emitter terminal configuration.
In the following, the discussion is based on the npn transistor, as shown now with the schematic symbol in Fig. B.7. The npn is chosen over the pnp, as it is substantially more basic to BJTs than the pnp. This probably has to do mostly with the fact that a common-emitter stage is consistent with a positive power supply (a holdover from the vacuum-tube days), that the npn is superior in terms of frequency response, and that it has consistently been the device of BJT digital switches including the TTL. The pnp was used in the discussion above on the fundamentals of transistor action, as it is somewhat more intuitively satisfying to have the current and particle flow (where the illustration is with the hole) in the same direction.

**Figure B.7. BJT (npn) in the common-base configuration, showing terminal voltages and branch currents.**

\[ I_E = I_C + I_B \]

The assignment of polarities of voltages \( V_{BE} \) and \( V_{BC} \) is consistent with forward bias for both the emitter–base and collector–base junctions. \( V_{BC} \) will be negative in active-mode operation. The assignment of \( V_{CE} \) is standard, as it will be positive in active-mode operation. Current directions are assigned to correspond to the actual directions of the currents in the forward-active mode.

Base currents do not couple between junctions. Rather, as suggested in Fig. B.8, a given base current is associated with a given pn junction. In the forward-active mode, a base-current component is added to the emitter current as indicated in Fig. B.7. However, since the base–collector junction is reverse biased, the base-current contribution to the collector current is negligible and (B.3) still represents the total collector current. The collector-current relation with the base-width-modulation effect (Unit B.2) now included becomes

**Equation B.7**

\[ I_C = I_S e^{\frac{V_{BE}}{V_T}} \left( 1 - \frac{V_{BC}}{V_{AF}} \right) \]
Figure B.8. Diodelike characteristics of the base currents. They are separately associated separately with their respective pn junctions. These currents do not couple across the base.

The equation has also been generalized to include the SPICE parameter $n_F$, the forward current emission coefficient (which is usually assumed to be 1).

The base current, for the forward-biased base – emitter junction, is made up of two terms; these are the ideal base current (because it has the same $V_{BE}$ dependence as $I_C$) and the leakage base current. The leakage component is typically small enough to be neglected and often is, for simplicity, in practice.

In the absence of leakage base current, the base current is

**Equation B.8**

$$I_B = I_{SBE} \left( \frac{V_{BE}}{n_FV_T} - 1 \right)$$

where $I_{SBE}$ is the base – emitter saturation current. In the active mode, $V_{BE}$ is positive, and typically, $V_{BE} \approx 0.6\text{V}$. The exponential term is, for this case, $\exp(V_{BE}/n_FV_T) \approx 10^{10}$ such that the $-1$ is quite negligible. The $-1$ is necessary for the current to go to zero for $V_{BE} = 0$. This current is due to (nnp) injection and recombination of minority-carrier electrons in the base and injection and recombination of minority-carrier holes in the emitter. Base current could also be connected to injection of holes into the n-type emitter, which recombine at the emitter-contact metal – semiconductor interface. In any event, base – emitter junction base current is predominantly from injection into the emitter, as opposed to injection into the base.

For this case of no leakage current and for $V_{BC} = 0$, the forward-active current gain (or current ratio) is defined as $\beta_{DC} \equiv \beta_F$. Using (B.6), (B.7), and (B.8) (with $-1$ neglected), this is

**Equation B.9**
and $I_{SBE} = I_s/\beta_F$. Consequently, the ideal base current is normally written as

**Equation B.10**

$$I_B = \frac{I_s e^{V_{BE}/n_F V_T}}{\beta_F} \left( 1 - \frac{V_{BC}}{V_{AF}} \right)$$

Note that the base current does not have $V_{BC}$ dependence as exhibited by the collector current. This is demonstrated to be valid in Project B.

The parameter $\beta_F$ is the SPICE transistor-model $\beta$. Implicit in the assignment of $IS$ ($I_s$) and $BF$ ($\beta_F$) in the SPICE device model is the assignment of the ideal base-current saturation $I_{SBE} = I_s/\beta_F$. That is, there is no $I_{SBE}$ (SPICE parameter) in the model. If the general active-region relation for $I_C$, (B.7), is now used in the $\beta_{DC}$ definition, we obtain the $\beta_{DC}$ relation for nonzero $V_{BC}$, namely,

**Equation B.11**

$$\beta_{DC} = \frac{I_C}{I_B} = \beta_F \left( 1 - \frac{V_{BC}}{V_{AF}} \right)$$

where $\beta_F$ is a constant (SPICE BF) and $\beta_{DC} = \beta_F$ for $V_{BC} = 0$.

In the real transistor, there is, in general, a component of leakage current. It is associated with recombination of holes and electrons in the depletion region of the base – emitter junction. In SPICE, the leakage-current component is characterized with parameters $n_E$ (base – emitter leakage coefficient) and $I_{SE}$ (base – emitter leakage saturation current). When added to the ideal component, the total base current is

**Equation B.12**

$$\beta_F = \frac{I_s e^{V_{BE}/n_F V_T}}{I_{SBE} e^{V_{BE}/n_F V_T}} = \frac{I_s}{I_{SBE}}$$
The parameter $n_E$ is ideally 2 (according to early, simplified theories), but in practice is typically about 1.5. When transistors are operated in or above the midrange of their rated current capacity, the leakage component becomes negligible.

For a small power transistor, the midrange starts at about 100 mA, such that the leakage term would be very significant at, for example, 1 mA. In the project on the transistor, which is designed to determine the SPICE parameters discussed here, a low-current range of less than about 1 mA is selected. The low current also avoids inadvertent rise in the temperature of the device during evaluation.

Similar equations that apply to the reverse-active mode can be obtained by direct substitution of the equivalent variables. The output current and input voltage, are, respectively, $I_E$ and $V_{BC}$, while, for the reverse-active mode, $V_{BE} = 0$ or negative. Based on the equivalent substitution

**Equation B.13**

$$I_E = -I_S e^{V_{BC}/n_R V_T} \left(1 - \frac{V_{BE}}{V_{AR}}\right)$$

The minus sign comes from having assigned the current direction of the emitter current out of the transistor (Fig. B.7). The parameter $I_S$ is common to (B.7) and (B.13). Equations (B.7) and (B.13) are combined to obtain the general case of $V_{BE}$ and $V_{BC}$ both positive (forward bias) in a following unit.

The reverse-operation base current is [the reverse-operation equivalent of (B.12)]

**Equation B.14**

$$I_B = I_S \left( e^{V_{BC}/n_R V_T} - 1 \right) \left( e^{V_{BC}/n_C V_T} - 1 \right) \approx I_S e^{V_{BC}/n_R V_T} + I_S e^{V_{BC}/n_C V_T}$$
where $\beta_R$ is the dc current ratio (reverse-active mode) for the case of no leakage component of base current, and is given by $\beta_R = I_E/I_B$. In practice, the reverse ideal current gain is $0.1 < \beta_R < 10$, and therefore, the reverse-operated transistor is not a useful configuration in, for example, analog amplifiers. However, the reverse-active mode equations are essential, as is shown below, for developing the general equations for the forward mode. The general form includes the possibility that the transistor will be out of the active mode.

Although $V_{AR}$ (reverse Early voltage), $I_{SC}$ (reverse leakage saturation current) and $n_c$ (base – collector leakage emission coefficient) are officially SPICE parameters, we will not be concerned with these as they would rarely be a factor in the study of analog circuits.

**B.4. Diode-Connected Transistor Circuits for Measuring Base and Collector Current**

The circuit shown in Fig. B.9 is used in the parameter-determination project for measuring the base current with the collector open. The collector is tied to the output channel voltage, which holds the collector – base junction in reverse bias, and therefore in the active mode. The configuration is effectively a diode (open collector) with two terminals, base and emitter, and the diode current is the base current. The base current is that of the active-mode transistor, because the collector – base junction is maintained in a reverse-bias state. Note that according to (B.12), base-current magnitude does not otherwise depend on the value of the base – collector voltage. This is shown to be valid in the project. (The base current is much different when the collector terminal is tied to ground and the base – collector junction is forward biased.)

*Figure B.9. Circuit for measuring base current in the open-collector diode-connected circuit.*

The measurement circuit includes a current sensing resistor, $R_B$. The relation between $I_B$ and $V_{BE}$ for this terminal configuration is (B.12), repeated here...
As noted above, the base current of (B.12) exhibits no base-collector voltage dependence other than the requirement that the transistor be in the active mode.

This is assured in this circuit since $V_{BC}$ is

**Equation B.15**

$$V_{BC} = V_B - V_C = V_{CC} - I_E R_B - V_{CC} = -I_E R_B$$

where $V_{CC} \equiv \text{Chan0\_out}$.

In the alternative diode circuit of Fig. B.10, the base and collector are connected such that $V_{BC} = 0$ and the equation for the collector current is (B.7) with $V_{BC} = 0$, or, simply,

**Equation B.16**

$$I_C = I_S e^{\frac{V_{BE}}{n_F} V_T}$$

*Figure B.10. Circuit for measuring emitter current. In this circuit, $V_{BC} = 0$ and (B.16) applies.*

The measured current in the circuit, that is, sensed by the sensing resistor, $R_E$, is the emitter current, $I_E$. This is the sum of (B.12) and (B.16), which is
We note that (B.12) remains valid for $V_{BC} = 0$. Current measurements from the two diode circuits provide, therefore, $I_C$, from $I_C = I_E - I_B$. In the parameter measurement project, it is verified that the base current is the same for both measurement circuits. This is a means by which the independence of base current on reverse voltage is demonstrated.

In the BJT parameter determination project, parameter extraction from the exponential relations is obtained from plots of current – voltage characteristics. The form of the log of the current versus voltage provides information on the two parameters of the exponential from a straight-line curve fit. For example combining the currents from the two circuits gives, as noted, $I_C = I_E - I_B$ and [from (B.16)]

**Equation B.18**

$$
\log(I_C) = \log(I_S) + V_{BE} / \ln(10) n_F V_T
$$

The zero voltage intercept thus reveals $I_S$ and the slope will show that $n_F \approx 1$.

A simple exponential represents the base current only approximately, as it is a combination of two exponentials; that is,

**Equation B.19**

$$
a_v = \frac{V_{CE}}{V_S} = \frac{V_{BE} x V_{CE}}{V_S} = \frac{R_b}{R_b + R_S} \alpha_n R_C
$$

In the measurement of the base current, using the circuit of Fig. B.9, the measured semilog plot will appear to be a straight line. This would suggest that the current – voltage relation is a simple exponential, as in the case of the collector current. However, parameters $n_{Eprime}$ and $I_{Eprime}$ vary, depending on the given narrow range of base – emitter voltage of the measurement. Note that since $n_F = 1$ and $n_E > 1$, $n_{Eprime}$ will be in the range $1 < n_{Eprime} < n_E$.

Sample measured results are shown in Fig. B.11, where the current is plotted on a log scale. For this plot, $I_C$ has been obtained from $I_C = I_E - I_B$. Both plots are straight lines,
indicating the exponential relationship between current and voltage for the two cases. Careful scrutiny of the lower curve ($I_B$) should show a slight upward curvature since it is a mixture of two exponential terms, as noted. The steeper slope for emitter current is a result of the fact that $n_F = 1$ and $n_E' > 1$.

*Figure B.11. LabVIEW plot of measured currents (mA) versus base – emitter voltage (V). The ratio of the two is the $\beta_{DC}$ of the transistor.*

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**B.5. Output Characteristics of BJT in the Common-Emitter Mode**

The common-emitter terminal configuration can be considered the fundamental building block of BJT analog amplifier circuits. The common base and common collector are applied to some extent in more special-purpose roles, such as for high output resistance (common base) and low output resistance (common collector). Therefore, a study of the transistor in the common-emitter mode is basic to a study of analog circuits.

The output characteristic of the common-emitter transistor is defined as the output current ($I_C$) as a function of the output terminal voltage ($V_{CE}$) for $I_B$ (or $V_{BE}$) held constant. It is very important to understand in the design of both analog and digital circuits. The output characteristic is experimentally explored in the project on parameter determination. The measurement circuit for obtaining the output characteristic is shown in *Fig. B.12*. This is also the circuit for measuring $\beta_{DC}$ versus $I_C$, which is discussed below.

*Figure B.12. Circuit for measuring transistor output characteristic and $\beta_{DC}$ versus $I_C$. 

---
The equations presented in Unit B.2 are in terms of terminal voltages $V_{BE}$ and $V_{BC}$. The common-emitter configuration has input voltage $V_{BE}$ but output voltage $V_{CE}$. Therefore, it is preferable to eliminate $V_{BC}$ in the equations in favor of $V_{CE}$, using $V_{BC} = V_{BE} - V_{CE}$.

When plotting the output characteristic, for example, from $0 < V_{CE} < 5 \text{ V}$, the range of $V_{BC}$ is $V_{BE} < V_{BC} < -(5 - V_{BE})$. Since $V_{BE} \approx 0.5 \text{ V}$, $V_{BC}$ covers the full range from strongly forward biased (out of the forward-active mode) to clearly reverse biased (forward-active mode). This requires that the $I_C$ [(B.7)] and $I_B$ [(B.12)] equations be modified to include all possibilities.

To obtain an equation for $I_C$ under general biasing conditions, we start with the fundamental equation of transistor action of the BJT. This is

Equation B.20

$$I_C = I_S \left( e^{V_{BE}/V_T} - e^{V_{BC}/V_T} \right) = I_E$$

This is a composite of (B.7) and (B.13) in which the base-modulation effects are neglected. Both of these equations are for $I_C$ and $I_E$ in the ideal transistor. (In this unit and beyond, we assume that $n_F = 1$.) Sometimes referred to as the linking-current equation, this is symmetrical in $I_C$ and $I_E$ and neglects all components of base current and dependence of the base width on $V_{BC}$ and $V_{BE}$.

To add an additional degree of applicability to the real transistor, base-width modulation must be added. We are interested in a relation between currents and voltages for the transistor in the forward-active mode. In this case, $V_{BE}$ is fixed at $0.4 < V_{BE} < 0.6 \text{ V}$. On this basis, base-width modulation of the emitter – base junction can be neglected. On the other hand, the relation must apply for a $V_{BC}$ range, which includes relatively large
negative values. Therefore, the effect of base-width modulation of the collector–base junction must be included in a modification of (B.20). If base-width modulation due to the dependence of base width on $V_{BC}$ is added and the substitution $V_{BC} = V_{BE} - V_{CE}$ is now made, (B.20) becomes:

**Equation B.21**

$$I_C = I_S \left( e^{V_{BE}/V_T} - e^{(V_{BE}-V_{CE})/V_T} \right) \left( 1 - \frac{V_{BE} - V_{CE}}{V_{AF}} \right)$$

The general equation must include any significant base current that contributes to collector current, that is, for when the base–collector junction becomes forward biased. For this we use (B.14) with base leakage current neglected. (Leakage current is neglected throughout this unit.) This is

**Equation B.22**

$$I_B = \frac{I_S}{\beta_R} \left( e^{(V_{BE}-V_{CE})/V_T} - 1 \right)$$

The $-1$ term has been retained in order for the equation to apply at all possible polarities and values for $V_{BC} = V_{BE} - V_{CE}$, including zero where this contribution of collector current is zero.

We note that this base current is in a loop (Fig. B.8) through the base–collector junction and is positive out of the collector terminal; $I_C$ of (B.21) is positive into the collector terminal as in Fig. B.7. Thus, the component of base current from (B.22) subtracts from the collector current to give

**Equation B.23**

$$\frac{V_{CE}}{V_s} = \frac{I_C}{I_s} \frac{R_c}{R_s + R_b} \approx \frac{I_C}{I_s} \frac{R_c}{R_s + \epsilon_n} \approx \frac{R_c}{R_s + \epsilon_n} \approx \frac{\beta_{ae} R_c}{R_s}$$

Again, for simplicity, this equation neglects the leakage current associated with the collector–base junction [$I_{SC}$ term (B.14)], which is only a fair approximation for the level of $I_C$ at which we will obtain an output characteristic in the parameter extraction project on the BJT.
A plot of this equation for $I_C$ as a function of $V_{CE}$ can be obtained for constant $V_{BE}$ or constant $I_B$. For the latter, $V_{BE}$ is also a variable such that the plot requires, in addition, a solution for $V_{BE}$ as a function of $V_{CE}$ for constant $I_B$. In the project on the output characteristic, the measured data and a SPICE solution are compared during the measurement. The input circuit provides a more or less constant $I_B$. However, the SPICE solution, which is computed by LabVIEW, is exact. It allows for a variable $I_B$ and associated variable $V_{BE}$. The SPICE solution formulation used by LabVIEW is outlined below in Unit B.7. The SPICE solution is also explored in the project Mathcad file.

After measuring the output characteristic, the segment of the resulting data array from the active region ($V_{CE} > V_{BE}$) is extracted. From these data, a straight-line curve fit is obtained by LabVIEW, which produces a number for the slope. From (B.23), we obtain an equation for the active region from letting $V_{CE} > V_{BE}$, with the result

**Equation B.24**

$$I_{C_{act}} = I_S e^{\frac{V_{BE}}{V_T} \left( 1 - \frac{V_{BE} - V_{CE}}{V_{AF}} \right)}$$

The slope for the active-region equation is $\text{slope} = \frac{dI_{C_{act}}}{dV_{CE}} = \frac{I_C}{V_{AF}}$. Thus, $V_{AF}$ can be calculated from $V_{AF} = I_C / \text{slope}$, where $I_C$ is the value taken from the data array for $V_{CE} = V_{BE}$.

For the special case of $V_{CE} = V_{BE}$, one can obtain a value for $I_S$ from the relation

**Equation B.25**

$$I_S = I_C e^{\frac{-V_{BE}}{V_T}}$$

After $V_{AF}$ and $I_S$ have been obtained, an iteration on $\beta_R$ will produce a final curve fit to the output characteristic, thereby providing a number for $\beta_R$. In this manner, all three parameters of this unit are obtained: $I_S$, $\beta_R$, and $V_{AF}$.

An example of a SPICE output characteristic (calculated in Mathcad), which uses the measured transistor-model parameters, is shown in Fig. B.13. Also shown is the calculated active-region plot.
Figure B.13. Mathcad calculated plot of the complete output characteristic, (B.23), and the active-region segment, (B.24). The saturation region [(B.34)] is graphically revealed where the plots separate.

The low-voltage region where $I_C < I_{C_{Sat}}$ is called the saturation region. The voltage and current in this region are $V_{CE_{Sat}}$ and $I_{C_{Sat}}$. In the derivation of the general equation for $I_C$, (B.23), the leakage current of the base – collector junction was neglected. If this is not valid, the reverse $\beta_R$, which is determined through curve fitting, is somewhat artificial. For example, suppose that the leakage current totally dominates the collector – base current. For this case, the general $I_C$ equation is

\begin{equation}
\beta_R = \frac{I_C}{I_{C_{leak}}}
\end{equation}

where a new definition of a sort of $\beta_R$ is defined in the relation $I_{SC} = I_C/\beta_{R_{leak}}$. A curve fit to the measured output characteristic would give $\beta_{R_{leak}}$. However, because $n_C > 1$, the result depends on the level of collector current at which the measurement is made. If, in a given measurement, the $\beta_{R_{leak}}$ is interpreted as $\beta_R$, it would function as $\beta_R$ in SPICE (when assigning BR to the model), but it would only be valid in a simulation for collector currents close to that of the measurement.

### B.6. SPICE Solution for $I_C$ versus $V_{CE}$ of the Measurement Circuit

All components of base current are those from (B.12) (forward mode) and (B.14) (reverse mode). These are summed together to obtain the following expression for the general bias case:

\begin{equation}
V_{be} = V_T \ln \left( \left| \frac{I_e}{I_C} \right| \right) \to \pm V_T \left| \frac{I_e}{I_C} \right| \left| \frac{I_C}{I_C} \right| < \lambda
\end{equation}
In the measurement circuit of the project on the output characteristic of the BJT, the circuit will provide a current source at the input and \( I_B \) (to a good approximation) will be a constant. However, in the event that a precision solution for \( I_B \) and \( V_{BE} \) is required, it can be obtained by equating (B.27) to \( I_B \) from the input circuit equation (Fig. B.12), which is

**Equation B.28**

\[
I_B = \frac{(V_{BB} - V_{BE})}{R_B}
\]

In the Mathcad project file, a solution for \( V_{BE} \) as a function of \( V_{CE} \) is obtained (using a root finder) for a given \( V_{BB} \) and \( R_B \). The result for \( V_{BE} \) (at a given \( V_{CE} \)) is used in (B.23) for a solution for \( I_C \), and hence the output characteristic is obtained. For this, the leakage components of base current are neglected.

In the LabVIEW output characteristic measurement project, a SPICE solution is obtained along with the measurement. The solution is obtained with LabVIEW using an iterative solution. The equations are (B.28) and (B.27) (without the leakage terms) solved for \( V_{BE} \). This is

**Equation B.29**

\[
V_{BE} = V_T \ln \left( \frac{\beta_P I_B}{I_S} \frac{\beta_{PE} V_{CE} / V_T}{1 + \beta_{PE} e^{-V_{CE} / V_T}} \right)
\]

The iterative method consists of guessing an initial \( V_{BE} \) and solving for \( I_B \) from (B.28). This is used in (B.29), with the given \( V_{CE} \), to obtain a better value for \( V_{BE} \). The new \( V_{BE} \) is then put back into the circuit equation, (B.28), and so on, until \( V_{BE} \) stops changing significantly. This \( V_{BE} \) is then used in (B.23) for a solution for \( I_C \) at the specified \( V_{CE} \). For the complete output characteristic, the solution is repeated in increments of \( V_{CE} \) for a
range from zero up to a specified maximum. This is accomplished in LabVIEW with a Formula Node in a While Loop. The analytical formulation is explored in the project Mathcad file.

From (B.29), we note that over the full range of $0 < V_{CE} < 5\, V$, for example, the limits of $V_{BE}$ are for $V_{CE} = 0$,

**Equation B.30**

$$V_{BE}(lo) \approx V_T \ln \left( \frac{\beta_R I_B}{I_S} \right)$$

while for large $V_{CE}$,

**Equation B.31**

$$V_{BE}(hi) = V_T \ln \left( \frac{\beta_F I_B}{I_S} \right)$$

The case of (B.30) uses $\beta_F >> \beta_R$. For example, for $\beta_F/\beta_R = 100$, the difference $V_{BE}(hi) - V_{BE}(lo) \approx V_T \ln(\beta_F/\beta_R)$, which is about 120 mV. In the base circuit equation (B.28), this change would be minor compared, for example, with a base bias voltage, $V_{BB}$, of 5 to 10 V. Thus, base current is close to a constant over the full range of $V_{CE}$, based on Chan1 out $\equiv V_{BB} = 5\, V$ or greater, as dictated by the design goal. That is, $V_{BB}$ is much greater than the change in $V_{BE}$ as $V_{CE}$ moves from (B.30) to (B.31).

We note that, consistent with the limit of (B.31), the solution for $I_B$ is from

**Equation B.32**

$$V_{BB} = V_T \ln \left( \frac{\beta_F I_B}{I_S} \right) + I_B R_B$$

Therefore, $I_B$ and $V_{BE}$ are constant and $I_C$ only varies with $V_{CE}$ due to the $V_{CE}$ dependence in (B.24). The value of the limit $V_{CE}$ is quantified in the next unit.
B.7. Collector-Emitter Voltage and Collector Current in the Saturation Region

An equation for $V_{C\text{E}_{\text{Sat}}}$ ($V_{CE}$ in the saturation region) can be obtained using the equations for $I_B$, (B.27) (with leakage components neglected), and $I_C$, (B.23), to eliminate $V_{BE}$. The approximate equation for $I_B$ is again

$$I_B = \frac{I_S}{\beta_F} e^{V_{BE}/V_T} + \frac{I_S}{\beta_R} e^{(V_{BE}-V_{CE})/V_T}$$

The equation for $I_C$, (B.23), which neglects the $V_{AF}$ term (well justified at low voltage of the saturation region), and the $-1$ is

**Equation B.33**

$$I_C = I_S \left[ e^{V_{BE}/V_T} - e^{(V_{BE}-V_{CE})/V_T} - \frac{1}{\beta_R} e^{(V_{BE}-V_{CE})/V_T} \right]$$

Eliminating $V_{BE}$ between the approximate form of (B.27) and (B.33) gives

**Equation B.34**

$$V_{C\text{E}_{\text{Sat}}} = V_T \ln \left( 1 + \frac{1}{\beta_R} + \frac{\beta_{\text{forced}}}{\beta_R} \right) \left( 1 - \frac{\beta_{\text{forced}}}{\beta_F} \right)$$

where

**Equation B.35**

$$\beta_{\text{forced}} = \frac{i_{C\text{E}_{\text{Sat}}}}{I_B} < \beta_F$$
The subscript comes from "beta forced," the conventional way to define $I_C/I_B$ in the saturation region. Note that by definition, $\beta_{\text{forced}} < \beta_F$, as $I_C < I_{\text{Cact}}$ defines the saturation region.

For example, we compute $V_{\text{CEsat}}$ at $I_{\text{Csat}} = I_C/2$. Assume that $\beta_F = 100$ and $\beta_R = 1$ such that $\beta_{\text{forced}} = \beta_F/2 = 50$. For this case, $V_{\text{CEsat}} = 120$ mV. Note that this is the midrange for the validity of (B.30).

It should be noted that $V_{\text{CEsat}}$ is not defined for $\beta_{\text{forced}} \rightarrow \beta_F$. This is because of the neglect of the $-1$ from the equations. Technically, the maximum $V_{\text{CEsat}}$ is $V_{\text{CEsat}} \approx V_{\text{BE}}$, as this is the maximum $V_{\text{CE}}$ at which the base–collector junction is forward biased, the condition for the onset of the saturation region. At $V_{\text{CE}}$ values very near $V_{\text{BE}}$, the $-1$ terms in the current equations are not mathematically negligible. On practical grounds, though, (B.34) is valid for when the output characteristic is clearly in the saturation region.

A value for $\beta_R$ can be obtained, using (B.34), from one set of data points, $I_{\text{Csat}}$ and $V_{\text{CEsat}}$ from a measurement, with $\beta_F$ known. If this proved to vary with the $I_{\text{Csat}}$ chosen for the calculation, it would suggest that the discussion at the end of Unit B.5 applies. That is, the leakage current is not negligible and the effective $\beta_R$, $\beta_{\text{Rleak}}$, is a variable throughout the saturation region.

### B.8. SPICE BJT $\beta_{\text{DC}}$ as a Function of Collector Current

SPICE calculates a dc beta, $\beta_{\text{DC}}$, when ISE and NE are included in the transistor model. The equation for the calculation uses $\beta_{\text{DC}} = I_C/I_B$, where $I_B$ (forward-active mode) includes the ideal and leakage terms, (B.12),

$$I_B = \frac{I_S}{\beta_F} e^{V_{\text{BE}}/n_F V_T} + I_S e^{V_{\text{BE}}/n_E V_T}$$

and $I_C$ is the collector current for the forward-active mode, (B.7),

$$I_C = I_S e^{V_{\text{BE}}/V_T} \left(1 - \frac{V_{\text{BC}}}{V_{\text{AF}}} \right)$$

Using (B.7) and (B.12) in the definition of $\beta_{\text{DC}}$, we obtain

Equation B.36
\[
\beta_{DC} = \frac{I_C}{I_B} = \frac{I_S e^{V_{BE}/V_T} \left(1 - \frac{V_{BC}}{V_{AF}}\right)}{I_F + I_S e^{V_{BE}/V_T} + I_S e^{V_{BE}/n_E V_T}}
\]

which is

**Equation B.37**

\[
\beta_{DC} = \frac{\beta_F \left(1 - \frac{V_{BC}}{V_{AF}}\right)}{1 + \frac{\beta_F I_S e^{V_{BE}/V_T} \left(1/n_E - 1\right)}{I_S}}
\]

The \( V_{BE} \) variable can be eliminated with

**Equation B.38**

\[
e^{V_{BE}/V_T} = \frac{I_{CO}}{I_S}
\]

giving

**Equation B.39**

\[
\beta_{DC} = \frac{\beta_F \left(1 - \frac{V_{BC}}{V_{AF}}\right)}{1 + \left(\frac{I_{CO}}{I_S}\right) \left(\frac{1}{n_E} - 1\right)}
\]

where
Equation B.40

\[ I_{CO} = \frac{I_C}{V_{BC} - V_{AF}} \]

and

Equation B.41

\[ X = \frac{\beta F I_{SE}}{I_S} \]

Note that for a given transistor, X is just a collection of parameters and the final result is a relatively simple function of \( I_C \) if the \( V_{AF} \) effect is neglected such that \( I_{CO} \approx I_C \). This is a very good approximation for the project transistors in which \( V_{AF} \) is about 200 V and the maximum \( |V_{BC}| \) is 3 or 4 V. In the project on the investigation of the \( \beta_{DC} \) dependence on \( I_C \), \( \beta_{DC} \) is specifically measured for \( V_{BC} = 0 \) (as set automatically by LabVIEW) such that the \( V_{AF} \) effect is eliminated.

The form of (B.39) indicates that \( \beta_{DC} \) is an increasing function of collector current, \( I_C \). The high-current asymptote is \( \beta_F \). The simple SPICE model treats \( \beta_{DC} \) as a constant \( \beta_F \), which therefore neglects leakage current. When parameters ISE and NE are included in the transistor model, SPICE uses (B.39) to compute \( \beta_{DC} \). Note that the circuit solution of Unit B.6 is substantially more complicated if (B.39) is included to account for the variable nature of \( \beta_{DC} \). The project Mathcad file performs this SPICE solution.

Mathcad-generated plots of collector current and the components of base current (mA) are shown in Fig. B.14. \( I_{B1}(V_{BE}) \) is the component with the same exponent as \( I_C \) (ideal transistor base current) and \( I_{B2}(V_{BE}) \) is the leakage component. That is \( ((B.12)) \)

**Figure B.14.** LabVIEW computed plots of \( I_C(mA) \) and \( I_B(mA) \) as a function of \( V_{BE}(V) \), including components \( I_{B1} \) (ideal) and \( I_{B2} \) (leakage).
The total $I_B(V_{BE})$ is seen to develop at high currents into a plot that is parallel to $I_C$.

The plot was made with numbers that are representative of the transistor of the project in which the parameters are measured. The diode-connected transistor measurements are made for the range $0.01 < I_C < 1$ mA ($-2 < \log I_C < 1$). It is apparent from the plots that the base current for these measurements is made up of a mixture of the two components, or that the base current is in the transition region between leakage-current domination and ideal-current domination.

The pure ideal base current does not develop until $I_C > 100$ mA. This mode cannot be observed experimentally (even if means to avoid heating are implemented, for example, using pulse measurements). Certain high-level effects, which have not been included in the discussion, would come into play at this level, rendering the theories presented here as marginally valid.

An experimental plot of $I_C/I_B = \beta_{DC}$ as a function of $I_C$ is shown in Fig. B.15. A curve fit to the data yields $n_E$, $I_{SE}$, and $\beta_F(104)$. We note that the maximum $\beta_{DC} \ll \beta_F$.

Figure B.15. LabVIEW measurement of ratio $I_C/I_B = \beta_{DC}$ as a function of $I_C$. 
B.9. Signal or Incremental Common-Emitter Current Gain

Since $\beta_{\text{DC}}/I_B$ is a variable function of $I_C$, the incremental $\beta_{\text{ac}}$ is, in general, different from the dc $\beta_{\text{DC}}$. (The incremental $\beta_{\text{ac}}$ is often referred to as $\beta_o$, but $\beta_{\text{ac}}$ is consistent with SPICE.) To get an approximate value, we could calculate $\beta_{\text{ac}}$ from

**Equation B.42**

$$\beta_{\text{ac}} = \frac{I_C}{I_b} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}} = \frac{I_{C2} - I_{C1}}{\beta_{\text{DC2}} - \beta_{\text{DC1}}}$$

with $I_{C1} = I_{C2}$ and where (B.39) is used to obtain $\beta_{\text{DC}}$ at the two currents. The definition of $\beta_{\text{ac}}$ is from the limiting case of $I_{C2} \rightarrow I_{C1}$, that is,

**Equation B.43**

$$\beta_{\text{ac}} = \frac{dI_C}{d\left(\frac{I_C}{\beta_{\text{DC}}}\right)}$$

Performing this operation with the use of (B.39) leads to

**Equation B.44**

$$\beta_{\text{ac}} = \frac{\beta_{\text{F}} \left(1 - \frac{V_{BE}}{V_{AF}}\right)}{1 + \frac{\chi \left(I_{C0} \frac{1}{I_S} \right)}{n_E}}$$
The result indicates that $\beta_{ac} > \beta_{DC}$ ($n_E > 1$) and that the two converge in the limit for high $I_C$. This is the expression used in SPICE for the incremental $\beta_{ac}$, and it is used by SPICE when $NE$ and $ISE$ are included in the model. Otherwise, SPICE uses $\beta_{ac} = \beta_{DC} = \beta_F$. (If IS and BF are not specified in the model, SPICE will use default values, typically, BF = 100 and IS = $10^{-16}$ A. For the project transistors, IS is about $10^{-13}$ A.)

### B.10. Summary of Equations

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta_{DC} = \frac{I_C}{I_B}$</td>
<td>Common-emitter dc current gain.</td>
</tr>
<tr>
<td>$I_C = I_S e^{V_{BE}/n_F V_T} \left(1 - \frac{V_{BC}}{V_{AF}}\right)$</td>
<td>Forward active-mode output characteristic relation.</td>
</tr>
<tr>
<td>$I_B = \frac{I_S}{\beta_F} \left(e^{V_{BE}/n_F V_T} - 1\right) + I_{SE} e^{V_{BE}/n_E V_T} \left(1 - \frac{V_{BE}}{V_{AF}}\right)$</td>
<td>Forward base current.</td>
</tr>
<tr>
<td>$I_B = \frac{I_S}{\beta_R} \left(e^{V_{BC}/n_R V_T} - 1\right) + I_{SC} e^{V_{BC}/n_C V_T} \left(1 - \frac{V_{BC}}{V_{AF}}\right)$</td>
<td>Reverse base current.</td>
</tr>
<tr>
<td>$I_C = I_S \left[e^{V_{BE}/V_T} - e^{V_{BE} - V_C E / V_T} \left(1 - \frac{V_{BE} - V_{CE}}{V_{AF}}\right) - \frac{1}{\beta_R} \left(e^{V_{BE} - V_{CE}} - V_T\right)\right] $</td>
<td>Output characteristic relation.</td>
</tr>
<tr>
<td>$V_{CE\text{sat}} = V_T \ln \left(1 + \frac{\frac{1}{\beta_R} + \frac{\beta_{\text{forced}}}{\beta_F}}{1 - \frac{\beta_{\text{forced}}}{\beta_F}}\right)$</td>
<td>Collector-emitter voltage in saturation region.</td>
</tr>
<tr>
<td>$\beta_{DC} = \frac{\beta_F \left(1 - \frac{V_{EC}}{V_{AF}}\right)}{1 + \left(\frac{I_C}{I_S}\right) \left(\frac{1}{n_E}\right)^{-1}}$</td>
<td>Collector-current dependence of dc common-emitter current gain.</td>
</tr>
<tr>
<td>$\beta_{ac} = \frac{\beta_F \left(1 - \frac{V_{BC}}{V_{AF}}\right)}{1 + \frac{\chi}{n_E} \left(\frac{I_C}{I_S}\right) \left(\frac{1}{n_E}\right)^{-1}}$</td>
<td>Collector-current dependence of incremental (ac) common-emitter current gain.</td>
</tr>
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B.11. Exercises and Projects

Project Mathcad

Files

Laboratory Project

PB.3

Characterization of the Bipolar Junction Transistor for Circuit Simulation

PB.4

Diode-Connected Transistor Measurements

PB.5

Measurement of $\beta_{DC}$ versus the Collector Current

PB.6

BJT Output Characteristic Measurement

Simulation of the Output Characteristic Measurement

Unit C. Common-Emitter Amplifier Stage

Analog amplifier stages (BJT) generally comprise three possible terminal configurations: common emitter, common base, and common collector (emitter follower). As the names suggest, in each case, the input and output are referred to the common terminal. The MOSFET equivalents are common source, common gate, and common drain (source follower), respectively.

As the most fundamental of transistor amplifier building blocks, the common-emitter stage is the logical configuration to begin a study of signal amplifiers. The common-emitter considered initially in this unit is obtainable with a simple extension of the dc measurement circuit from Unit B (Fig. B.12). Based on this circuit various aspects germane to signal amplifiers in general are discussed. In Unit C.7, the common-emitter stage with active load is explored. Both types of amplifiers, with resistive and active loads, are investigated extensively in projects.

The emitter-follower stage is discussed in Unit C.9 along with a general treatment of the various effects on the common-emitter stage with an emitter-branch resistor. An entire unit (Unit C.7) is devoted to the source-follower stage, the MOSFET equivalent of the emitter-follower stage. The common-gate stage, the MOSFET equivalent of the BJT common-base stage, is considered extensively in conjunction with the role it plays in the differential amplifier stage (Unit 8).

C.1. DC (Bias) Analysis

The two common-emitter amplifier-stage configurations studied in projects are shown in Fig. C.1. We note that the dc circuit of Fig. C.1(a) is that of Fig. B.12. Amplifier performance analysis can be performed with the two output channels available from the DAQ in the following manner: Fig. C.1(a) uses separate channels for the input and output bias circuits and superimposes the input signal on the input bias. In Fig. C.1(b) we add a signal-source resistor and coupling capacitor and use one channel for the input signal and one channel for bias. The capacitor is required to prevent the connection of the signal
source from affecting the dc (bias) operation of the circuit. The latter represents the classical practical common-emitter amplifier stage. The signal-source resistor provides for a current-source input signal and hence linear amplification.

**Figure C.1.** (a) Base current bias (dc) and input signal applied to the same node. Collector circuit has a separate power supply. (b) Amplifier with signal coupling capacitor and single power supply for bias.

In the experimental project on the common-emitter amplifiers, we measure the voltage gain as a function of the collector current and compare the results with SPICE. The bias collector current is swept from 0.1 to 1 mA. The measurement uses the circuit in Fig. C.1(a). A DAQ output channel (V_{BB}) sets the bias currents. Another output channel (V_{CC}) sets the design bias V_{CE} at each bias current. The gain of the circuit of Fig. C.1(b) is also measured with particular emphasis on the bias solution and the frequency response.

### C.1.1. DC (bias) Formulation

A formulation for obtaining the collector current for a given V_{BB} [Fig. C.1(a)] is based on the following: From the input loop equation,

**Equation C.1**

\[ I_B = \frac{V_{BB} - V_{BE}}{R_B} \]

The two relevant transistor characterization equations are (B.6),

\[ I_C = \beta_{DC} I_B \]
and base–emitter dc voltage equation, from (B.7), setting $V_{BC} = 0$ for simplicity,

**Equation C.2**

$$V_{BE} \approx V_T \ln \left( \frac{I_C}{I_S} \right)$$

The equation set above has three unknowns, $I_C$, $I_B$, and $V_{BE}$. The equations can be combined to obtain a function for $I_C$,

**Equation C.3**

$$I_C = \frac{V_{BB} - V_T \ln \left( \frac{I_C}{I_S} \right)}{R_B} \beta_{DC}$$

A good estimate can be obtained with using $V_{BE} \approx 0.6$ V, giving simply

**Equation C.4**

$$I_C = \frac{V_{BB} - 0.5V}{R_B} \beta_{DC}$$

The simple expression is sufficient, for example, for selecting a value for $R_B$ in the circuit of Fig. C.1(a) in the BJT amplifier project. We have also neglected the dependence of $\beta_{DC}$ on $V_{BC}$ of (B.11). This is a reasonable approximation for establishing the nominal values for the measurement circuit components.

The collector–emitter voltage, $V_{CE}$, is then established with

**Equation C.5**

$$V_{CE} = V_{CC} - I_C R_C$$

In designing a project circuit for a current sweep, $R_B$ and $R_C$ are selected for the highest currents and highest DAQ output voltage. In the amplifier project, the circuit of Fig. C.1(b) uses the resistors from the circuit of Fig. C.1(a). It thus has a unique bias variable
and \( V_{CC} \) solution for a given design \( V_{CE} \) requirement. This is based on (C.3) and (C.5) and is

\[
\frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE}}{R_B} \beta_{DC}
\]

In the amplifier project, the project Mathcad file is used to find the solution for \( V_{CC} \) [with an educated guess for \( V_{BE} \), as in (C.4)]. If the result has \( V_{CC} > 10 \) V, the limit from the DAQ, it is necessary to decrease \( R_C \) or increase \( R_B \). This may be necessary, as the transistor \( \beta_{DC} \) is not known with precision at the point of the selection of the resistor values. After measuring the actual \( V_{CC} \), the result is used in the Mathcad file to compute a value for \( \beta_{DC} \) from a circuit solution.

### C.2. Linear or Signal Model for the BJT

The primary function of a transistor in analog circuits is to produce a signal output current in response to a signal input voltage. In the case of the common-emitter circuits of Fig. C.1, the transistor input voltage is \( V_{be} \) and the responding output current is the collector current \( I_c \). (Variable subscript conventions are covered in Unit 2. Uppercase symbols with lowercase subscripts denote RMS or peak magnitude of periodic signals.) The linear relation between the two variables is the transconductance, \( g_m \). By definition, for the BJT

\[
I_c = g_m V_{be}
\]

In some simple amplifier circuits, this would be all that would have to be known about the transistor to perform a design or analysis. More generally, however, the model also includes input and output resistances, \( r_i = r_b + r_\pi \) and \( r_o \), respectively. The transistor linear model, which includes these components and a load resistor (in this case, bias resistor, \( R_C \)), is shown in Fig. C.2. Applied input voltage \( V_{be} \) and responding \( I_c \) are indicated.

**Figure C.2. Linear signal model for the BJT. Model parameters are \( r_b \), \( r_\pi \), \( g_m \), and \( r_o \). Added to the model are circuit components \( R_C \) and applied voltage \( V_{be} \).**
The input resistance relates the input signal base current $I_b$ to the signal emitter – base voltage, $V_{be}$, that is

**Equation C.8**

$$I_b = \frac{V_{be}}{r_b + r_x}$$

Parameter $r_b$ is the actual physical resistance through which the base current must flow to arrive at the true, internal physical base – emitter junction. The signal voltage across the internal base – emitter junction is $V'_{be}$. Parameter $r_x$ is the linear relation between $I_b$ and $V'_{be}$ and is not a physical resistance.

We assume in the following discussion that $r_x >> r_b$. This is especially true in the low current range of our BJT transistor projects. As will be seen below, $r_x$ is inversely proportional to bias collector current, $I_c$, whereas $r_b$ is close to a constant and could be significant at currents corresponding to midrange or higher for the transistor. (As a rule, $r_b$ must be taken into consideration when the model is applied in very high frequency applications.) Note that neglecting $r_b$ compared to $r_x$ is equivalent to $V'_{be} \approx V_{be}$, as assumed below.

The output-resistance parameter, $r_o$, accounts for the fact that total collector current, $i_C$, increases with increasing total collector – emitter voltage, $V_{CE}$. According to the output resistance parameter relationship, the current through this resistance is

**Equation C.9**

$$I_o = \frac{V_{ce}}{r_o}$$
Including $r_o$, the current through the load, in this case bias resistor, $R_C$, is

**Equation C.10**

$$I_C = g_m V_{be} + \frac{V_{ce}}{r_o} \approx g_m V_{be} + \frac{V_{ce}}{r_o}$$

This current flows up through $R_C$ such that $V_{ce}$ is negative for positive $V_{be}$. Thus, the current associated with $r_o$ subtracts from $g_m V_{be}$ to reduce the current through $R_C$. For a positive $V_{be}$, there is an increase in the total $v_{BE}$, thus causing the total collector current to increase. The result is a decrease in the total $v_{CE}$ and hence a negative incremental $V_{ce}$.

The two components of (C.10) are illustrated graphically in Fig. C.3. The output characteristics are for two values of base – emitter voltage: bias only, $V_{BE}$, and bias plus base – emitter signal voltage, $V_{BE} + V_{be}$. They are designated Bias and Signal. The solution to $i_C$ and $v_{CE}$ is constrained to the "load line," which is $i_{RC} = i_C = V_{CC}/R_C - v_{CE}/R_C$ [(C.5)].

**Figure C.3. Transistor output characteristic with no signal and signal. Also plotted is the $R_C$ load line. The solution for $i_C$ and $v_{CE}$ is always the intersection.**

At a constant $v_{CE} = V_{CE}$, the change in the current-source current for the applied $V_{be}$ is $g_m V_{be}$ [(C.7)]. The net collector current change (signal current), $I_n$, though, is as given by (C.10); that is, it includes the component associated with $r_o$. Since the output characteristic slopes downward for decreasing $v_{CE}$, the actual transconductance decreases, but the linear model treats this effect with a constant $g_m$ combined with the effect of the output resistance, $r_o$. 
C.2.1. Determination of the Linear Model Parameters

We can relate the values of the two parameters in (C.10) to the SPICE model parameters using (B.7) with the substitution \( v_{BC} = -(v_{CE} - v_{BE}) \). This is

Equation C.11

\[
i_C = I_S e^{V_{BE}/V_T} \left( 1 + \frac{v_{CE} - v_{BE}}{V_{AF}} \right)
\]

Differentiating (C.11) with respect to \( v_{BE} \) (with \( v_{CE} = V_{CE}, V_{cc} = 0 \)), \( g_m \) is found to be

Equation C.12

\[
g_m = \frac{\partial i_C}{\partial v_{BE}} = \frac{\partial \left[ I_S e^{V_{BE}/V_T} \left( 1 + \frac{v_{CE} - v_{BE}}{V_{AF}} \right) \right]}{\partial v_{BE}} \approx \frac{I_C}{V_T}
\]

The approximate form only ignores a term on the order of \( I_C/V_{AF} \), where \( V_{AF} \gg V_T \).

The output resistance is obtained with \( v_{BE} = V_{BE} \) (bias value) or \( V_{be} = 0 \). This is

Equation C.13

\[
1/r_o = \frac{\partial i_C}{\partial v_{CE}} = \frac{I_C(v_{CE} = V_{BE})}{V_{AF}}
\]

where, from (C.11), \( I_C(v_{CE} = V_{BE}) = I_S e^{(V_{BE}/V_T)} \). For simplicity, the bias collector current, from (C.11), \( I_C = i_C(V_{CE}) \), is usually used for the calculation for \( r_o \). Finally, a relation for \( r_t \) comes directly from (C.7), \( I_c = g_m V_{bc} \), and (B.41), \( I_c = \beta_{ac} I_b \). Equating the two gives

Equation C.14

\[
g_m V_{be} = \beta_{ac} I_b
\]
Hence, from the definition \( r_n = V_{be}/I_b \) (with \( V_{be} \approx V_{be} \))

Equation C.15

\[
r^*_n = \frac{\beta_{ac}}{g_m} = \frac{\beta_{ac} V_r}{I_c}
\]

Note that the right-hand side of (C.14) is the alternative current-dependent current source of the linear model of Fig. C.2.

As discussed in Unit B.9, \( \beta_{ac} \) can be slightly different from \( \beta_{DC} \), but the distinction usually need not be made in analysis or design. This is due to the fact that \( \beta_{DC} \) tends to be quite variable among devices and that most analog designs are based on making the results as independent of \( \beta_{DC} \) as possible. Signal parameter \( \beta_{ac} \) will be used in the following, but it is understood that \( \beta_{DC} \) can be used in the calculations without serious penalty in precision.

C.3. Amplifier Voltage Gain

Any transistor amplifier stage has a gain from the input terminal to its output terminal (base and collector, respectively, for this case). But the circuit gain, from the source to the output, takes into consideration the possible finite input resistance at the transistor input terminal. Due to the finite signal-source resistance, an attenuation results from the signal-source to the transistor input terminal. The example of this case of the common-emitter amplifier stage is considered here.

C.3.1. Gain from Base of Transistor to Output at Collector

The midband (frequency-independent) signal version of the circuit of Fig. C.1(b) is shown in Fig. C.4. It is obtained from the general circuit by converting dc voltages to zero. This includes the capacitor voltage, which ideally, remains at its constant dc (bias) value. The rule followed here is that if there is no incremental variation between any two nodes with a signal applied at the input, then the component between the two nodes is superfluous. In Fig. C.4, the output voltage is \( V_o = V_{cc} \) and the signal source is designated \( V_s \) along with its source resistance, \( R_s \). In the case of an actual signal source, \( R_s \) is probably an equivalent rather than an actual resistor. Thus, it is assigned a lowercase subscript.

**Figure C.4. Signal equivalent circuit for the amplifier. dc nodes have been grounded and the capacitor has been shorted.**
Neglecting the output resistance, the signal collector current for a signal voltage applied at the base reverts to (C.7), which is

$$I_c = g_m V_{be} = \frac{I_C}{V_T} V_{be}$$

with $g_m = I_C/V_T$ [(C.12)]. $I_C$ is the bias current with uppercase subscript, not the signal, with lowercase subscript. (Recall that signal voltage and currents can be, for example, periodic peak or RMS values or instantaneous values, as these are all proportional throughout the linear circuit. To be specific, as in the experiment on the common-emitter amplifier, we consider them to be periodic-signal peak values.)

The signal voltage developed at the collector is (still assuming that $r_o \gg R_C$)

**Equation C.16**

$$V_o = V_{CE} = -I_CR_C$$

From (C.16) and (C.7), the gain of the transistor in the circuit (input at the base of the transistor and output at the collector) is

**Equation C.17**

$$a_{vb} = \frac{V_o}{V_{be}} = -g_m R_C = -\frac{I_C}{V_T} R_C$$

We note that the magnitude of the result is the dc voltage drop across the bias resistor divided by $V_T$. For example, for $V_{Re} = 5$ V and $V_T = 26$ mV (room temperature), the gain
magnitude is about 200. The BJT circuit is capable of providing very substantial voltage gains.

**C.3.2. Overall Gain Magnitude from Signal Source Voltage to Output**

The circuit input resistance looking into the base of the transistor, $R_b$, is the transistor input resistance, $r_\pi$ (still neglecting $r_b$), in parallel with the bias resistor $R_B$, that is,

**Equation C.18**

$$ R_b = \frac{r_\pi R_B}{r_\pi + R_B} $$

The gain from the signal source to the output at the collector of the transistor is thus

**Equation C.19**

$$ a_v = \frac{v_{ce}}{v_s} = \frac{v_{be}}{v_s} \frac{v_{ce}}{v_{be}} = -\frac{R_B}{R_b + R_s} g_m R_C $$

When the input-signal source resistance is large ($R_s \gg R_b$), a good approximation for $a_v$ is

**Equation C.20**

$$ a_v \approx -\frac{R_b}{R_s} g_m R_C $$

Further approximation can be made using $R_B \gg r_\pi$, to obtain

**Equation C.21**

$$ a_v = -\frac{r_\pi}{R_s} g_m R_C $$

Finally, using $\beta_{ac} = g_m r_\pi$ [(C.15)],
Equation C.22

\[ a_v = -\beta_{ac} \frac{R_C}{R_s} \]

This result is intuitive on the basis of \( I_b \approx I_s \), \( I_s \approx V_s/R_s \), and \( I_c = \beta_{ac} I_b \). The sequence of approximations for the gain magnitude is

Equation C.23

\[ |\beta_v| = \frac{V_{ce}}{V_s} = \frac{I_c}{I_s} \frac{R_C}{R_s} + R_b \approx \frac{\beta_{ac} R_C}{R_s} + r_s \approx \frac{\beta_{ac} R_C}{R_s} \]

An additional approximation is with \( \beta_{ac} \approx \beta_{DC} \).

Note that the requirement for the voltage gain to be greater than unity is that \( R_s < \beta_{ac} R_C \). Thus, for sources with a large \( R_s \), an amplifier design should have a high input resistance stage such as an emitter-follower stage. The emitter-follower stage is discussed in Unit C.9.

In the Project C1 the gain of the amplifier as a function of bias current, \( I_C \), is measured using the circuit of Fig. C.1(a). This is made possible with the use of LabVIEW and the DAQ, with two output channels, to provide a signal source superimposed on the input bias voltage. In this case, the overall gain from the signal source is restricted (input bias and signal source resistor are the same) and \( a_v \approx -\beta_{ac} R_C/R_B \). Since \( R_B \) of the circuit is roughly \( \beta_{DC} R_C \), the gain is on the order of unity.

C.4. Accuracy of Transistor Gain Measurements

We want now to consider the measurement of the gain of the transistor amplifier (Fig. C.1) based on the linear model. This model is not valid if the signals are too large, such as to cause an unacceptable degree of nonlinearity. If the linear model is valid, the signal input voltage magnitude, between the base and emitter of the transistor, is related to the fraction \( I_c/I_C \) according to [combining (C.7) and (C.12)]

Equation C.24

\[ V_{be} = \frac{I_c}{I_C} V_T \]
This voltage must be large enough for a good measurement using the DAQ board in the computer (i.e., at least a few millivolts), yet small enough so as not to cause substantial nonlinearity, which would invalidate the measurement of signal gain. Again, the signal-gain concept is based on the linear model. In the following, we will find the conditions under which the linear model is valid and to what extent.

The general expression (active region) between total collector current and total base–emitter voltage, $v_{BE} = V_{BE} + V_{be}$, is (neglecting the $V_{AF}$ factor) [from (B.7)]

**Equation C.25**

$$i_C = I_S e^{v_{BE}/V_T} e^{v_{be}/V_T} = I_C e^{v_{be}/V_T} = I_C + I_C$$

or

**Equation C.26**

$$v_{be} = V_T \ln\left(1 \pm \frac{I_C}{I_C}\right) \rightarrow \pm V_T \frac{I_C}{I_C} \quad |I_C| \ll 1$$

where the limit form for $|I_C/|I_C| \ll 1$ gives (C.24). The plus sign is for $I_C$ and $V_{be}$ positive, and vice versa.

Since the signal output voltage is $V_o = -I_C R_C$, the signal "gain" is

**Equation C.27**

$$a_v = \frac{V_o}{v_{be}} = -\frac{I_C R_C}{V_T \ln\left(1 \pm \frac{I_C}{I_C}\right)} = -g_m R_C \frac{I_C}{I_C}$$

which reduces to the linear form, (C.17), when $|I_C/|I_C| \ll 1$.

In the amplifier project, the gain is obtained by dividing the measured signal $V_o$ by the measured signal $V_{be}$. The circuit has $R_s (=R_B) >> r_\pi$, such that $I_C \approx \beta_{ac} V_S / R_s$ [as in (C.23)]. As a result, for the positive and negative peaks of $V_s$, the positive and negative peak
magnitudes of $I_c$ are equal. Thus, the fraction $|I_c/I_C|$ is the same for both signal polarities. Incremental voltage $V_{be}$ will respond nonsymmetrically according to (C.26). We note that this does not constitute a form of distortion at the output, as is evident from the approximate form of (C.23) (neglecting a very small effect due to variation of $\beta_{ac}$).

For output currents on the order of, for example, $|I_c/I_C| = 0.5$, the plus and minus peak values of $V_{be}$ are significantly different. In the amplifier-gain measurement project, the ac voltmeter indicates a peak voltage, which is the average of the plus and minus peak values. To some extent, in this manner, the error is canceled. A comparison is made of the average value of the peaks, $V_{be_{avg}}$, with the distortion-free $V_{be}$, as shown in Fig. C.5.

Figure C.5. Plot of calculated measured $V_{be_{avg}}$ as a function of $frac = I_c/I_C$ and distortion-free $V_{be}$. The measured value exhibits a 10% error at $|I_c/I_C| = 0.5$ and $V_{be} = 12.9 \text{ mV}$ and $V_{be_{avg}} = 14.2 \text{ mV}$.

In the amplifier project, the measurement base – emitter voltage is limited to about $|I_c/I_C| = 0.2$. This corresponds to $V_{be} \approx 5 \text{ mV}$. The measurement error, due to the distortion discussed here, is only about 1% for this case.

The measurement circuit is configured to be able to measure the signal voltage with the dc base – emitter voltage removed. Therefore, the DAQ conversion limit can be set at the minimum of 50 mV, where the resolution is much less than $V_{be} \approx 5 \text{ mV}$.

As noted, a possible nonlinearity in $\beta_{ac}$ could be a contributor to nonlinearity in the gain function (C.22). The effect from including the $\beta_{ac}$ nonlinearity in the development of (C.27) is also, to a degree, canceled in the averaging process of measuring the gain.

C.5. Effect of Finite Slope of the Transistor Output Characteristic

As discussed in Unit C.2, the signal model contains an output resistance, which reflects the fact that the output characteristic of the transistor has a finite slope. This is characterized with the SPICE parameter VAF. It was noted that the effect of the finite
slope is to place a resistance effectively across the output of the amplifier. It is calculated from \( r_o = V_{AF}/I_C \), (C.13).

With increasing bias current, \( r_o \) may not be negligible compared to \( R_C \). In the project on the gain of the amplifier, we will read the experimental data into a Mathcad file and adjust \( V_{AF} \) to make the SPICE calculation and measured data match. The gain expression that includes transistor output resistance is

**Equation C.28**

\[
a_{vb} = -g_m \frac{R_o}{R_C} = -g_m \frac{R_C}{1 + \frac{I_C}{V_{AF}} R_C}
\]

In a representative transistor, \( V_{AF} \approx 100 \). The circuit design could call for \( I_C R_C \approx 5 \) V for a 10-V supply voltage. In this case, the output resistance has about a 5% effect on the gain value.

**C.6. Selection of Coupling Capacitors**

External capacitors are added to the circuits of this unit for two purposes. One, shown in Fig. C.1(b), is to connect the signal input source to the amplifier. The other is a special-purpose capacitor of the amplifier project. It is attached to facilitate measurement of the base–emitter voltage with high resolution. Design considerations for selection of the capacitor values are discussed in the following.

**C.6.1. Coupling Capacitor for the Common-Emitter Amplifier**

The linear equivalent circuit of the amplifier of Fig. C.1(b) is shown in Fig. C.6. The selection of the value of the capacitor \( C_b \) is based on the requirement that it has negligible effect on the signal current at any frequency at which the amplifier will be operated. Including the reactance of the capacitor, the input signal current is

**Equation C.29**

\[
I_z(f) = \frac{V_z}{R_z + \frac{1}{j2\pi f C_c} + R_b} = \frac{V_z}{R_z + R_b} \cdot \frac{1}{1 + \frac{1}{j2\pi f (R_z + R_b) C_c}}
\]

*Figure C.6. Signal model of the circuit for the determination the characteristic frequency of the frequency response associated with the coupling capacitor.*
The input signal current magnitude is

**Equation C.30**

\[ |I_s(f)| = \frac{V_s}{R_s + R_b} \cdot \frac{1}{\sqrt{1 + \left(\frac{f}{f_b}\right)^2}} \]

where

**Equation C.31**

\[ f_b = \frac{1}{2\pi(R_s + R_b)C_b} \]

Frequency \( f_{3dB} \) is defined as the frequency where the response magnitude is

**Equation C.32**

\[ |I_s(f_{3dB})| = \frac{V_s}{R_s + R_b} \cdot \frac{1}{\sqrt{2}} \]

It follows that for this case, \( f_{3dB} = f_b \). Note that at \( f = 10f_{3dB} \),

\[ |I_s(10f_{3dB})| = \frac{V_s}{R_s + R_b} \cdot 0.995 \]
C.6.2. Coupling Capacitor for Measuring the Base Input Voltage

In Project C1 measurement of the base input voltage is made at the signal side of the coupling capacitor. This is the node designated by $V_x$ in Fig. C.6. Good measurement precision is provided, as the dc component of the base voltage is blocked by the coupling capacitor. The maximum voltage sensed by the input channel is only the signal voltage $V_b \approx V_x \approx 5$ mV, as discussed in Unit C.4. This value is much smaller than dc $V_{BE} \approx 0.5$ V. In this configuration, the limit setting for the input channel is set at 0.1 V, for a resolution of about 48 $\mu$V with the input channel in the bipolar mode. If the peak signal voltage is, for example 5 mV, the resolution is about 1% of the measured voltage.

The required capacitor, $C_b$, for this case and for same $f_{3dB}$, is substantially larger than that obtained from (C.31). As will be shown, at $f \approx f_{3dB}$, the requirement is that $|X_{Cb}| \approx \pi$. It follows that at $f$ near $f_{3dB}$, $R_s >> |X_{Cb}|$ since $R_s >> R_b \approx \pi$. The input signal current is thus given approximately by

**Equation C.33**

$$I_s = \frac{V_x}{R_s + R_b + |X_{Cb}|} \approx \frac{V_x}{R_s}$$

This includes the good assumption that $R_s >> R_b$ and that, by design, $|X_{Cb}| \approx R_b$ for $f \approx f_{3dB}$. (Technically, the pole of the transfer function is ignored.)

The signal voltage, $V_x(f)$, at the input signal source side of the capacitor is the sum of the voltage at the base plus the voltage across the capacitor, that is, with (C.33),

**Equation C.34**

$$V_x(f) = I_s \frac{1}{\pi \omega C_b} + I_s R_b$$

The ratio $V_x(f)/V_b$ is thus

**Equation C.35**

$$\frac{V_x(f)}{V_b} = \frac{I_s \frac{1}{\pi \omega C_b} + 1}{I_s R_b}$$
Note that the form of $V_x(f)$ is falling, for increasing frequencies, to a plateau ($V_b$). We will define $f_{3\text{dB}}$ as the frequency where the magnitude of this ratio is $\sqrt{2}$. This could qualify as a type of corner frequency, as it represents the frequency where the frequency response function is $\sqrt{2}$ times the asymptotic value. A solution for $f_{3\text{dB}}$ then comes from

**Equation C.36**

$$\sqrt{1 + \left(\frac{1}{2\pi f_{3\text{dB}} R_b C_b}\right)^2} = \sqrt{2}$$

giving

**Equation C.37**

$$f_{3\text{dB}} = \frac{1}{2\pi R_b C_b} = \frac{1}{2\pi r \pi C_b}$$

At $f=10f_{3\text{dB}}$, $V_x = 1.005V_b$. Note that for this case of a current source [(C.33)], the value of the capacitor can be obtained simply to satisfy $|X_{cb}| = r_\pi$.

### C.6.3. Coupling Capacitor for the Base Voltage Measurement of the DC Sweep Circuit

The project circuit for making a precision measurement of the gain of the amplifier of Fig. C.1(a) is shown in Fig. C.7. The circuit has the addition of $C_b$ and $R_s$ for measuring the base signal voltage without the dc component. The selection of $R_s$ in the amplifier project is made to satisfy if $R_s \gg r_\pi$ such that the effect on the gain referred to $V_s$ is small. The choice is, on the other side, $R_s < R_B$, such that the charging time of $C_b$ is not prohibitively long during the bias sweeps. The $f_{3\text{dB}}$ frequency at $V_x$ for this case is (C.31) with $f_b = f_{3\text{dB}}$. In the amplifier project, the capacitor is selected from (C.37) to satisfy the requirement for the amplifier of Fig. C.1(b) using (C.37). The capacitor will thus certainly be adequate for the amplifier of Figs. C.1(a) and C.7.

**Figure C.7. Common-emitter amplifier for measuring the amplifier gain as a function of bias current. The signal base – emitter voltage is measured at $V_x$.**
C.7. Common-Emitter Amplifier with Active Load

In the early days of electronic amplifiers, the voltage amplification device was, of course, the vacuum tube. It existed in only one polarity configuration, that is, with positive plate (bus or rail) voltage. With the appearance of semiconductor transistors came the availability of the dual set of devices with opposite terminal voltage polarities. This is the case for BJTs, JFETs, and MOSFETs. (Vacuum tubes were implemented in class B amplifiers. The application required a pair of inputs, one 180° out of phase with the other, normally derived from a transformer.)

The dual set has provided the versatility for a wide range of electronic system applications, including the amplifier with active load shown in Fig. C.8. This can be compared with the circuit of Fig. C.1, which in place of the pnp transistor, has a bias collector resistor, $R_C$.

Figure C.8. Common-emitter amplifier with active (transistor) load. The npn is the driver transistor and the pnp is the load transistor. The input signal source could be moved to the base of the pnp, in which case the two transistors play opposite rolls.
Note that either transistor base could serve as the input such that the opposite transistor becomes the load. In Fig. C.8, the npn is chosen as the driver transistor and the pnp as the load transistor.

A dc output characteristic plot is shown in Fig. C.9. Since the collector current of the individual transistors is the same, the solution to bias voltage $V_{CE}$ for the npn is the intersection of the two curves, that is, 5 V. This would be a good choice for a bias output voltage for the power supply voltage of this case, which is 10 V. For the plots, $V_{AFn} = 100$ V and $V_{AFp} = 20$ V were used. (In the discussion of the npn – pnp amplifier, the added subscript n or p will denote npn or pnp, respectively.)

**Figure C.9. Output characteristics for the npn and pnp transistors.** The pnp emitter – collector voltage is $v_{EC} = V_{CC} - v_{CE}$, where $v_{CE}$ is the collector – emitter voltage of the npn. The bias variables $V_{CE}$, $V_{EC}$, and $I_C$ are at the intersection of the two plots.

A signal impressed at the base of the npn causes the npn curve to move up or down while the pnp curve remains in place. Note that the pnp acts like a load line of a resistive load; however, an extension of the active-region characteristic of the pnp intersects the zero-current axis at $V_{CC} + V_{AFp} = 30$ V. The pnp active-load transistor thus provides the equivalent of a bias resistor with a power supply of 30 V instead of the actual 10 V.

**C.7.1. Gain of the NPN – PNP Common-Emitter Amplifier with Active Load**

The gain benefit for the case of the active load is apparent from the following. The equation for the gain of the BJT common-emitter amplifier with resistor $R_C$, which includes the output resistance of the driver transistor (in this case, npn), is a form of (C.28)

**Equation C.38**
\[ a_{vb} = -g_m \frac{R_C r_{on}}{R_C + r_{on}} \]

where \( r_{on} \) is the output resistance of the npn and is given by [generalization of (C.13)]

**Equation C.39**

\[ r_{on} = \frac{V_{AFn} + V_{CE} - V_{BE}}{I_C(V_{CE})} \]

where \( V_{CE} \) and \( V_{BE} \) are the transistor bias voltage variables and \( I_C \) is the collect bias current of the amplifier. Parameters \( V_{AFn} \) and \( V_{Afp} \) are used in this unit for the slope parameter for the npn and pnp, respectively.

The output resistance expression is generalized here to emphasize that strictly speaking, the collector currents and voltages must match as suggested in the expression. Voltages \( V_{BE} \) and \( V_{CE} \) are bias values. In the following, as is standard in electronics circuit analysis, we approximate the output resistance, for example, for the npn as follows:

**Equation C.40**

\[ r_{on} = \frac{V_{AFn}}{I_C} \]

It follows that for the pnp

**Equation C.41**

\[ r_{op} = \frac{V_{Afp}}{I_C} \]

where \( I_C \equiv I_C(V_{CE}) \), that is, the actual bias collector current.

For the pnp active load, the resistor \( R_C \) is now replaced with the output resistance of the pnp, to obtain

**Equation C.42**
where the far right-hand side uses $g_m = I_C/V_T$.

The gains for the resistive load and active load cases can readily be compared with the substitution of $g_m = I_C/V_T$ in (C.38) (gain with load $R_C$) and (C.40) for $r_{on}$ to obtain

Equation C.43

$$a_{vb} = -g_m \frac{r_{on} r_{op}}{r_{on} + r_{op}} = -g_m \frac{1}{I_C} \frac{V_{AFn} V_{AFp}}{V_{AFn} + V_{AFp}} = -\frac{1}{V_T} \frac{V_{AFn} V_{AFp}}{V_{AFn} + V_{AFp}}$$

For the example of $V_{CC} = 10 \, \text{V}$ and bias $V_{CE} = 5 \, \text{V}, V_{Re} = 5 \, \text{V}$. Using $V_{AFn} = 100 \, \text{V}$ and $V_{AFp} = 20 \, \text{V}$, the room-temperature gain magnitudes are $|a_{vbRc}| = 4.76 \, \text{V}/0.026 \, \text{V}=183$ for the amplifier with $R_c$ load compared to an npn – pnp amplifier gain magnitude of $|a_{vb}| = 16.7 \, \text{V}/0.026 \, \text{V}=641$. In practice, the advantage will be considerably more, as the value for $V_{AFp}$ used here is smaller than normal for BJTs. The small number was used above in the plot (Fig. C.9) to exaggerate the effect of the slope.

C.7.2. Output Resistance at the Collector with an Emitter Resistor

In Project C2 the effect of an emitter resistor in the emitter branch of the pnp, $R_{E_p}$, on the output resistance of the pnp will be explored. The circuit is shown in Fig. C.10. The effect of the emitter resistor is to increase the output resistance, due to the negative feedback effect, at the collector of the pnp. This increase can be made to be substantial; in fact, to a good approximation, the load on the amplifier is only $r_{on}$ of the npn.

**Figure C.10. Amplifier with an emitter resistor in emitter branch of pnp to increase the output resistance at the collector of the pnp. Also included is a capacitor, $C_b$, for grounding (signal) the base voltage of the pnp.**
The generalized gain expression, which includes the effect of the emitter resistor, is

**Equation C.44**

\[ a_{vb} = -g_m \frac{r_{on} R_{op}}{r_{on} + R_{op}} \]

where \( R_{op} \) is the output resistance at the collector of pnp, for the circuit with \( R_{Ep} \).

Here, we develop an expression for the output resistance of a BJT with the emitter resistor. This is a function of both \( R_{Ep} \) and \( R_{Bp} \). In the **Project C2** the amplifier gain is measured with and without a base shunt capacitor, \( C_b \). With the capacitor in place, the base resistance in the signal circuit is effectively zero, and this alters \( R_{op} \) significantly. The linear circuit for the general case of a BJT common-emitter amplifier with emitter resistor is shown in **Fig. C.11**. The circuit includes a base resistor, \( R_B \).

**Figure C.11. Linear circuit for the determination of the output resistance at the collector for a circuit with emitter and base resistor.**
A test voltage, $V_o$, is applied at the collector with the base resistor and emitter resistor at signal ground. In response, a current $I_o$ flows from $V_o$ through $R_E$ in parallel with $R_B + r_\pi$. This induces a voltage $V_{RE} = (I_o - I_b)R_E$ across $R_E$ that is applied to $r_\pi$ in series with $R_B$.

Base current $I_b$ is a fraction of $I_o$ as given by

**Equation C.45**

$$I_b = -\frac{R_E}{r_\pi + R_B + R_E} I_o$$

Applied voltage $V_o$ sums up to

**Equation C.46**

$$V_o = (I_o + g_m I_b r_\pi) r_\pi + (I_o - I_b)R_E + (I_o + g_m I_b r_\pi) r_\pi$$

The approximation is based on $r_\pi \gg R_E$ and is consistent with the fact that the signal voltage drop across the output of the transistor is much greater than across the emitter resistor.

Eliminating $I_b$ in (C.46) using (C.45) results in the solution for $R_o$, which is

**Equation C.47**

$$R_o \equiv \frac{V_o}{I_o} = \left(1 + g_m \frac{R_E}{r_\pi + R_B + R_E} \right) r_\pi$$
The result has two limiting forms based on the relative value of \( R_B \): When \( R_B \gg r_\pi + R_E \),

**Equation C.48**

\[
R_O = \left(1 + g_m \frac{r_\pi R_E}{R_B}\right) r_o = \left(1 + \frac{\beta_{ac} R_E}{R_B}\right) r_o \approx \left(1 + \frac{\beta_{ac} V_T}{\beta_{DC} V_{BE}}\right) r_o \approx r_o
\]

The approximate form uses \( I_C \approx I_E \).

Intuitively, for \( R_B \to \infty \), the feedback current, \( g_m I_b r_\pi \), goes to zero.

For \( R_B \to 0 \),

**Equation C.49**

\[
R_O = \left(1 + g_m \frac{r_\pi R_E}{r_\pi + R_E}\right) r_o = \left(1 + \beta_{ac} \frac{R_E}{r_\pi + R_E}\right) r_o \approx \frac{\beta_{ac} V_T}{1 + \beta_{ac} V_T} r_o \gg r_o
\]

The alternative forms on the right in (C.48) and (C.49) use (C.15), \( \beta_{ac} = g_m r_\pi \). Again, the approximate form uses \( I_C \approx I_E \). Note that the solution corresponds to the maximum fraction of \( I_o \) that can flow through \( r_\pi (R_B = 0) \), to induce a feedback current.

When applied specifically to the npn – pnp circuit of Fig. C.10, the limiting case is, for \( R_{Bp} \) zero,

**Equation C.50**

\[
R_{Op} = \frac{\beta_{acp}}{1 + \frac{\beta_{acp} V_T}{V_{BEp}}} r_{Op}
\]
where $R_{op}$ is the signal resistance looking up into the collector of the pnp. For example, if $R_{Ep}$ is selected to produce $V_{REp} = 1$ V and $\beta_{acp} = 50$, the denominator is roughly 2, such that $R_{op} \approx (\beta_{acp}/2)r_{op}$. In this case, the load on the amplifier is due almost entirely to the output resistance looking into the collector of the npn ($\text{Ron} = r_{on}$), with the result that the gain is [from C.44]

**Equation C.51**

$$a_{vb} \approx -\frac{V_{AFn}}{V_T}$$

The other extreme is for $R_{Bp} \gg r_{np} + R_{Ep}$, where $R_{op} \approx r_{op}$ [(C.48)]. The gain reverts to (C.42), repeated here

$$a_{vb} \approx -\frac{1}{V_T} \frac{V_{AFn}V_{AFp}}{V_{AFn} + V_{AFp}} = -\frac{1}{V_T} V_{AFp}$$

The npn – pnp amplifier circuit of [Fig. C.10](#) is used in the project on the amplifier to investigate the signal-derived magnitude of the slope parameters of npn and pnp transistors. Using a bypass capacitor at the base of the npn, as discussed below, the signal circuit will effectively have $R_B = 0$, and a gain measurement along with (C.51) yields $V_{AFn}$. The gain will also be measured for the circuit without the capacitor and with $R_{Bp} \gg r_{np} + R_{Ep}$ (by design). For this case, (C.42) applies and the gain measurement provides information on the combination output resistance parameter, $V_{AFnp}$. Between the two measurements, values for both parameters are determined.

In the measurement circuit of the npn – pnp amplifier, the gain referred to the signal source (amplifier circuit gain) is

**Equation C.52**

$$a_v = -\beta_{acn} \frac{R_{onp}}{R_{En} + r_{nn}} \approx -\beta_{acn} \frac{R_{onp}}{R_{En}}$$

where $R_{onp}$ is the signal resistance at the output node (Fig. C.10), that is, the combined resistance looking back into the collects of the npn and pnp transistors. In general, this is

**Equation C.53**
\[ R_{onp} = \frac{r_{on}R_{op}}{r_{on} + R_{op}} \]

With \( R_{bp} \) effectively made zero with the shunting capacitor, \( R_{onp} \approx r_{on} = V_{AFn}/I_C \). Without the capacitor, \( R_{op} \) is obtainable from (C.47) for use in (C.53).

In the amplifier project, the circuit-gain equation (C.52) is used to convert measured gain into \( R_{onp} \) and then information on \( V_{AFn} \) and \( V_{AFp} \). With the availability of these numbers, we can then calculate the gain produced by the transistor (base to collector), using (C.44).

### C.7.3. DC (Bias) of the NPN – PNP Amplifier

The circuit equations for the circuit of Fig. C.10 are (collector power supply through pnp base)

**Equation C.54**

\[ V_{CC} = I_C \left( 1 + \frac{\beta_{DCp}}{\beta_{DCp}} R_{Ep} \right) + V_{EBp} + \frac{I_C}{\beta_{DCp}} R_{Bp} \]

and (nbn base)

**Equation C.55**

\[ V_{BBn} = \frac{I_C}{\beta_{DCn}} R_{Bn} + V_{BBn} \]

In the project on the amplifier, \( R_{bp} \) is determined for a design collector current. The selection uses (C.54) with, for example, \( V_{CC} \approx 9 \text{ V} \), that is, less than the maximum available from the DAQ output. Then with \( R_{Bn} = R_{Bp} \), \( V_{BBn} \) will be less than \( V_{CC} \) by the amount of the drop across \( R_{Ep} \) (for example, 1 V). This makes the good assumption that \( \beta_{DCn} \approx \beta_{DCp} \). A LabVIEW program then sets up the circuit for the design collector current by adjusting two supply voltages (DAQ output channels).

### C.8. Frequency Response of NPN – PNP Amplifier Due to the Base Shunt Capacitor

In the npn – pnp amplifier project, we determine \( V_{AFn} \) directly through a gain measurement for a circuit configuration in which (C.51) is valid. The requirement that
$R_{Bp} \approx 0$ will be implemented by shunting the base of the pnp transistor to ground with a capacitor, $C_b$, as shown in Fig. C.12. The capacitor must be sufficiently large to hold the base at ground at the frequency of the gain measurements.

**Figure C.12. Segment of the npn – pnp amplifier of Fig. C.10 showing the addition of a pnp base-bypass capacitor, $C_b$.**

The expression to determine the required value of $C_b$ can be obtained as follows: We start with the expression for $R_o$ without $C_b$, which is (C.47) and repeated here (referring to the generalized circuit Fig. C.11):

$$R_o \equiv \frac{V_o}{I_o} = \left(1 + g_m \frac{R_E}{r_\pi + R_B + R_E} \right) r_o$$

With the capacitor in parallel with $R_{Bp}$, $R_B$ in (C.47) is replaced with the impedance of the parallel combination of $R_{Bp}$ and $C_b$. The resulting $R_{op}$ is frequency dependent and is given by

**Equation C.56**

$$R_{op}(f) = \left\{1 + \frac{r_\pi p + R_{Ep} + \frac{g_m R_{Ep}}{1 + j2 \pi f R_{Bp} C_b}}{r_\pi p + R_{Ep}}\right\} r_{op}$$

This can be manipulated into the form
where

Equation C.58

\[ f_1 = \frac{1}{2\pi r_{Bp} c_b} \]

and

Equation C.59

\[ f_2 = \frac{r_{\pi p} + R_{Ep} + R_{Ep} f_1}{r_{\pi p} + R_{Ep}} \approx \frac{1}{2\pi (r_{\pi p} + R_{Ep}) c_b} \]

The approximate form uses \( R_{Bp} \gg r_{\pi p} + R_{Ep} \). At \( f \approx f_1 \), \( R_{op}(f_1) \approx r_{op} \), such that a good approximation is obtained with dropping the "1" in the numerator. The approximate form is then

Equation C.60

\[ R_{op}(f) = \left(1 + \frac{g m r_{\pi p} R_{Ep}}{r_{\pi p} + R_{Ep} + R_{Bp} \left(1 + jf/f_2\right)}\right)r_{op} \]

Further rearranging leads to

Equation C.61

\[ R_{op}(f) = R_{op\max} \frac{f_2 + jf}{f_2 + jf} \]
where

**Equation C.62**

\[
R_{\text{op max}} = \left( 1 + \frac{\beta_{\text{acp}} R_{\text{Ep}}}{R_{\text{Ep}} + r_{\text{np}}} \right) R_{\text{op}}
\]

and

**Equation C.63**

\[
f_2 = \frac{r_{\pi p} + R_{\text{bp}} + R_{\text{Ep}}}{r_{\pi p} + R_{\text{Ep}} + \beta_{\text{acp}} R_{\text{Ep}}} f_1 \approx \frac{1}{2\pi \beta_{\text{acp}} R_{\text{Ep}} C_b}
\]

The approximate form again uses \( R_{\text{bp}} \gg r_{\text{np}} + R_{\text{Ep}} \).

Mathcad-generated plots of the magnitude of \( R_{\text{op}}(f) \) using (C.57) (and \( f_2 \) and \( f_z \) exact) and (C.61) (with the approximate forms for \( f_2 \) and \( f_z \)) are shown in Fig. C.13. These are for \( V_{\text{AFp}} = 150 \text{ V}, \beta_{\text{acp}} = 50, R_{\text{bp}} = 330 \text{ K\Omega}, R_{\text{Ep}} = 800 \text{ \Omega}, C_b = 2 \mu\text{F} \) and \( I_c = 1 \text{ mA} \). Characteristic frequencies are \( f_z = 1.9 \text{ Hz} \) and \( f_2 = 38.2 \text{ Hz} \). The approximate form is very close to the exact form except in the lowest frequency range. For \( f \rightarrow 0 \), \( R_{\text{op}}(f) \approx r_{\text{op}} \) in both cases. For example, in the exact and approximate cases, \( R_{\text{op}}(f) = 1.12r_{\text{op}} \) and \( R_{\text{op}}(f) = 1.05r_{\text{op}} \), respectively, for \( f = 0 \).

**Figure C.13. Mathcad-generated plots of the magnitude of \( R_{\text{op}}(f) \) using (57) and (61). The calculation made with the approximate form, (61), also uses the approximate forms for \( f_2 \) and \( f_z \).**
Substituting $R_{op}(f)$ for $R_{op}$ in (C.52), we obtain the frequency-dependent amplifier-circuit gain

**Equation C.64**

$$a_v(f) = -\frac{\beta_{ac}}{R_{bn}} \cdot \frac{r_{on}}{1 + \frac{r_{on}}{R_{op}(f)}}$$

Then using (C.61) for $R_{op}(f)$ in (C.64) results in

**Equation C.65**

$$a_v(f) = \frac{\beta_{ac}}{R_{bn}} \cdot \frac{R_{op max} r_{on}}{R_{op max} + r_{on}} \cdot \frac{f_z + j f}{f_p + j f}$$

where

**Equation C.66**

$$f_p = \frac{R_{op max} f_z + r_{on} f_z}{R_{op max} + r_{on}} = \left(1 + \frac{r_{on}}{R_{op max}}\right) \frac{1}{2 \pi \beta_{ac} R_{Ep} C_b}$$

The approximate form uses $R_{op max} \gg r_{on}$ and the approximate $f_z$ and $f_p$. 
The design frequency $f_{3\text{dB}}$ is obtained from $f_{3\text{dB}} = \sqrt{f_e^2 - 2f_z^2}$ [(6.8)]. Utilizing the approximate forms of $f_2$, $f_z$, and $f_p$, $f_{3\text{dB}}$ simplifies to

**Equation C.67**

$$f_{3\text{dB}\text{approx}} = \frac{1}{2\pi\beta_{\text{acp}}R_{\text{Ep}}C_b} \left( \frac{r_{\text{on}} + r_{\text{op}}}{r_{\text{op}}} \right)^2 - 2$$

The result is significantly lower than $f_2$ in (C.61) because $R_{\text{op}}(f)$ is in parallel with $r_{\text{on}}$, which is much smaller than the high-frequency value of $R_{\text{op}}(f)$. The parameter $\beta_{\text{acp}}$ appears from the association $\beta_{\text{acp}} = g_m r_{\text{np}}$ [(C.15)].

Mathcad-generated plots of (C.65) for the exact and approximate values for $f_p$ and $f_z$ are shown in Fig. C.14. The parameter and component values are from the plots of Fig. C.13 with the addition of $V_{\text{AFn}} = 250$ V, $\beta_{\text{acn}} = \beta_{\text{acp}} = 50$, and $R_{\text{Bn}} = R_{\text{Bp}} = 330$ kΩ. With capacitor $C_b = 2$ μF, $f_{3\text{dB}} = 3.8$ Hz (exact $f_p$ and $f_z$) and $f_{3\text{dB}\text{approx}} = 4.5$ Hz [(C.67)].

**Figure C.14. Plots of (C.65) with approximate and exact values for $f_p$, (C.63), and $f_p$, (C.66). The approximate form is sufficiently close for selecting $C_b$.**

C.9. Common-Emitter Stage with Emitter Resistor and the Emitter-Follower Amplifier Stage

It was shown that the emitter resistor of the measurement circuit of Fig. C.10 can have a significant effect on output resistance. The emitter resistor has the effect of increasing the input resistance as well, such that it is compatible with high-resistance sources and the resistor adds to the bias stability. The common-emitter stage with an emitter resistor is, in fact, a very common configuration in BJT electronics.
Here, we analyze the effect of the emitter resistor on the input resistance (at the base) and on the gain of the common-emitter stage. The development leads directly to an assessment of the signal performance of the emitter-follower (common-collector) stage. The two aspects of the circuit with the emitter resistor are discussed in the following.

C.9.1. Input Resistance in the Common-Emitter Emitter-Resistor Circuit

The discussion is applicable to the circuit of Fig. C.10, where the input resistance is at the base of the pnp. In this circuit, \( R_E = R_{Ep} \) and, for the analysis, a base signal voltage, \( V_{b} \), is applied directly to the base of the pnp. A general signal circuit for a common-emitter stage (output, \( V_{oce} \)) with emitter resistor is shown in Fig. C.15. Also indicated is the output for the emitter-follower stage (\( V_{oef} \)).

Figure C.15. Linear circuit for deriving the input resistance of the common-emitter stage with emitter resistor. The amplifier output nodes for the common-emitter stage (\( V_{oce} \)) and the emitter-follow (\( V_{oef} \)) stage are indicated.

Assume that \( r_o >> R_L \), such that we can neglect the current through \( r_o \). (This assumption is violated in the circuit of Fig. C.10, as the load is the output resistance of the npn, \( r_{on} \).) With this simplification, the loop equation at the input of the circuit is

Equation C.68

\[
V_b = V_{be} + g_m V_{be} R_E = I_b r_s + I_b g_m r_s
\]

having used \( V_{be} = I_b r_s \). The input resistance at the base is thus (with respect to signal ground)
Equation C.69

\[ R_{ib} = \frac{V_b}{I_b} = r_\pi + (1 + g_m r_n) R_E = r_\pi + (1 + \beta_{ac}) R_E \]

The following form of the result provides a convenient way of assessing the effect of the resistor on the input resistance:

Equation C.70

\[ R_{ib} = \frac{\beta_{ac}}{g_m} + (1 + \beta_{ac}) R_E = \beta_{ac}\frac{V_T}{I_C} + (1 + \beta_{ac})\frac{V_{RE}}{I_C} \]

The result shows that with \( R_E \) in the circuit, the input resistance is increased over that of the circuit without \( R_E \) by a factor of approximately \( V_{RE}/V_T \). For example, with \( V_{RE} = 1 \text{ V} \), \( V_{RE}/V_T \) is about 40 at room temperature.

For the npn – pnp circuit of Figure C.10, \( R_{ib} \) at the base of the pnp is somewhat less than given by (C.70) because the effective load, that is, \( r_{on} \), is so large and the simplification made above, \( r_o \gg R_L \), is not valid. However, as is usually the case in design, such approximate forms are sufficient. This takes into consideration that exact solutions are not required or justified, given the variation in the model and circuit parameters that naturally occur.

If better precision is, however, required, a good approximation for (C.70) is readily obtained by replacing, in (C.70), \( 1 + \beta_{ac} \) with \( 1 + \beta_{ac}\left[r_{op}/(r_{op} + r_{on})\right] \). This is specifically applied to the circuit of Figure C.10, where the input is at the base of the pnp and \( r_{on} \equiv R_L \) and the output resistance of the pnp is \( r_{op} \). The approximation is based on the expectation that \( V_{ooe} \gg V_{oef} \) Figure C.15 such that the voltages across \( r_{on} \) and \( r_{op} \) are similar.

Equation C.71

\[ a_{vb} = \frac{V_c}{I_b} = -\frac{I_C R_L}{R_{ib}} = \frac{\beta_{ac} R_L}{R_{ib}} = \frac{\beta_{ac} R_L}{r_\pi + (1 + \beta_{ac}) R_E} \approx \frac{R_L}{R_E} \]

Suppose that the gain expression is applied to the circuit of Figure C.1(b) but with an emitter resistor installed. From the signal source, the gain is then
\[ a_v = \frac{R_b}{R_z + R_b} a_{vb} \]

where the resistance at the base, \( R_b \), is now

\[ R_b = \frac{R_{ib}R_B}{R_{ib} + R_B} \]

With \((C.71)\) for the base-to-output gain,

\[ a_v \approx -\frac{R_b}{R_z + R_b} \beta_{ac} \frac{R_L}{R_{ib}} \approx -\frac{R_b}{R_z + R_b} \frac{R_L}{R_E} \]

The result shows that the maximum gain is approximately \( R_L/R_E \). Therefore, although the circuit can have good bias stability, the emitter resistor seriously reduces the signal gain. The circuit with a bypass capacitor would have a gain given by \((C.19)\). The circuit with a bypass capacitor would still have the advantage of bias stability. Essentially all practical common-emitter circuits have the emitter resistor, with or without the bypass capacitor. A two-stage-circuit significant voltage gain without a capacitor is discussed in the next unit.

**C.9.2. Emitter-Follower Amplifier Stage**

When the output is taken at the emitter instead of at the collector \((\text{Fig. C.15})\), the circuit becomes an emitter-follower amplifier stage. (The collector resistor is unnecessary and the collector terminal is connected to the power supply.) The output voltage in this case is

\[ V_{oef} = (I_b + I_c)R_E = I_b (1 + \beta_{ac})R_E \]

The emitter-follower stage gain (transfer ratio) is the ratio of \((C.75)\) and \((C.68)\), that is
Equation C.76

\[ a_{\text{vef}} = \frac{(1 + \beta_{ac})R_E}{r_I + (1 + \beta_{ac})R_E} = \frac{(1 + \beta_{ac})R_E}{g_{m} + (1 + \beta_{ac})R_E} \]

A magnitude assessment can be made from

Equation C.77

\[ a_{\text{vef}} = \frac{(1 + \beta_{ac})R_E}{I_C + (1 + \beta_{ac})R_E} \approx \frac{V_{R_E}}{V_T + V_{R_E}} \]

For example, with \( V_{RE} = 1 \text{ V} \), \( a_{\text{vef}} = 0.97 \) at room temperature. The input resistance, from (C.70), for the same conditions in addition to \( I_C = 0.1 \text{ mA} \) and \( \beta_{ac} = 100 \) is \( R_{ib} = 1 \text{ M}\Omega \). The emitter-follower stage is seen to have a gain of approximately unity and a very high input resistance. Its primary role is therefore that of a buffer stage.

An alternative form for the emitter-follower stage gain is

Equation C.78

\[ a_{\text{vef}} = \frac{R_E}{V_T \frac{\beta_K}{I_C (1 + \beta_{ac})} + R_E} \approx \frac{R_E}{\frac{1}{g_m} + R_E} \]

This is equivalent to a unity-gain amplifier with an output resistance of \( 1/g_m \). The output resistance is, for example, about 26 \( \Omega \) at \( I_C = 1 \text{ mA} \). Therefore, when an external load is attached to the emitter-follower stage output, the gain remains near unity for very small load values.

An example of an application that takes advantage of the characteristics of the emitter-follower stage is shown in Fig. C.16. This is a cascade of an emitter-follower stage and a common-emitter stage. The overall gain is the product of the input network function and the gains of the two stages. That is,

Equation C.79
where $R'_E = R_E | l_{\pi} R_{\text{CE}}$. For example, suppose that $\beta_{bc} = 100$ and that the bias collector currents are $I_{C1} = 0.1 \text{ mA}$ and $I_{C2} = 10 I_{C1} = 1 \text{ mA}$. The emitter resistor is $R_E = V_{BE}/I_{C1} = 6000 \Omega$ (neglecting the base current, $I_{B2}$) with $V_{BE} = 0.6 \text{ V}$ such that $R'_E \approx 4900 \Omega$ and the gain of the emitter-follower stage is 0.87. With $V_{CC} = 10 \text{ V}$ and $V_{CE} = 5 \text{ V}$, the gain of the common-emitter stage is –192. Both gains are at room temperature. Therefore, the gain from the base of the emitter-follower stage to the output is –168.

**Figure C.16. Cascade of an emitter-follower stage and a common-emitter stage. The overall gain is the product of the gains of the separate stages. The load on the emitter-follower stage is $r_{\pi2}$ of the common-emitter stage.**

The input resistance at the base of the emitter follower is $R_{ib} \approx 500 \Omega$. Assume, for example, that $R_B \approx 50 \Omega$. The overall gain for this case is –136. By comparison, the circuit, which omits the emitter-follower stage ($R_B$ connected directly to the base of the common-emitter stage), has a gain of –9.5.

### C.10. Summary of BJT Model Parameter Relations

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<th>Formula</th>
<th>Description</th>
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<td>$g_m$</td>
<td>$I_C/V_T$</td>
<td>Transconductance.</td>
</tr>
<tr>
<td>$r_{\pi}$</td>
<td>$\frac{g_m \beta_{bc} V_T}{I_C}$</td>
<td>Emitter-base junction common-emitter stage input resistance.</td>
</tr>
<tr>
<td>$r'_o$</td>
<td>$V_{AF}/I_C$</td>
<td>Collector – emitter output resistance.</td>
</tr>
<tr>
<td>Equation</td>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>-----------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>( g_m = \frac{I_C}{V_T} )</td>
<td>Transconductance.</td>
<td></td>
</tr>
<tr>
<td>( r_i = r_D + r_B )</td>
<td>Total base – emitter input resistance.</td>
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### C.11. Summary of Circuit Equations

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<td>Base current equation for common-emitter amplifier.</td>
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<tr>
<td>( V_{BE} \approx V_T \ln \left( \frac{I_C}{I_S} \right) )</td>
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<tr>
<td>( V_{CE} = V_{CC} - I_C R_C )</td>
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<td>( \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE}}{R_B} \beta_{DC} )</td>
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<td>( a_{vb} = -g_m R_C )</td>
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<td>( a_v = -\frac{R_b}{R_b + R_i} g_m R_C )</td>
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<td>Overall gain with very large source resistor, ( R_s ), as in amplifier gain experiments. ( R_s \gg r_B ), ( R_B \gg r_B ).</td>
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<td>Base-to-collector large-signal &quot;gain&quot; that includes nonlinearity of ( I_C ), ( V_{BE} ) relationship. Linear relation applies when ( I_C/I_C ) ratio is small enough for ( \ln(1 + I_C/I_C) \approx I_C/I_C ).</td>
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<td>General solution for base-to-collector gain for npn – pnp amplifier with emitter resistor, $R_{Ep}$.</td>
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<td>$f_p = \frac{R_{omax} f_2 + r_{on} f_2}{R_{omax} + r_{on}} \approx \left( 1 + \frac{r_{on}}{r_{op}} \right)^{-1} \frac{1}{2\pi \beta_{acp} R_{Ep} C_B}$</td>
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Base current equation for common-emitter amplifier.

\[ R_i = r_T + (1 + g_m \cdot r_T) R_E = r_T + (1 + \beta_{ac}) R_E \]

Input resistance at base of common-emitter stage with emitter resistor.

\[ a_{v_{ef}} = \frac{1 + \beta_{ac} R_E}{I_C R_T + (1 + \beta_{ac}) R_E} \approx \frac{V_{RE}}{V_T + V_{RE}} \]

Gain of the emitter-follower stage.

\[ a_{v_{ef}} \approx \frac{R_E}{1 + g_m \cdot R_E} \]

Alternative form of the gain of the emitter-follower stage.

**C.12. Exercises and Projects**

Project Mathcad Files: ExerciseC1.mcd – ProjectC1.mcd – ExerciseC2 – ProjectC2.mcd

Laboratory Project C1: [NPN Common-Emitter Amplifier](#)

- **PC.2**  
  DC Circuit Setup and Parameter Determination

- **PC.3**  
  Amplifier Gain at One Bias Current

- **PC.4**  
  Amplifier Gain versus Bias Current

- **PC.5**  
  Gain-Measurement Frequency Response

Laboratory Project C2: [NPN – PNP Common-Emitter Amplifier with Current-Source Load](#)

- **PC.7**  
  Measurement of the PNP Parameters

- **PC.8**  
  DC Circuit Setup

- **PC.9**  
  Measurement of the Amplifier Gain

**C.11. Summary of Circuit Equations**

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C.12. Exercises and Projects

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- ExerciseC1.mcd – ProjectC1.mcd – ExerciseC2 – ProjectC2.mcd

Laboratory Project C1
- NPN Common-Emitter Amplifier
  - PC.2 DC Circuit Setup and Parameter Determination
  - PC.3 Amplifier Gain at One Bias Current
  - PC.4 Amplifier Gain versus Bias Current
  - PC.5 Gain-Measurement Frequency Response

Laboratory Project C2
- NPN – PNP Common-Emitter Amplifier with Current-Source Load
  - PC.7 Measurement of the PNP Parameters
  - PC.8 DC Circuit Setup
  - PC.9 Measurement of the Amplifier Gain

Laboratory Project 1. Basic Circuit Analysis for Electronic Circuits and Programming Exercises

P1.1 Resistor Voltage-Divider Measurements
P1.2 Resistor Voltage Divider with Current Measurement
P1.3 Resistor Voltage Divider with Resistor Measurement
P1.4 Resistor Voltage Divider with a Sine-Wave Source Voltage
P1.5 Frequency Response of a Resistor-Capacitor Circuit

Exercises and Analysis Exercise01.mcd - Project01.mcd
P1.1. Resistor Voltage-Divider Measurements

Components

\[ R_{G1} \approx R_{G2}/X \]
\[ 0.5 < X < 2 \]

\[ \text{Chan0\_out}_{\text{max}} = 10 \ \text{V} \]

\[ I_{R_G \text{max}} = \frac{\text{Chan0\_out}_{\text{max}}}{R_{G1} + R_{G2}} \]
\[ 10 \ \mu\text{A} < I_{R_G \text{max}} < 100 \ \mu\text{A} \]

Programming Exercise 1.1

Use Tab to switch between Tools. Use Space Bar to switch between Wiring Tool and Position Tool (arrow). Get Tools Palette under Windows menu (or Shift/Right Click)
from the Diagram.

- Open a new VI to construct your **VI_01.vi**. The VI opens with a Front Panel (top) and a Diagram (under). Switch from one to the other using the Windows menu or Ctrl/E. The VI opens with the Operate Value Tool.

- Place a Digital Control and Digital Indicator on the Front Panel (example below). (Right Click on Front Panel to get the Controls Palette.) The Digital Control and Digital Indicator are in the Numeric Palette (below). Save the file with your choice of Name.

- Go to the Diagram (Ctrl/E) or Window>>Show Diagram. Place a Sequence Structure in the Diagram. (Right Click on Diagram to get Functions>>Structures>>Sequence Structure.) Enlarge the Structure by contacting the Arrow Tool (Position Tool) at the bottom-right corner of the Structure (drag).
• Right Click on the edge of the Frame and Add Frame After. Click on arrows to switch between Frame 0 and Frame 1.

• Place **AO Update Channel.vi** in Frame 0.
  
  (Functions>>Data Acquisition>>Analog Output >>AO Update Channel.vi.)

• Place **AI Sample Channel.vi** in Frame 1.
  
  (Functions>>Data Acquisition>>Analog Input>>AI Sample Channel.vi.)
• Position the icons, etc., with the Arrow Tool (Left Click>>Drag).

• Wire the Digital Control (darker) terminal to the value terminal of the Analog Output VI, **AO Update Channel.vi**. Press the space bar to alternate between the Wiring Tool and Position (arrow) Tool.

• To wire, get the Wiring Tool (space bar), Left Click on a terminal, release, drag the Tool to the opposite terminal, and Left Click. To clean up wiring mistakes, use Ctrl/B. Note that the terminal name (value in the example) of an
icon is displayed while the Wiring Tool is over the terminal.

- Wire the Digital Indicator terminal (lighter) to the output terminal (sample) of the Analog Input VI, *AI Sample Channel.vi*.

- Place the Constant (4) and the String (0) in the Diagram as shown in the example (Frame 0). Use the Writing Tool to type in the numbers. The location of Constants and Strings, under Functions, is shown below. Place Constants (4), (10) and (0) and String (0) in Frame 1.

- Wire the Constants and Strings as shown in the examples. To wire, get the Wiring Tool (space bar), Left Click on a terminal, release, drag the Tool to the opposite terminal, and Left Click. To clean up wiring mistakes, use Ctrl/B.

- Change the names of the Digital Control and Digital Indicator. Use the Writing Tool. This can be done from the Diagram or the Front Panel. Click
on the existing name (e.g., Numeric) and edit.

**Procedure**

- Calculate the resistor values. Connect the circuit.
- To Run a VI, from the Front Panel, use Operate>>Run or (better) use Ctrl/R. Run the VI with Chan0_out = 10V (Vout) and note the value of Chan0_in (VRG2). This should be consistent with your resistor ratio choice. Try a variety of Chan0_out values. (The maximum is 10 V.)

![Image](Image.png)

- (Optional) To install the circuit Diagram on the Front Panel, open **VI_01.vi** from **Project01.llb**. Use the Arrow Tool, Click on the circuit diagram, use Window's copy (Ctrl/C), and paste it into your VI Front Panel.

---

**P1.2. Resistor Voltage Divider with Current Measurement**

![Diagram](Diagram.png)

**LabVIEW Computation**
\[ I_{RG} = \frac{\text{Chan0\_in}}{R_{G2}} \]

**Programming Exercise 1.2**

- Save a copy of VI_01.vi (your name) and give it a new name (such as #2).

- On the Front Panel, place a Digital Indicator for IRG (Controls>>Numeric).

- On the Front Panel, place a Digital Control for the resistor value. (Controls>>Numeric.)

- In the Diagram (below) place a Divide operation. (Functions>>Numeric>>Divide.)

- Wire the Diagram as in the example.

**Procedure**

- Set your value of \( R_{G2} \) in the Digital Control (MΩ). To set in three digits,
change the precision. Right Click on the Control, go to Format and Precision, and change Digits of Precision.

- Run VI_02.vi with Chan0_out set at 5 V and note the value of IRG. 
  Default and save the Front Panel for comparison with the Mathcad evaluation file. For Default, menu Operate>>Make Current Values Default.

**P1.3. Resistor Voltage Divider with Resistor Measurement**

Basic sample shown below.
Programming Exercise 1.3

- Save a copy of VI_02.vi with a new name and add Digital Indicators for VRG1 and RG1 as in VI_03.vi (basic sample below). The new VI will find and indicate the value of RG1.

![Diagram showing the circuit with indicators for VRG1 and RG1](image)

- In the Diagram, we will add Get Y Value.vi. This VI is found in the Functions Palette with the sequence shown on the left.

- Note that the full Palette Set is required. Your Palette may be an abbreviated form called Basic. If so, open the Palette and use the Stick Pin to keep it open. Then Click on Options as shown below. Select the default Palette Set.
- **Get Y Value.vi** is used to extract a given Y value in a waveform. AI Sample **Channel.vi** is a special case of a waveform with only one component. In the VI of part P1.2, we connected the output directly to a Digital Indicator, in which case, LabVIEW sorted out the component value automatically.

- Place **Get Y Value.vi** as shown in the Diagram (cursor, Arrow). Connect the balance of the circuit as shown. The new math formulations are indicated below and in the Diagram.

**LabVIEW Computations**

\[ R_{G1} = \frac{V_{R \cdot G1}}{V_{R \cdot G2}} \]

\[ V_{R \cdot G1} = \text{Chan0\_out} - \text{Chan0\_in} \]

**Procedure**

- Run the VI_03.vi for Chan0\_out set at 10 V. Note the value of RG1 and VRG1. **Default and save** the Front Panel for the Mathcad evaluation file.
P1.4. Resistor Voltage Divider with a Sine-Wave Source Voltage

Procedure

- The VI sends out, on Chan0_out, a sine-wave superimposed on the dc value. Add the connection, Chan1_in, directly to the output channel. **Run** the VI for various values of Chan0_out. Note that the maximum allowed Chan0_out is about 6 V since the dc and ac peak must be less than 10 V. Verify that the results are consistent. For example, the peak ac values must be 1.5 of the dc values since $V_s = V_{DD}/2$. **Default and save** the Front Panel using Chan0_out = 4V.
**P1.5. Frequency Response of a Resistor-Capacitor Circuit**

**Components**

\[ C_1 = C_2 \]

\[ f_{3dBhi} = 50f_{3dBlo} \]

\[ R_s \approx R_G/50 \]

\[ f_{3dBlo} = 5 \text{ Hz (approximately)} \]

\[ C_1 \approx \frac{1}{2\pi R_G f_{3dBlow}} \]

\[ R_G = R_{G1} \parallel R_{G2} \]

Typical \( C_1 \approx 0.5 \mu F \)

**Procedure**

- Configure the circuit for the low-end measurement and \( f_{3dBlo} \). Install \( C_1 \) and do not install \( C_2 \). **Run VI_05.vi** to obtain \( f_{3dBlo} \). Obtain a Log of the Front Panel to save the results. To obtain a Log, go through menu sequence **Operate>>Data Logging>>Log**. To retrieve data: **Operate>>Data Logging>>Retrieve**.

- An example of retrieving a Log using **VI_01.vi** is shown here. Note that at the first Data Logging, you will be asked to name a Data Log file.
Select any name and Click Save, to install Log File in the Project folder.

- Now move the capacitor $C_2 = C_1$ to the $C_2$ location and install a large capacitor, $C_{1\text{new}}$, in place of $C_1$, which satisfies $C_{1\text{new}} \gg C_2$ (e.g., $C_{1\text{new}} = 47 \ \mu F$). Note that the source side of the capacitor (connected to $R_s$) is more negative than the output side (Chan0_in). Run VI_05.vi to obtain $f_{3\text{dBhi}}$. Default and save the Front Panel. Note that when reopening the VI, the Front Panel will contain the information last defaulted from this $f_{3\text{dBhi}}$ measurement. The first measurement is in the data Log. Repeating, to retrieve the information from the data Log, go through menu sequence Operate>>Data Logging>>Retrieve. To then go back to the defaulted Front Panel, click OK and go through Operate>>Reinitialize All to Default Values.

- Note that if $C_2 = C_1$ are actually both in the circuit at the same time, the output in the plateau region is $1/2$ as large (Exercise 1). This configuration is not implemented here. The use of $C_2 = C_1$ is only for convenience and $f_{3\text{dBlo}} \ll f_{3\text{dBhi}}$ is satisfied with $R_s \ll R_G$. 
Laboratory Project 2. Basic NMOS Common-Source Amplifier with Programming Exercises

P2.1 NMOS Common-Source Circuit with Drain Current Measurement

P2.2 NMOS Common-Source Amplifier with Resistor Gate Bias Circuit

P2.3 Amplifier with Signal and Gain Measurement

Exercises and Analysis Exercise02.mcd - Project02.mcd

P2.1. NMOS Common-Source Circuit with Drain Current Measurement
Chip Diagram

Connect pin 14 to Chan0_out.

Maintain Chan0_out > Chan1_out.

Components
\[
R_D \approx \frac{\text{Chan0_out}_{\text{max}}}{I_{D_{\text{max}}}}
\]

\[
\text{Chan0_out}_{\text{max}} = 10V
\]

\[
I_{D_{\text{max}}} \approx 500 \mu A
\]

**Programming Exercise 2.1**

- On the Front Panel of a New VI, install two Digital Controls and two Digital Indicators (*AmpP2.1.vi*). Also install a Menu Ring (Controls>>Ring and Enum>>Menu Ring).

- In the Diagram (below), place, from left to right, one Case Structure: Functions>>Structures>>Case, and two While Loops:
Functions>>Structures>>While Loop.

- On the Front Panel, using the Text Tool (Shift/Right Click for Tool Palette) in the Menu Ring, type 10 V. Right Click on the Menu Ring and execute Add Item After. In the new listing, type 6 V. Go to the Diagram and wire the output of the Menu Ring to the "?" on the edge of the Case Structure. Note that the Items correspond to integers 0 and 1 at the terminal.

- In the Diagram, place two copies of AO Update Channel.vi in the first (left) While Loop and place AI Sample Channel.vi in the right-hand Loop. In the latter, also place Get Y Value.vi (Functions>>Waveform>>Waveform Operations>> Get Y Value.vi). Connect the constants and Front Panel terminals as in the example.

- Install constant values 10 and 6 in the 0 and 1 case states, respectively, and wire to the value terminal of the Chan0_out AO Update Channel.vi icon.

- Configure the current computation function as in the example (lower-right side in Diagram) and wire to the current Digital Indicator and resistor Digital Control. Optionally, relabel the Digital Controls and Digital Indicators according to their functions (as in AmpP2.1.vi).

Procedure

- Connect the circuit using the RD selected. Install the value of RD(MΩ) in the Digital Control. To obtain three digits of precision in the resistor Digital Control, Right Click on the Control and go to Format and Precision... Set Digits of Precision.

- Run AmpP2.1.vi with VDD (Chan0_out) set at 10 V. Adjust VGS
Obtain a log of the Front Panel to preserve the current (ID) and VGS information for the Mathcad file. Reminder: Data Logging is under the Operate menu.

- Now reset VDD to 6 V and re-run. Note that VDS drops by roughly 4 V, indicating that the transistor drain terminal is a current source. Note that the change in the ID indicated is only slight.

- Reset VDD = 10 V. Increase VGS by an amount that makes VDS about 2 to 3 V. Note the increase in drain current. Log the Front Panel to preserve the information for the Mathcad file.

**P2.2. NMOS Common-Source Amplifier with Resistor Gate Bias Circuit**

![Circuit P2.2 diagram](Diagram)

**Components**

\[ R_{G1} \approx 2R_{G2} \]
Programming Exercise 2.2

- Save a copy of AmpP2.1.vi (your name) and give it a new name.

- As in the example (below), use three While Loops to send Chan0_out and receive on Chan0_in and Chan1_in. Note that the index "i" of a loop on the left is connected to the border of the following Loop to establish the proper order of execution of the program.

- Provide Digital Indicators for VGS and VDS.
Procedure

- Run **AmpP2.2.vi** with VDD set at 6 V to obtain VGS of about 2 V (due to \( R_{G1} \approx 2 R_{G2} \)). Re-run and adjust VDD to obtain VDS equal to about one-half of VDD. Note that decreasing VDD raises VDS toward VDD. **Default and save** the Front Panel for the Mathcad evaluation.

**P2.3. Amplifier with Signal and Gain Measurement**

**Programming Exercise 2.3** follows below.

(Advanced-Optional)

Procedure

- Move the bottom of RG2 from ground to Chan1_out. The VI will send out a
sine-wave signal via this channel with peak $V_s$. Set Chan0_out (VDD) as in the circuit for P2.2 above (for $V_{DS} \approx \frac{VDD}{2}$).

- **Run** AmpP2.3.vi *(Project02.llb)* for various values of $V_s$. Re-set for a $V_o$ peak of about 1V ($V_{DS}/3$). Note the gains, which are $V_o/V_s$ and $V_o/V_g$. Verify that the gain from the source is about two-thirds of the gain the gate, based on the selection (ratio) of the gate bias resistors. Default and save the Front Panel for the Mathcad evaluation.

---

**Programming Exercise 2.3**

- Make a copy of AmpP2.2.vi with a new name.
- Go to the Diagram and delete all except Control and Indicator terminals.
- Install a Sequence Structure in the Diagram (below). In the first Frame, install AO Update Channel.vi. *(Functions>>Data Acquisition>>Analog Output.)* Press Ctrl and drag (with Arrow Tool) an additional copy, also in Frame 0.
- Connect a voltage-out (VDD, Chan0_out) value as shown in the example. Connect a numeric 0 (value) to set Chan1_out initially to 0 V for the dc measurements. Connect channel numbers (String) and device number (Numeric, 4 in the example).
• Add a Frame After. In this Frame (1), install two copies of AI Acquire Waveform.vi. (in menu Functions>>Data Acquisition>>Analog Input.) These will be used for the dc measurements. A given node voltage will be sampled 100 times and the samples will be averaged for the result. Connect constants to the icons as shown in the example. These include device (Numeric, 4, default), channel (String), number of samples (Numeric, 100), sample rate (Numeric, 10000), **high limit** (10 V) and **low limit** (0 V).

• Place two copies of Get Waveform Components in Frame 1 (Palette Functions>>Waveform>>Get Waveform Components). Then **Left Click** on the output (right side) of these and select "Y". Connect the inputs to the waveform outputs of AI Acquire Waveform.

• Connect the outputs of Get Waveform Components to the inputs of **Mean.vi** functions. These are located in Functions>>Mathematics>>Probability and Statistics or in Functions>>Analyze>>Mathematics>>Probability and Statistics. Connect the outputs of the **Mean.vi** icons to the terminals of the Digital Indicators of VDS (Chan0_in) and VGS (Chan1_in).

• Add a Frame After (2). In this Frame we place a general-purpose function generator and oscilloscope function. This is **FG1Chan.vi** and is in Functions>>User Libraries>>FunctGen. A Digital Control and a Digital Indicator are required for this Frame. Install Digital Control, Vs, and Digital
• Connect to **FG1Chan.vi**, the various terminals, constants, and strings. The connections include Frequency (Numeric, 50), Vacin (Vo), Chan_out (String, 1), Sinewave - SqWave (False), Graph Out (leave disconnected for now), Chan_in (String, 0), Vs (Digital Control), and VDCout (Numeric, 0).

• Now add another Frame after (3). In this Frame, install the same function, **FG1Chan.vi**. This can be copied and pasted from Frame 2. Add, in the Front Panel, an additional Digital Indicator, Vg. Make the connections the same as in Frame 2 except Chan_in (String, 1).

• In Frame 2, configure, using a divide function, Vo/Vs, as shown in the example. Add a Digital Indicator in the Front Panel with the label Vo/Vs and connect the output from the divide function to the terminal of this Digital Indicator.

• Click on the edge of Frame 2 and install Add Sequence Local and, to this, Connect Vacin (Vo). Move to Frame 3, install a Divide function, and configure Vo/Vg as in the example. Note that Vo comes from the Add Sequence Local from Frame 2. In the Front Panel, add an additional Digital Indicator to read Vo/Vg.

• Now add the graph in the Front Panel. (A detailed description of using a graph is given in [Section A.1.5.](#).) The graph for this case is a Waveform Graph. Get this in the Front Panel under Controls>>Graph>>Waveform Graph. Use the Coloring Tool to adjust the color of the graph background by Right Clicking on the graph with the Coloring Tool. Right Click on the sample trace in the Plot Legend to adjust the color of the trace. Using the Operating Tool, Right Click on the X Scale or Y Scale>>Formatting to set the Grid Options.

• Configure the Diagram for connecting to the graph. Outside the Sequence Structure and on the right, install a Build Array function. (Functions>>Array>>Build Array.) Connect the Plot output of **FG1Chan.vi**
Laboratory Project 3. Characterization of the PMOS Transistor for Circuit Simulation

P3.1 SPICE Parameters and Pin Diagram

P3.2 SPICE Equations

P3.3 PMOS Transistor

P3.4 Low-Voltage Linear Region of the Output Characteristic

P3.5 PMOS Parameters from the Transfer Characteristic

P3.6 PMOS Lambda from the Transfer Characteristic

P3.7 PMOS Output Characteristic

P3.8 PMOS Lambda

Exercises and Analysis Exercise03.mcd - Project03.mcd

### P3.1. SPICE Parameters and Pin Diagram

<table>
<thead>
<tr>
<th>SPICE Name</th>
<th>Math Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTO</td>
<td>$V_{tno}$, $V_{tpo}$</td>
<td>Zero VSB threshold voltage.</td>
</tr>
<tr>
<td>KP</td>
<td>$k_{n,p}$</td>
<td>Transconductance parameter.</td>
</tr>
<tr>
<td>GAMMA</td>
<td>$\gamma_n, \gamma_p$</td>
<td>Threshold voltage parameter.</td>
</tr>
<tr>
<td>LAMBDA</td>
<td>$\lambda_n, \lambda_p$</td>
<td>Active-region slope parameter.</td>
</tr>
</tbody>
</table>

CD4007 Pin Diagram
### SPICE PARAMETERS

<table>
<thead>
<tr>
<th>SPICE Name</th>
<th>Math Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_p$, $B_p$</td>
<td>$D_p$</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Gp</td>
<td>Bn</td>
</tr>
<tr>
<td>Pin 14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pin 13</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### P3.2. SPICE Equations

<table>
<thead>
<tr>
<th>SPICE Equation (PMOS)</th>
<th>NMOS Eq.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_{chan} = \frac{\mu_p C_{ox} W}{L} (V_{SG} - V_{tpo}) = 2k_p V_{effp}$</td>
<td>3.2</td>
<td>Output characteristic low-voltage conductance.</td>
</tr>
<tr>
<td>$V_{effp} = (V_{SG} - V_{tpo})$</td>
<td>3.10</td>
<td>Output characteristic for full linear range ($0 &lt; V_{SD} &lt; V_{effp}$).</td>
</tr>
<tr>
<td>$I_D = 2k_p V_{effp}^2 \left(1 + \lambda_p V_{SD}\right)$</td>
<td>3.8</td>
<td>Active region transfer characteristic and output characteristic ($V_{SD} &gt; V_{effp}$).</td>
</tr>
<tr>
<td>$V_{SG} = \sqrt{\frac{I_D}{k'<em>p}} + V</em>{tpo}$</td>
<td>3.12</td>
<td>Active region relation solved for $V_{SG}$.</td>
</tr>
<tr>
<td>$k'<em>p = k_p \left(1 + \lambda_p V</em>{SD}\right)$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
P3.3. PMOS Transistor

Use pins 6 (gate), 14 (source), and 13 (drain). Connect the NMOS body (pin 7) to the most negative node, Chan1_out, for PMOSparam.vi. Leave pin 7 disconnected when running PMOSoutput.vi. Note that the source and body for this transistor are internally connected. Note that Chan0_in is used for positive voltages only. Thus, it is always set automatically for the unipolar mode, which slightly improves the resolution. Chan1_in must measure positive and negative voltages.

P3.4. Low-Voltage Linear Region of the Output Characteristic

Components

\[
R_D \approx \frac{10 \text{ V}}{I_{D_{\max}}}
\]

\[
|\text{Chan0\_out}_{\text{max}}| = 10 \text{ V}
\]

\[
|\text{Chan1\_in}_{\text{max}}| = 0.1 \text{ V}
\]

\[
I_{D_{\max}} \approx 150 \mu \text{A}
\]

LabVIEW Computations
Procedure

- Run **PMOSlinear.vi** and adjust VSGstart(V) such that Veppstart(V) > 0.5 V. The maximum ID is set for 0.1 V. Run the VI to obtain parameters as indicated in the Front Panel. *Default and save* the Front Panel to save information for the Mathcad analysis.
P3.5. PMOS Parameters from the Transfer Characteristic

Components

\[ R_S \approx \frac{|\text{Chan0}_\text{out}_{\text{max}}| - |\text{Chan0}_\text{in}_{\text{min}}|}{I_{D_{\text{max}}}} \]

<table>
<thead>
<tr>
<th>Chan0_out_max</th>
<th>10 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chan0_in_min</td>
<td>3 V</td>
</tr>
<tr>
<td>I_{D_{\text{max}}}</td>
<td>\approx 500 \mu A</td>
</tr>
</tbody>
</table>

LabVIEW Computations
\[
k'_p = \frac{1}{\left(\text{slope}(V_{SG}, \sqrt{I_D})\right)^2}
\]

\[
V_{tpo} = f(V_{SG}, \sqrt{I_D})\bigg|_{I_D=0}
\]

**Procedure**

- Run **PMOSparsub.vi** with VSD = 3 V and VSD = 9 V. VDD (Chan0_out) starts at 2 V such that the minimum current is \(I_D\text{min} = (2 \text{ V} - V_{SG\text{min}})/R_S\). \(I_D\) stops automatically at \(I_D = 500 \mu\text{A}\) or Chan0_out = 10 V. Verify that the VI functions properly. **PMOSparsub.vi** will run as a subVI of the next VI.

**P3.6. PMOS Lambda from the Transfer Characteristic**

![Circuit Diagram]

**Components**
\[ R_S \approx \frac{7 \text{ V}}{I_{D_{\text{max}}}} \]

\[ |\text{Chan0}_\text{out}_{\text{max}}| = 10 \text{ V} \]

\[ |\text{Chan0}_\text{in}_{\text{min}}| = 3 \text{ V} \]

\[ I_{D_{\text{max}}} \approx 500 \mu\text{A} \]

**LabVIEW Computations**

\[ \lambda_p = \frac{\frac{k_p'(9 \text{ V})}{k_p'(3 \text{ V})} - 1}{9 - \frac{k_p'(9 \text{ V})}{k_p'(3 \text{ V})}} \]

\[ k_p = \frac{k_p'(9)}{1 + \lambda_p \cdot 9} \]
Procedure

- Run PMOSparam.vi to run subVI PMOSparsub.vi at VSD = 3 V and VSD = 9 V to resolve Lambda and final values of kp and Vtpo. Default and save the Front Panel to save the parameter values for the Mathcad results analysis file.

P3.7. PMOS Output Characteristic

Components

\[ R_D \approx \frac{|\text{Chan0\_out}_{\text{max}}| - |\text{Chan1\_in}|}{I_{D_{\text{max}}}} \]

\[ |\text{Chan0\_out}_{\text{max}}| = 10 \text{ V} \]

\[ |\text{Chan1\_in}| \approx 5 \text{ V at } I_{D_{\text{max}}} \approx 500 \mu\text{A} \]
LabVIEW Computations

Linear Region

\[ I_D = 2k_p \left( V_{eff} \frac{V_{SD}}{2} \left( 1 + \lambda_p V_{SD} \right) \right) \]

Active Region

\[ I_D = k_p V_{eff} \left( 1 + \lambda_p V_{SD} \right) \]

Procedure

- Install PMOS parameters from P3.6 into the Front Panel of PMOSoutput.vi. A given VSD sweep will halt at Chan0_out = 10 V. Set VSGstart(V) as necessary to obtain \( I_D \approx 100 \mu A \) for VSD in the active region. Verify that the measured data and SPICE calculation agree reasonably well. Write in your file path and save a data file for Mathcad. The file will contain the data points for the highest current output characteristic. Default Front Panel and save. These data will be used in the Mathcad analysis file.

- With the data defaulted and saved in the graph of the VI, a data file can be obtained at a later time. From the Diagram of PMOSoutput.vi, click on XYtoDataFile.vi, copy the data from PMOSoutput.vi, and paste it
into the Control Graph of `XYtoDataFile.vi`. Name the path and data file and run the VI. `XYtoDataFile.vi` is located in the User.lib in the LabVIEW folder. Therefore, it can also be opened from the Diagram of a VI under Functions>>User Libraries>>Dat_File.

### P3.8. PMOS Lambda

**LabVIEW Computations**

Straight-line curve fit from active region data:

\[ I_D = \text{Slope} \cdot V_{SD} + I_{Do} \]

\[ \lambda_p = \text{Slope}/I_{Do} \]

\[ k_p = I_{Do}/V_{effp}^2 \]

**Procedure**

- **Lambda.vi** is configured for Enable Data Base Access to read the data from `PMOSOutput.vi`. **Lambda.vi** can read all of the Front Panel information in `PMOSOutput.vi` when a log of the Front Panel has been obtained.

- From the Diagram of Lambda.vi, open `PMOSOutput.vi`. Obtain a data log of the Front Panel of the `PMOSOutput.vi` (under Operate Menu).

- **Run Lambda.vi** to read the graph of measured data (from `PMOSOutput.vi`) and to plot the measured data from the active region. The VI obtains \( k_p \) and \( \lambda_p \) from these data, for each of the voltage sweeps. Note that Lambda varies. Compare the average Lambda value with that from `PMOSParam.vi`.

- Click on **Call PlotID_VSD.vi** Green to bring up a plot of the active-region equation plot for \(-1/\lambda_p < V_{SD} < V_{SDmax}\), compared with the measured data. **Lambda.vi** will be used in the Mathcad analysis file.
Laboratory Project 4. Characterization of the NMOS Transistor for Circuit Simulation

P4.1 SPICE Parameters and Chip Diagram

P4.2 NMOS Transistor

P4.3 SPICE Equations

P4.4 NMOS Parameters from the Transfer Characteristic

P4.5 NMOS Lambda from the Transfer Characteristic

P4.6 NMOS Gamma SubVI

P4.7 NMOS Gamma

P4.8 NMOS Circuit with Body Effect

Exercises and Analysis Exercise04.mcd - Project04.mcd

P4.1. SPICE Parameters and Chip Diagram

SPICE PARAMETERS
### SPICE Name | Math Symbol | Description
--- | --- | ---
VTO | $V_{tno}, V_{tpo}$ | Zero VSB threshold voltage.
KP | $k_{n,p} = \frac{K_{p,n} W}{2 L}$ | Transconductance parameter.
GAMMA | $\gamma_n, \gamma_p$ | Threshold voltage parameter.
LAMBDA | $\lambda_n, \lambda_p$ | Active-region slope parameter.

**CD4007 Pin Diagram**

**P4.2. NMOS Transistor**

Use CD4007 pins 3 (gate), 4 (source) and 5 (drain). Connect pin 4 (source) to pin 7 (body). Connect PMOS body (pin 14) to the most positive node in the NMOS measurements, Chan0_out or ground, depending on the circuit. In the $\gamma_n$ measurement (`NMOSgamma.vi`) and the transfer characteristic measurement (`NMOS_Cir.vi`), pin 14 is connected to ground. Note that the NMOS of pins 6, 7, and 8 has internally connected body and source. This transistor is used in a following project.

**P4.3. SPICE Equations**

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D = k_n V_{effn}^2 (1 + \lambda_n V_{DS})$</td>
<td>Active region transfer characteristic and output characteristic ($V_{DS} &gt; V_{effn}$, $V_{SB} = 0$).</td>
</tr>
<tr>
<td>$V_{effn} = (V_{GS} - V_{tno})$</td>
<td>3.8</td>
</tr>
</tbody>
</table>
### SPICE Equation

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS} = \sqrt{\frac{I_D}{k'<em>n} + V</em>{tno}}$</td>
<td>3.12 Active-region equation solved for $V_{SG}$.</td>
</tr>
<tr>
<td>$k'<em>n = k_n (1 + \lambda_n V</em>{DS})$</td>
<td>3.14 Threshold voltage dependence on $V_{SB}$.</td>
</tr>
<tr>
<td>$V_{tn} = V_{tno} + \gamma_n \left( \sqrt{V_{SB}} + 2\phi_F - \sqrt{2\phi_F} \right)$</td>
<td></td>
</tr>
<tr>
<td>$X = \sqrt{V_{SB}} + 2\phi_F - \sqrt{2\phi_F}$</td>
<td>X variable for $V_{tn}$ versus X plot in $\gamma_n$ determination.</td>
</tr>
</tbody>
</table>

### P4.4. NMOS Parameters from the Transfer Characteristic

![Circuit Diagram]

**LabVIEW Computations**

- $k'_n = \frac{1}{\text{slope}(V_{GS}, \sqrt{I_D})^2}$
- $V_{tno} = f(V_{GS}, \sqrt{I_D})|_{I_d=0}$

**Components**
Procedure

- Set RS value. **Run NMOSparsub.vi** and adjust VSSinit for a minimum ID \( \approx 50 \ \mu A \). Test run **NMOSparsub.vi** with VDS = 3 V and 10 V. Execution halts at ID \( \approx 500 \ \mu A \). The VI runs as a subVI in the next part. **Default and save**. Saved VSSinit is used in the Top VI in the next part.

\[
R_S \approx \frac{7 \text{ V}}{I_{D_{max}}}
\]

\[
|\text{Chan1\_out}_{max}| = 10 \text{ V}
\]

\[
|\text{Chan1\_in}_{max}| = V_{GS_{max}}
\]

\[
I_{E_{max}} \approx 500 \ \mu A
\]
P4.5. NMOS Lambda from the Transfer Characteristic

Components

\[ R_S \approx \frac{7 \, \text{V}}{I_{D_{\text{max}}}} \]

\[ |\text{Chan1}_{\text{out max}}| = 10 \, \text{V} \]

\[ |\text{Chan1}_{\text{in max}}| = V_{GS_{\text{max}}} \]

\[ I_{D_{\text{max}}} \approx 500 \, \mu\text{A} \]

LabVIEW Computations

\[ \lambda_n = \frac{k_n'(10 \, \text{V}) - 1}{10 - \frac{k_n'(3 \, \text{V})}{k_n'(3 \, \text{V})}} \]

\[ k_n = \frac{k_n(10)}{1 + \lambda_n 10} \]
Procedure

- Set RS. Run NMOSparam.vi to obtain a set of NMOS parameters. The VI runs NMOSparsub.vi automatically with VDS = 3 V and VDS = 10 V. The sweep stops at ID $\approx 500\mu$A or $|\text{Chan0\_out}| = 10$ V. Default and save the VI.

P4.6. NMOS Gamma SubVI

Components
Note: \( V_{GS} \) will be larger with the body effect.

\[
R_S \approx \frac{\text{Chan1\_out\_max} - \text{Chan1\_in\_min}}{I_{D_{max}}}
\]

\[
\text{Chan1\_out\_max} = 10 \text{ V} \\
\text{Chan1\_in\_min} \approx 5 \text{ V} \\
I_{D_{max}} \approx 500 \mu\text{A}
\]

Procedure

- Note that PMOS body pin 14 and the NMOS drain terminal are at ground. Set \( R_S \) and \( V_{SSinit} \) from \textbf{NMOSparsub.vi}. Run \textbf{NMOSgamsub.vi} with \( VSB = 0 \text{ V} \) and 3 \text{ V} to verify that circuit is functioning properly. Note the change in the \( V_{GS} \) range for the larger \( VSB \). \( V_{SSinit} \) is adjusted automatically for larger values of \( VSB \), to obtain, approximately, a starting ID of about 50 \( \mu\text{A} \). \textit{Default and save} the Front Panel to save \( V_{SSinit} \).
P4.7. NMOS Gamma

Components

\[ R_S \approx \frac{5 \text{ V}}{I_{D_{\text{max}}}} \]

\[ |\text{Chan1\_out}_{\text{max}}| = 10 \text{ V} \]

\[ |\text{Chan1\_in}_{\text{max}}| \approx 5 \text{ V} \]

\[ I_{D_{\text{max}}} \approx 500 \mu\text{A} \]

LabVIEW Computations

\[ X = \sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F} \]

\[ \gamma_n = \text{Slope}(f(V_{on}, X)) \]
Procedure

- Set RS. With NMOSgamsub.vi open, run NMOSgamma.vi to obtain Gamma. Adjust $2\phi_F$ to try to match $V_{tno}$ (intercept, curve fit) with $V_{tno}$ ($V_{SB} = 0$, transfer characteristic, graph on right). Save the results.

**P4.8. NMOS Circuit with Body Effect**

**Components**

Use RS from NMOSgamma.vi.
Procedure

- Set RS. Install SPICE parameters from NMOSparam.vi and NMOSgamma.vi. Run NMOS_Cir.vi to obtain ID versus VGS with a sweep of VSS. The iteration solution obtained in SPICEgamma.vi (Diagram below) is compared in the graph of NMOS_Cir.vi. Adjust VSSinit to obtain IDmin of about 50μA. Re-adjust Gamma for best fit. Then save a data file with your data file name. The data file must be in the folder with the Mathcad file. The file name must have a *.prn extension.

- A file can be obtained from the graph of the defaulted and saved VI using XY1toDataFile.vi. The VI XY1toDataFile.vi is located in \LabVIEW 6\User.lib\Dat_Files\Dat.llb.

- Note that XY1toDataFile.vi is different from XYtoDataFile2.vi, as used to obtain a data file in the Diagram of NMOS_Cir.vi. The Control Graph
of \texttt{XYtoDataFile2.vi} accepts single plots while \texttt{XY1toDataFile.vi} is for graphs with two Y functions (with only one Y function in the data file). For convenience, a copy of \texttt{XY1toDataFile.vi}, \texttt{GetDataFile.vi}, is included in the Project04.llb. For clarification, \texttt{XY1Y2toDataFile.vi} accepts graph data with two Y functions and includes both in the data file.

**Laboratory Project 5. PMOS Common-Source Amplifier**

**P5.1 SPICE Equations and Pin Diagram**

**P5.2 PMOS Common-Source Amplifier DC Setup**

**P5.3 Amplifier Gain at One Bias Current**

**P5.4 Amplifier Gain versus Bias Current**

Exercises and Analysis Exercise05.mcd - Project05.mcd

**P5.1. SPICE Equations and Pin Diagram**

<table>
<thead>
<tr>
<th>CD4007 Pin Diagram</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D = k_p V_{eff} \left( \frac{V}{1 + \lambda_p V_{SD}} \right)$</td>
<td>\textbf{3.8} (NMOS)</td>
</tr>
</tbody>
</table>
CD4007 Pin Diagram

SPICE Equation | Description
--- | ---
\[
a_{\text{vo}} = -2\sqrt{\kappa_p I_D} \frac{R_D}{1+\lambda_p I_D R_D}
\] | 5.6 Gain versus I_D.

\[
a_v = -2 \frac{I_D}{V_{\text{effp}}} \frac{R_D}{1+\lambda_p I_D R_D}
\] | 5.7 Gain versus I_D, V_{\text{effp}}.

P5.2. PMOS Common-Source Amplifier DC Setup

LabVIEW Computations
\[ I_D = \frac{\text{Chan1\_in} - \text{Chan0\_out}}{R_D} \]

\[ V_D = V_{SS} - I_D R_D \]

\[ V_{SS} = \text{Chan0\_out} \]

**Components**

\[ R_D \approx \frac{6 \text{ V}}{I_{D_{\text{max}}}} \]

\[ |\text{Chan0\_out}_{\text{max}}| = 10 \text{ V} \]

\[ |\text{Chan1\_in}| = 4 \text{ V} \]

\[ I_{D_{\text{max}}} \approx 500 \mu\text{A} \]

\[ R_G > 500 \text{ k}\Omega \]

**Procedure**

- Install RD value. Adjust VSG in *SetVSD.vi* and **run** the VI to find the value for \( I_{D_{\text{MAX}}} = 500 \mu\text{A} \pm 50 \mu\text{A} \). VSS is ramped up from 10 V (default value) to find the value for \( V_D = -4 \text{ V} \). Note that if RD is too large, \( V_D \) will be \( > -4 \text{ V} \) initially (for \( V_{SS} = -10 \text{ V} \)) at \( I_{D_{\text{max}}} \). **Default and save** the Front Panel.
P5.3. Amplifier Gain at One Bias Current

LabVIEW Computations

\[ a_{vi} = \frac{\text{Chan1\_in\_acPeak}}{\text{VSG}/20} \]

Components

Same as SetVSD.vi

SubVI's

SetVSD.vi (Set Bias)
**FG1Chan.vi** (Function Generator)

**SR.vi** (Send-Receive Function)

**Oscilloscope.vi** (Chan1_in Read Waveform)

---

**Procedure**

- Sub VI **FG1Chan.vi** sends out the bias VSG and, in series, a sine-wave signal equal to $\frac{V_{SG}}{20}$. Set $V_{SGinit}$ as determined with SetVSD.vi as the VSG required to obtain $I_D \approx 500 \mu A$. This is the initial VSG in the sweep of the next part. **Run** the VI to obtain the gain for this bias current. Obtain a *data log* of the Front Panel. **Default and save**. **Re-run** with a new $V_{SGnew} = V_{SG} - 0.5 \text{ V}$ to obtain the gain at a lower bias current. Obtain a *data log*.

---

**P5.4. Amplifier Gain versus Bias Current**
LabVIEW Computations

\[ a_{vi} = \frac{\text{Chan1\_in}_{acPeak}}{VSG/20} \]

Components

Same as SetVSD.vi

Sub VI's

GainSub.vi

SetVSD.vi (Set Bias)

FGsine.vi (Function Generator)

SR.vi (Send-Receive Function)

Oscilloscope.vi (Chan1\_in Read Waveform)

Procedure
• **Run Gain.vi** to run GainSub.vi over a range of currents. Set VSGinit(V) to the value obtained above for ID ≈ 500 μA (defaulted in SetVSD.vi). The VI automatically halts (decreasing) at ID ≈ 50 μA. 
*Default and save the Front Panel. Now obtain a data file as follows.*

• Open GraphToDataFile.vi (copy of XYtoDataFile.vi) in Project05.llb. Copy the data from the graph ID versus VSG of Gain.vi. *(Right Click on the graph, then Data Operations>>Copy Data.) Then paste the data into the Control Graph of GraphToDataFile.vi. *(Right Click on the graph and then Data Operations>>Paste Data.) Type the data file path and name the data file. Run the VI to obtain a data file to be read by the Mathcad evaluation file. Repeat for the gain plot, av versus ID. Recall: The data files must be in the folder with the Mathcad file. The file name must have a *.prn extension.*

---

**Laboratory Project 6. PMOS Common-Source Amplifier Stage with Current-Source Biasing**

**P6.1 PMOS Schematic and Pin Diagram**

**P6.2 SPICE PMOS and Circuit Equations**

**P6.3 PMOS Current-Source Amplifier DC Setup**

**P6.4 Amplifier Gain**

**P6.5 Amplifier Frequency Response**

Exercises and Analysis Exercise06.mcd - Project06.mcd

**P6.1. PMOS Schematic and Pin Diagram**

CD4007 Pin Diagram

![CD4007 Pin Diagram](image)
## P6.2. SPICE PMOS and Circuit Equations

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_D = k_p V_{eff} V_{SD} \left(1 + \lambda_p V_{SD}\right)$</td>
<td>3.8 (NMOS) DC drain current – voltage relation (PMOS).</td>
</tr>
<tr>
<td>$a_v = -\frac{g_m R_D}{1 + g_m R_S}$</td>
<td>5.15 Midfrequency gain versus $I_D$.</td>
</tr>
<tr>
<td>$g_m \approx 2 \sqrt{k_p I_D}$</td>
<td></td>
</tr>
<tr>
<td>$a_v = -2 \sqrt{k_p I_D} \frac{R_D}{1 + \lambda_p I_D R_D}$</td>
<td>5.6 Midfrequency gain versus $I_D$ with bypass capacitor $C_s$.</td>
</tr>
<tr>
<td>$V_g = \frac{R_G}{R_G + R_S} \frac{1}{1 - \frac{1}{f g}} V_S$</td>
<td>6.1 Gate signal voltage, $V_g$, frequency-dependent relation to signal source, $V_s$.</td>
</tr>
<tr>
<td>$f_g = \frac{1}{2\pi (R_G + R_S) C_g}$</td>
<td></td>
</tr>
<tr>
<td>$a_v(f) = -g_m R_D \frac{1 + \frac{f}{f_2}}{1 + g_m R_S 1 + \frac{f}{f_2}}$</td>
<td>6.4 Gain frequency response with $C_s$ only ($C_g$ infinite).</td>
</tr>
<tr>
<td>$g_m = 2 \frac{V_{eff} I_D}{V_{SD}}$</td>
<td></td>
</tr>
<tr>
<td>$f_S = (1 + g_m R_S) f_2$</td>
<td></td>
</tr>
<tr>
<td>$f_2 = \frac{1}{2\pi R_S C_S}$</td>
<td></td>
</tr>
<tr>
<td>$f_{3dB} \approx \frac{g_m}{2\pi C_s}$</td>
<td>6.9 Approximate $f_{3dB}$ with $C_g$ infinite.</td>
</tr>
</tbody>
</table>
P6.3. PMOS Current-Source Amplifier DC Setup

Components

\[ V_{RS} = V_{SG} + I_D R_S = \text{Chan0\_out}/2 \]

\[ I_D \approx 300 \ \mu A \]

\[ \text{Chan0\_out} = 10 \ \text{V} \]

\[ R_D = R_S \approx \frac{\text{Chan0\_out}/2 - V_{SG}}{I_D}; \ V_{SG} \approx 2 \ \text{V} \]

\[ R_{G1} = R_{G2} > 500 \ \text{k}\Omega \]

\[ V_{SG} \text{ versus } I_D \text{ from Lab Projects 4,5.} \]

LabVIEW Computations

\[ I_D = \frac{\text{Chan0\_out} - \text{Chan0\_in}}{R_S} \]

Procedure

- Install your value of \( R_S \) in the Front Panel. Verify that VDD = 10V. Run DC.vi to verify your selection of \( R_S \approx R_D \). Goal is \( I_D \approx 300 \ \mu A \). Verify
that VG is about VDD/2. Default and save the Front Panel. Note that VSD is about 2VSG.

P6.4. Amplifier Gain

LabVIEW Computations

\[ C_g = \frac{1}{2\pi R_{Gg} f_g} \quad f_g = 1 \text{ Hz} \]
\[ R_G = R_{G1} \parallel R_{G2} \]
\[ C_s \approx \frac{g_m}{2\pi f_{3dB}} \quad f_{3dB} \approx 20 \text{ Hz} \]
\[ g_m = 2 \frac{I_D}{V_{SG} - V_{tpo}} = 2 \sqrt{k_p I_D} \]
Use **Project06.mcd** for calculations.

**SubVI's**

**FG1Chan.vi**

**SpecAnaly.vi**

**LabVIEW Computation**

\[ a_v = \frac{\text{Chan1_in} \text{acpeak}}{Vs(V)} \]

**Procedure**

- The SubVI of **Gain.vi, FG1Chan.vi**, sends out a signal with sine-wave peak Vs (Chan1_out). The first measurement is with only capacitor \( C_g \) installed. Be sure to conform to the capacitor polarity requirement. Set the Signal Frequency to 1000 Hz. Set your value of \( RS \) and check \( VDD = 10 \text{ V} \). **Run Gain.vi** to measure the gain. The gain should be less than 1 without the source bypass capacitor. A signal of \( Vs \approx 0.5 \text{ V} \) should thus suffice for good linearity and measurement precision.

- Now install the capacitor \( C_s \). Note that the source is at a positive voltage. Run the VI while setting Vs at various values. Adjust Vs until the
THD% (total harmonic distortion, %) is reduced to below about 5%.

- Continue to lower $V_s$ and run Gain.vi. Verify that the measured gain, $av$, is invariant for smaller values of $V_s$ except as eventually limited by DAQ resolution and noise. Find the largest $V_s$ (up to 5% THD), which is consistent with a constant gain measurement with increasing $V_s$.

- Run the VI again with a lower frequency (e.g., 800 Hz) to verify that the gain is not frequency dependent in this frequency range. Now default and save the Front Panel.

### P6.5. Amplifier Frequency Response

![Circuit Diagram]

**Procedure**

- The frequency of the input source voltage is swept from 1 to 1000 Hz to 1000 Hz. Set $V_s$ in FreqResp.vi as determined above for a valid voltage gain measurement. Open FG1Chan.vi to observe the waveform at the output.

- Set your value of $R_s$. Run FreqResp.vi without $C_s$. Recall that the gain will be less than 1. The frequency response is dictated by $C_g$ only. Verify that $f_{3dB}$ is about equal to or less than 1 Hz. Note that $f_{3dB} < 1$ Hz if the digital indicator $f_{3dB}$ indicates 1 Hz.

- Install $C_s$ and run the VI. Obtain a value for $f_{3dB}$. Default and save the Front Panel. Then use XYtoDataFile.vi to obtain a data file for the frequency response. A copy of the VI is in Project06.llb.
Laboratory Project 7. NMOS Common-Source Amplifier Stage with Source-Resistor Bias

P7.1 SPICE Equations and Pin Diagram

P7.2 NMOS Common-Source Amplifier DC Evaluation

P7.3 Amplifier Gain at Optimum Bias for Linear Output

P7.4 Optimum Bias Stability Test

P7.5 Amplifier Frequency Response

Exercises and Analysis Exercise07.mcd - Project07 1.mcd - Project07 2.mcd
P7.1. Chip Diagram and SPICE Equation

CD4007 Pin Diagram

<table>
<thead>
<tr>
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<tr>
<td>( I_D = k_n V_{eff}^2 \left( 1 + \lambda_n V_{DS} \right) )</td>
<td>3.8 (NMOS) Dc current – voltage relation.</td>
</tr>
<tr>
<td>( a_V = -\frac{g_m R_D}{1 + g_m R_S} )</td>
<td>5.15 Voltage gain versus ( I_D ).</td>
</tr>
<tr>
<td>( g_m \approx 2 \sqrt{k_n I_D} )</td>
<td>6.8 Corner frequency (( f_{3dB} )) with capacitor ( C_s ).</td>
</tr>
</tbody>
</table>

\[ a_{VO} = -2 \sqrt{\frac{k_p I_D}{1 + \lambda_p I_D R_D}} \]

\[ f_{3dB} = \sqrt{\frac{f_s^2 - 2 f_z^2}{2}} = \sqrt{\frac{1 + g_m R_S}{2}} - 2 f_z \approx f_s \]

\[ f_s = \left[ 1 + \frac{g_m + g_{ds} R_S}{1 + g_{ds} R_D} \right] f_z \]

P7.2. NMOS Common-Source Amplifier DC Evaluation

Procedure (Design)

- Start in the Mathcad file Project07.mcd to compute circuit component values as follows:
- We will design for a selected \( I_{Dmax} \) at \( Chan0\_out_{max} = 10 \text{ V} \) with \( V_{DSmin} \).
V. Select your $I_{D_{\text{max}}}$ in the range $100 \mu A < I_{D_{\text{max}}} < 500 \mu A$.

- Make $R_{G1} = R_{G2} \approx 100 \text{k}\Omega$. Thus, the gate voltage is

$$V_G = \frac{\text{Chan0\_out}_{\text{max}}}{2}.$$

- Select the circuit source resistor, $R_S$, to satisfy $V_G = V_{GS} (I_{D_{\text{max}}}) + I_{D_{\text{max}}} R_S$. $V_{GS} (I_{D_{\text{max}}})$ can be calculated using previously measured parameters or obtained graphically from, for example, NMOSparam.vi from Project 4.

- After acquiring a real $R_S$ (which is close to the calculated value), calculate an actual, new $I_{D_{\text{max}}}$ using the same equation in reverse with the real $R_S$. Neglect the change in $V_{GS}$.

- We will select $R_D$ to set the condition of $V_{DS_{\text{min}}} = 1 \text{V}$ (at Chan0\_out_{max}) from $R_D = (V_{DD} - V_{DS_{\text{min}}})/I_{D_{\text{max}}-} R_S$. (Use actual, new $I_{D_{\text{max}}}$.)

Procedure (Measurement)

- Install your value of $R_S$ in CSAMPBIAS.vi (for current sensing). With $V_{DD} = 10 \text{V}$ ($V_{DD_{\text{max}}}$), run the VI to verify the design. $V_{DS_{\text{min}}}$ can be significantly different from design 1 V due to parameter variation. For example, $1 < V_{DS_{\text{min}}} < 1.5 \text{V}$ is satisfactory, where the low limitation is based on $V_{DS_{\text{min}}} > V_{\text{effn}}$. This is the requirement to be in the active region. In the example, the design drain current is $I_{D_{\text{max}}} = 300 \mu A$.

- Verify that as $V_{DD}$ is reduced, ID decreases and VDS increases. Check $V_{DD} = 4 \text{V}$, the minimum in the sweep for parameter measurement of the next part. Verify that at the minimum $V_{DD}$, $VDS > ID\cdot RD$ Obtain a log for Chan0\_out = 10V.

- Reduce $V_{DD}$ from the maximum $V_{DD} = 10 \text{V}$ and determine,
approximately, the value between $4V < VDD < 10V$ that corresponds to \( V_{DS} \approx I_D R_D \). This is the operating point (bias) condition for the amplifier gain measurement. This will be found automatically in the gain measurement VI.

**P7.3. Amplifier Gain at Optimum Bias for Linear Output**
Components*

\[
C_s \approx \frac{g_m 10^{-6}}{2\pi f_{3\text{dB}}} \\
f_{3\text{dB}} \approx 10 \text{ Hz} \quad g_m = 2 \frac{I_D}{V_{\text{effn}}}
\]

Note that \( g_m \) is in \( \mu \text{A/V} \).

*Run the first part of Procedure with GainNMOS.vi, below, without the capacitor, to obtain \( V_{\text{effn}} \) and bias \( I_D \), for computing \( g_m \).

**LabVIEW Computations**

Parameters: \( V_{\text{tno}} \), \( k_n \)

\[
a_{\text{avg}} = \frac{\text{Chan0\_inpeak} / V_s}{1 - \text{Chan2\_inDC} / \text{Chan0\_out}} \\
R_GZ / (R_G1 + R_G2) = \frac{\text{Chan2\_inDC}}{\text{Chan0\_out}}
\]
Procedure (Obtain Parameters and Bias Variables)

- Open **GainNMOS.vi**. Install your $R_S$ value. Without the capacitor installed, set the Mode Switch to Param (red, switch in logic state 0). **Run** the VI for a VDD sweep to get the parameters. (Note: The sweep rate is configured to be slow in case the capacitor is in place during the sweep.) The VDD sweep is from 4 V to 10 V. Obtain a log of the results.

Procedure (Gain Measurement)

- In the Param mode, the VI finds and indicates VDDbias corresponding to the optimum $V_{DS} = (V_{DD} - V_{RS} + V_{effn})/2$. This permits maximum signal swing without distortion. Set the indicated value of VDDbias into the Set VDD Digital Control. **Run** the VI with the Mode Switch set to Gain (green, switch position logic 1) without the capacitor. Obtain a log of the Front Panel. **Default and save** the Front Panel.

- At the end of the parameter sweep, $V_{effn}$ is indicated for VDDbias. The value is retained in the Digital Indicator in the gain measurement. The value of ID indicated in the gain measurement is the amplifier gain bias value. Use $V_{effn}$ along with bias ID, to compute $g_m$ and thus $C_s$. Use Project07.mcd for the calculation.

- **Install** the capacitor. Make certain that the polarity of the capacitor is correct. Check that the Mode Switch is set to Gain (switch position logic 1). Check that the value of VDDbias matches the value in Set VDD Digital Control. The VI will measure the gain at this one VDD setting (optimum for distortion-free output). The signal frequency is initially 500 Hz.

- **Run** the VI and vary the value of $V_s$ to determine that the gain result, $V_d/V_s$, is not affected by changes, that is, by distortion. **Default and save** the Front Panel. Obtain a log of the results. Also, run with slight variations in Freq (e.g., 300 Hz). Note that the parameter values are preserved when running the gain mode. Parameter, bias variable, and gain data are required for the project Mathcad file.

P7.4. Optimum Bias Stability Test

- As will be explored in a project Mathcad file, the basis stability computation is performed here with LabVIEW. Recall (Section 5.5) that this takes into consideration a possible range of $V_{tno}$ and $k_n$ values. Here, an analysis is made regarding the extent to which your design is optimum in terms of bias stability. Note that this is separate from the
maximum signal condition that has been included in the design.

- Open CalVDS optimum.vi. In the Digital Controls, set your values for VDD, kn, Vtno, and ID. ID is the nominal value of the design for the nominal values of the parameters. Your value of ID, along with your parameter values, will be assumed to be, for this evaluation, the nominal values. The computation holds the bias current constant at the design value (as entered into the Front Panel). As VG is increased (X axis), the added increment of VG is the added drop across the new RS, for a given new VG. Run the VI.

- Verify that the value of VGS in the top Digital Indicator matches reasonably well your measured value (Front Panel of GainNMOS.vi). This SPICE computation uses your measured parameter values and ID. The values should be consistent.

- The top graph is its VDS limits versus VG. The center (dashed) curve is for your parameters. The downward slope reflects the increasing drop across VG. The top and bottom plots are for the two extremes of VDS that occur for the worst case of the combination of the limits of kn and Vtno. The computation is for Vtno ± = Vtno ± 100 mV and knz = kn ± 100 μA/V². The same optimum signal level condition as used in your design is maintained throughout.
- The lower graph contains plots of the output signal limiting values. The best combination of bias stability and signal level is at the peak of these curves.

- Step through the RS Array Digital Indicator to locate your RS and the associated index. Then determine the corresponding VG and RD (same index). The value of RD should match your design value. The value of VG should match the value from the Front Panel of GainNMOS.vi.

- Locate your value of VG on the X-axis of the two graphs. If it falls in the range of values surrounding the peaks, the circuit is optimized both in terms of signal limits and bias stability. Note that bias stability was not taken into consideration in the design. In the design, though, often a given criterion serves as the basis and the design may then be evaluated for other criteria.

P7.5. Amplifier Frequency Response

Procedure

- In FreqRespNMOS.vi, the frequency of the with source voltage (sine-wave Chan1_out) is swept from 1 to 1000 Hz. Chan2_in should be disconnected to reduce the stray capacitance at the gate. In the Front Panel of the VI, set VDDbias and Vs at the values determined in the gain measurement with GainNMOS.vi.
Along with `FreqRespNMOS.vi`, open `FG1Chan.vi` to observe the output waveform. Verify that $C_s$ is installed and run the VI to obtain a value for $f_{3dB}$.

Open, from the Diagram of `FreqRespNMOS.vi`, Frame 2, `XYtoDataFile2.vi`. Run `FreqRespNMOS.vi` again, with the data mode switch set to Green (logic stage 1), to obtain a data file of the frequency-response plot in `XYtoDataFile2.vi`. (Note that with the data VI open, the data are transferred to the VI and can then be saved in the VI.) The data file is used in the Mathcad project file. Default and save the Front Panels of both `XYtoDataFile2.vi` and `FreqRespNMOS.vi`. Note the maximum index for the Mathcad file. The $f_{3dB}$ result will differ from the design, as the design was based on the simple form. This will be explored in the Mathcad file.

A data file can be obtained later from the saved data in the graph of `FreqRespNMOS.vi`, with `XYtoDataFile2.vi`. As noted above, the data file VI can be obtained from the Diagram of `FreqRespNMOS.vi`. The data file VI is located in `Dat.lib` in the `User.lib` folder (Program Files>>National Instruments>>LabVIEW 6). The VI can also be accessed from the menu sequence in `FreqRespNMOS.vi`, Browse>>Show VI Hierarchy, and open the data file VI from the Hierarchy Window.

Return to Project07.mcd.
Laboratory Project 8. NMOS Source-Follower Stage

P8.1 SPICE Equations and Pin Diagram

P8.2 Source-Follower DC Evaluation

P8.3 Source-Follower Voltage Transfer Relation

P8.4 Source-Follower Voltage Transfer Relation with Body Effect

Exercises and Analysis Exercise08.mcd - Project08.mcd

### P8.1. SPICE Equations and Pin Diagram

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in} = V_{tn0} + \gamma_n \left( \sqrt{V_{SS} + \frac{2\phi}{\sqrt{2\phi}}} \right)$</td>
<td>7.1 Threshold voltage for $V_B = V_{SS}$.</td>
</tr>
<tr>
<td>$a_v = \frac{g_m}{g_m + \frac{1}{R_s} + g_{ds}}$</td>
<td>7.7 Source-follower voltage-transfer relation with $V_{sb} = 0$.</td>
</tr>
<tr>
<td>$a_v = \frac{g_m}{g_m(1 + \eta) + \frac{1}{R_s} + g_{ds}}$</td>
<td>7.12 Source-follower voltage transfer relation with body effect.</td>
</tr>
<tr>
<td>$g_{mb} = \eta g_m$, $\eta = \frac{\gamma_n}{2\sqrt{V_{SB} + 2\phi_F}}$</td>
<td>4.11 Body-effect transconductance.</td>
</tr>
</tbody>
</table>

CD4007

**Do not connect pin 14.**

[Diagram of CD4007 NMOS Source-Follower Stage]
P8.2. Source-Follower DC Evaluation

Pin 14 must not be connected. Chan0_out will be plus and minus and the drain is at ground.

Components

For Gain.vi

\[ I_{D_{\text{max}}} \approx 500 \mu A \quad |\text{Chan1}_\text{out}_{\text{max}}| = 10 \text{ V} \]
\[ V_{G_{\text{Smax}}} \approx 5 \text{ V} \]
\[ R_S \approx \frac{|\text{Chan1}_\text{out}_{\text{max}}| - |V_{G_{\text{Smax}}}|}{I_{D_{\text{max}}}} \]

Note that with \( R_S \) is selected for the condition of maximum body-effect (\( V_{G_{\text{Smax}}} \approx 5 \text{ V} \)), \( I_{D_{\text{max}}} > 500 \mu \text{A} \) for the case without body effect. The current sweep VI's halt at \( I_D = 500 \mu \text{A} \).

Procedure

- In the Front Panel of DCcheck.vi, set the value of RS in the Digital Control. With VSS (magnitude) set at 10 V, run the VI to verify the dc design. Note that \(|V_S|\) is equal to the VGS magnitude. Verify that \( I_D > 500 \mu \text{A} \) for this case of no body effect.
P8.3. Source-Follower Voltage Transfer Relation

Pin 14 must not be connected to ground. Chan0_out will be greater than 0 for the positive signal.

LabVIEW Computation

Procedure

- GainSF.vi measures the gain (transfer relation) of the circuit over a
range of drain current. Parameters Vtno and knprime are obtained from the ID sweep. Vtno is used in the voltage transfer-relation calculation as plotted along with the measured data.

- Open GainSF.vi and install your value of RS. Open FG1Chan.vi to observe the waveform at the output. Run the VI and verify that the curves match reasonably well as in the example. Adjust the magnitude of VSS to obtain a minimum ID of about 50 μA.

- Adjust the value of Vs while rerunning the VI. Use the largest Vs without distortion. Large-signal distortion is manifested by a poor curve fit, particularly at the low end of the current range.

- Default and save the Front Panel. The value obtained for knprime must be available for the next VI. It is used in the calculation of 

\[ g_m = \frac{2}{\sqrt{\text{nprime}T_D}} \]

. The alternative form, \( g_m = 2I_D/V_{effo} \), is used in the calculations for this VI.

- Obtain a data file of the plot using XY1ToDataFile.vi.

**P8.4. Source-Follower Voltage Transfer Relation with Body Effect**
Pin 14 must not be connected to ground. Chan0_out will be greater than 0 for the positive signal.

**LabVIEW Computation**

\[
\begin{align*}
\text{gm} &= 2 \times \text{sqrt}(\text{knprime} \times \text{ID}); \\
\text{gmb} &= \text{gn} \times \text{gm} / (2 \times \text{sqrt}(\text{VRS} + \text{phi})); \\
\text{av} &= \text{gm} / (\text{gm} + \text{gmb} + 1 / \text{RS});
\end{align*}
\]

**Procedure**

- Move the body pin connection as in Circuit P8.2. In **GainBE.vi**, install a first-guess value for \(\gamma_n\) (**Project 4**). Install the value of knprime, obtained from the Front Panel of **GainSF.vi**. Run the VI and readjust \(\gamma_n\) for the best fit. Adjust |VSS| init for a minimum ID of about 50 \(\mu\text{A}\). Note the reduced value of the voltage transfer relation (gain).

- Open **Compare.vi** from **Project08.llb**. Paste the results from the graphs of the plots for with and without body effect into the control graphs. Run the VI to compare the results.

- Use **XY1ToDataFile.vi** to obtain a data file of the plot in **GainBE.vi**.

**Laboratory Project 9. MOSFET Differential Amplifier Stage**

**P9.1 SPICE Equations and Pin Diagram**
P9.2 DC Evaluation of the Single-Power-Supply Differential Amplifier

P9.3 Determination of the PMOS Parameters

P9.4 Amplifier Gain Measurement

P9.5 Transistor Parameters and DC Imbalance

P9.6 Common-Mode Gain Measurement

Exercises and Analysis Exercise09.mcd - Project09.mcd

**P9.1. SPICE Equations and Pin Diagram**

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a_{v1} = \frac{-g_{m1}R_{D1}}{(R_{D1} + R_s)g_{ds1} + (1 + g_{m1}R_s)} )</td>
<td>8.34 Inverting gain.</td>
</tr>
<tr>
<td>( a_{v2} = a_{vs}a_{vcg} = \frac{g_{m1}R_s}{(R_{D1} + R_s)g_{ds1} + (1 + g_{m1}R_s)} \frac{(g_{m2} + g_{ds2})R_D}{1 + g_{ds2}R_D} )</td>
<td>8.40 Noninverting gain.</td>
</tr>
<tr>
<td>( R_s = \frac{R_{bias}}{R_{is2}} ) ( R_{is2} = \frac{1 + g_{ds2}R_D}{g_{m2} + g_{ds2}} )</td>
<td>8.38 Signal resistance at source node.</td>
</tr>
</tbody>
</table>

**CD4007**

![Diagram of CD4007 circuit](image)

**PMOS 1**
- Pin 1
- Pin 6
- Pin 13

**PMOS 2**
- Pin 11
- Pin 10
- Pin 12
P9.2. DC Evaluation of the Single-Power-Supply Differential Amplifier

Components

\[ R_{D1} = R_{D2} = R_D \]
\[ R_s = R_D/2 \]
\[ V_D \approx V_{DD}/2 - V_{SG} \]

For \( \text{Chan0\_out} = 10 \text{ V} \):

\[ 100 \mu A < I_D < 400 \mu A \]

(Choose One)

\[ R_G < 100 \text{ k}\Omega \]
Match the gate resistors on each side to obtain $V_G = V_{DD}/2$. On a given side, the resistors must be equal, but can be different on opposite sides.

**Procedure**

- After completing the circuit connections, open **DC.vi**. Set Chan0_out = 10 V and run the VI. **DC.vi** scans Chan1_out to balance the circuit (i.e., to set $V_{D1} = V_{D2}$ within 20 mV). Try Chan0_out in the range 5 to 10 V. Verify that $100 \mu A < ID < 400 \mu A$ (your design) with maximum Chan0_out = 10 V.

- Note the value sent out by Chan1_out. This should be only mV if the gate resistors were selected properly.

- Verify that VSD is roughly $2V_{SG}$. Default and save the Front Panel with Chan0_out = 10 V. The VI serves as a subVI in the next part to bias and balance the circuit.
P9.3. Determination of the PMOS Parameters

Procedure

- **Parameters.vi** sweeps output channel Chan0_out from $V_{DD} - 1$ to $V_{DD} + 1$ (where the design bias $V_{DD}$ is set in the Front Panel). The gain measurement will be made at $V_{DD}$, intermediate to the sweep range. Since voltage $V_{SD}$ is approximately equal to $2V_{SG}$, $V_{SD}$ will be relatively constant during the sweep, as is required for a reliable measurement of $K_p$ and $V_{tpo}$.

- **Run** the VI for VDD set at 6 V and 8 V and verify that $V_{tpo}$ is close to the same for both VDD values. For the larger VDD (and VSD), $k_p$ (at VSD) should be slightly larger.

- Now set VDD = 6, 7, or 8 V and the File Mode switch to Green (on) and re-run to obtain a parameter data file. The file has $R_{D1}$, $R_{D2}$, $k_p$. 

![Parameters.vi](image)
(technically, $k^*_P$) and $V_{tpo}$. The Parameters are actually for $M_2$. These will be read by the evaluation Mathcad file.

- The parameters can be obtained with SimParam.vi from the data saved in Parameters.vi. Paste the data from the Indicator Graph (sample, $VDD = 7$ V) of Parameters.vi into the Control Graph of SimParam.vi and run the VI with the Data Mode switch set to on (Green).

**P9.4. Amplifier Gain Measurement**

**Procedure**

- Gain.vi runs DC.vi to set up the bias and balance the circuit. It then sends out a signal squarewave and reads the response at the two outputs. Gain is calculated as output voltage divided by $V_g/2$. The 1/2 accounts for the voltage divider of the two gate resistors.
- Set in Chan0_out (V_DD), which you selected above in Parameters.vi. Run Gain.vi to obtain the gain at the two outputs. Adjust Vs for an output voltage magnitude similar to that in the example.

- Now run AvgGain.vi with your V_DD (Chan0_out) and Vs from Gain.vi. as a subVI repeatedly and averages the gains continuously during the measurements. With the Run Mode on (Green), allow the VI to continue to run until the average gain no longer appears to be changing. Reset Run Mode to halt execution.

- Repeat with the File Mode button set to on (Green). The data file contains I_D1, I_D2, V_SG, V_SD, a_v1, and a_v2. The Mathcad evaluation file will read these data.

- Use SimAvgGain.vi to obtain the data file from the data saved in AvgGain.vi. Paste graph data and copy and paste the Digital Control values. Gains will be obtained from the graph data and need not be copied from the Digital Indicators.
P9.5. Transistor Parameters and DC Imbalance

Procedure

- **Sweep.vi** runs a special version of **DC.vi, DCimbal.vi**, as a subVI of **Sweep.vi**. **Sweep.vi** sends out a range of bias voltage, $5 \, \text{V} < V_{\text{DD}} < 10 \, \text{V}$ (Chan0_out), in 0.5 V steps. $V_{\text{SG}}$, $I_D$, and $I_{D2}$ are measured at each step. A three-column data file is saved for the Mathcad project evaluation.
Note that Circuit P9.2 has the gates connected to make certain that the gate voltages are equal. There is no balancing in this circuit, as the goal is to study circuit imbalances. DCimbal.vi calls for Chan1_out = 0 V.

- Open Sweep.vi and set in the resistor values. Also open DCimbal.vi. Run DCimbal.vi to verify that the circuit is functioning properly.

- Run Sweep.vi. Set the File-Mode switch to on (Green), write in the file path (or click on the Browse button) and data file name and run the VI to obtain the data file. The data dc variables will be used in the project Mathcad file to obtain kp and Vfpo. The values are used in a computation for a graphical comparison of measured and computed current ratios versus drain current.

- Run SweepSim.vi to obtain the data file from the graph data saved. [Note that the VSG graph is not shown in the sample Sweep.vi (above). The actual Sweep.vi has a Front Panel as the sample SweepSim.vi (below).] Copy and paste data from Sweep.vi.

Procedure

- The common-mode gain can be obtained directly with Circuit P9.2. This is accomplished with the VI, CBGain.vi. The squarewave input signal is applied with Chan1_out.
• Open **CMGain.vi** and set in the resistor values. Set Vs to a larger value than that used in **Gain.vi**, to compensate for lower gain. **Run** the VI to verify that the circuit is functioning properly. Expect the gain to be about unity, based on the design Rs = R_D/2. (Ideal common-mode gain is zero.)

• Open and **run AvgCMGain.vi**. Obtain a data file consisting of drain currents, V_SG, gains, and V_SD.

• Use **SimAvgGain.vi** to obtain a data file from data saved in **AvgCMGain.vi**. Copy and paste the graph data and the drain currents, V_SG and V_SD. Gains will be averaged from the graph data.

---

**Laboratory Project 10. Current Mirror and Common-Source Amplifier with Current-Source Load**

**P10.1 SPICE Equations and Pin Diagram**

**P10.2 Evaluation of the Current-Source Circuit**

**P10.3 Evaluation of the Mirror-Current Circuit**

**P10.4 Evaluation of the Bias Setup**

**P10.5 Measurements of the Amplifier Gain versus Bias Current**

Exercises and Analysis Exercise10.mcd - Project10.mcd

**P10.1. SPICE Equations and Pin Diagram**

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### SPICE Equation

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( a_v = \frac{2}{(\lambda_n + \lambda_p) V_{\text{effn}}} )</td>
<td>( V_{\text{effn}} = V_{\text{GS}} - V_{\text{no}} )</td>
</tr>
<tr>
<td>( a_v \approx \frac{2}{\lambda_n + \lambda_p} \sqrt{\frac{k_{nn}}{I_{D1}}} )</td>
<td>( k_{nn} )</td>
</tr>
</tbody>
</table>

### Figure

- **PMOS3**
  - Pin 14
  - Pin 6

- **PMOS2**
  - Pin 11
  - Pin 10

- **NMOS1**
  - Pin 5
  - Pin 7

### P10.2. Evaluation of the Current-Source Circuit

**Power Supply = 5 V**
**Pin 14 on Conn. B lock**

**Circuit P10.1**

**Components**

- \( I_{D\text{max}} \approx 500 \mu A \)
- \( \text{Chan0\_out\_min} = -10 \text{ V} \)
- \( R_{\text{Ref}} \approx \frac{5 \text{ V} - V_{\text{SG3}} + 10 \text{ V}}{I_{D\text{max}}} \)

**Procedure**

- Set your value of RRef in the Digital Control. **Run RefCurrent.vi** to determine the current range. Chan1\_out is swept from the Initial value to \( \approx -10 \text{ V} \). Readjust Initial Chan1\_out to obtain a minimum drain current.
of about 50 μA. Verify that the maximum current is about 500 μA.

P10.3. Evaluation of the Mirror-Current Circuit

- Install the additional circuit components, which form the current source. Set your resistor values in the Digital Controls. Use Initial Chan0_out from RefCurrent.vi. Run MirrorCurrent.vi to assess the mirror current (current-source current). Chan0_out is swept from the Initial value to \(-10\) V. Chan1_out is varied downward to maintain \(V_{SD2} = V_{SD3}\). Any difference between the currents indicates a difference in transistor parameters of \(M_2\) and \(M_3\).

Components
P10.4. Evaluation of the Bias Setup

SetVolID.vi sends out the gate voltage of the driver transistor (M1, NMOS) and then sweeps Chan1_out to set the output bias voltage (Chan1_in) at VDD/2. This VI is a subVI in the gain measurement VI (below, next part). To run this VI as a top VI, set the Index to zero. Set Chan0_out Initial to 0V.
- Run `SetVoID.vi` while adjusting $V_{GS}$ for the lowest value of the $I_D$ range of about 50 $\mu$A. Verify that the bias-setting circuit functions properly. Adjust the Control-Loop Constant to obtain a final dc value convergence rate similar to that in the example. Default and save the Front Panel.

**P10.5. Measurement of the Amplifier Gain versus Drain Current**

**Procedure**

- In `Gain.vi`, set $V_{GS1}$ Initial to the value from the evaluation of `SetVoID.vi` above. The VI will sweep $V_{GS1}$ over a range to include a maximum response of about 500 $\mu$A, according to the design above. Due to the high gain, the input signal voltage will be small in terms of the DAC. A subVI computes the actual output signal voltage from the value requested. The value computed is used in the gain computation.
• Open SetVoID.vi along with Gain.vi. Set all numbers in the Digital Controls of Gain.vi. Run the VI and adjust Vs such that Vo min and Vo max are confined between 1 and 4 V, as in the example. These are indicated for the initial bias current (highest gain). Also, adjust (down) the Control-Loop Constant of SetVoID.vi if the bias setting function oscillates out of control. Save the Front Panel when the VI is functioning properly.

• Open AvgGain_ID.vi. This VI runs Gain.vi as a subVI repeatedly and averages the plots of each execution. Set the Run Mode switch to Continuous and the File Mode switch to on (Green) and run the VI for data smoothing. Switch to One Plot to halt the execution. The data file includes gain, VGS1, and ID. This is used in the project Mathcad analysis file.

• Obtain a data file from saved data in AvgGain_ID.vi with SimAvgGain_ID.vi.
Laboratory Project 11. Operational Amplifier with Resistor Feedback

P11.1 SPICE Equations

P11.2 Bias Circuit Setup

P11.3 Opamp Offset Voltage

P11.4 Evaluation of the Bias Balancing Circuit

P11.5 Evaluation of the Gain and Signal Limits with Swept Input

P11.6 Evaluation of the Gain with Sine-Wave and Square-Wave Signals

P11.7 Determination of the Opamp Frequency Response

Exercises and Analysis Exercise11.mcd - Project11.mcd

P11.1. SPICE Equations

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_O = \frac{-A_{vNI}}{1 + A_{vNI}} V_{off} \approx -A_{vNI} V_{off}$</td>
<td>11.16 Output voltage of resistance-feedback opamp with offset voltage, $V_{off}$.</td>
</tr>
<tr>
<td>$A_v = \frac{A_{vNI}}{1 + A_{vNI} \frac{R_f}{R_y}}$</td>
<td>11.3, 11.4 Midfrequency gain dependence on opamp gain $a_v$.</td>
</tr>
<tr>
<td>$A_v(f) = \frac{A_{vNI}}{1 + A_{vNI} \frac{1}{a_v} \frac{1}{f_{BW}}} = \frac{A_v}{1 + A_v \frac{1}{f_{BW}}}$</td>
<td>11.20 Frequency-response function of resistance-feedback opamp amplifier.</td>
</tr>
<tr>
<td>$f_{BW} = f_{3dB} \left(1 + \frac{a_v}{A_{vNI}}\right) = f_{3dB} \left(1 + a_v \frac{R_y}{R_y + R_f}\right)$</td>
<td>11.21 Bandwidth (corner frequency) of opamp amplifier with opamp open-loop corner frequency, $f_{3dB}$.</td>
</tr>
</tbody>
</table>
P11.2. Bias Circuit Setup

1 Offset Null 1
2 Invert. Input
3 Non-Invert. Input
4 V-
8 ISET
7 V+
6 Output
5 Offset Null 2

Components
Procedure

- Do not initially turn on the power supply. Connect the circuit after having made precision measurements of the resistors. Turn on the power supply only with the circuit completely connected, Install the resistor value RSET in the Digital Control of DCCheck.vi. Run the VI. Check the dc values. Verify that ISET is roughly 25μA VO is normally close to V+ or V−. Default and save the Front Panel.
P11.3. Opamp Offset Voltage

Components

\[ R_f \approx 4 \times 10^3 R_2 \]

(Very Approximate)

\[ A_{\text{VNI}} \approx 4000 \]

\[
V_{\text{off}} = -\frac{A_{\text{VNI}}}{a_{\text{VO}}} V_O 
\]

(11.16)

\[ A_{\text{VNI}} \approx 1 + \frac{R_f}{R_2} \approx \frac{R_f}{R_2} \]

Procedure

- Install \( R_f \) and re-run DCCheck.vi. Verify that \(|V_O|\) is less than the value without the feedback resistor. If not, use a smaller \( R_f \). Default and save the information in the Front Panel.

Datasheet Offset Voltage

<table>
<thead>
<tr>
<th></th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{\text{io}}</td>
<td></td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>( V_o = 1.4 \text{ V}, V_{\text{ic}} = 0 \text{ TS271C/I/M} )</td>
<td>1.1</td>
<td>10</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
P11.4. Evaluation of the Bias Balancing Circuit

Components

\[ R_1 = R_3 \]

\[ \frac{R_1}{R_2} = \frac{R_3}{R_4} = 1000 \]

\[ R_f \approx 4000R_2 \]

![Circuit Diagram](image)

Procedure

- Connect the additional circuit components, \( R_1 \) and \( R_3 \). (Gain measurement results depend on the precision of the values entered.) The VI will sweep Chan1_out to drive the output to near 0 V. Set the value of \( R_f \) in the Digital Control of \textit{IterateVo.vi}. 

  ![IterateVo.vi](image)

- **Run** the VI to verify that the balancing circuit is functioning properly. The VI, \textit{IterateVo.vi}, is a subVI in the amplifier gain evaluations, for balancing the circuit (i.e., for setting the dc output to near 0 V). The indicated \( VO(init) \) should match the value from the result of P11.3. **Save**
P11.5. Evaluation of the Gain and Signal Limits with Swept Input

**Procedure**

- Enter the resistor values in the Digital Controls of `ScanAmp.vi`. The gain of interest is amplifier gain, $A_v = \text{Chan0\_in}/V_+$. This is obtained from the measured Slope of $n \text{ Chan0\_in}$ versus $\text{Chan0\_out}$ and then

  $$A_v = \frac{R_4 + R_3}{R_4} \cdot \text{Slope}$$

- Opamp gain, $a_{vo}$, is calculated in a Formula Node using $A_v$ and the ideal gain $A_{vNI} = 1 + R_f R_2 || R_1$. Thus, the gain-measurement results depend critically on the precise value of the resistors.

- Run the VI and reset $\text{Chan0\_out}$ Range as necessary to obtain an output range of about plus and minus 1 V [graph Y axis and Indicators, $V_{\text{max}}(V)$ and $V_{\text{min}}(V)$]. Save the Front Panel.
Reset the Chan0_out Range, such as in the example (left), to drive the output to the limits. Run the VI and note the limits Vomax(V) (VOH) and Vomin(V) (VOL). Compare these with the datasheet values.

Note that the datasheet numbers (below) were obtained for a single power supply and V+ = 10V and V− = 0V. Thus, Vomax approximately 1 V below the power supply and Vomin is approximately 50 m above the negative supply (ground in the datasheet case and −8 V for our opamp amplifier).

**Datasheet Limit Voltages (Power Supply = 0 to +10V)**

<table>
<thead>
<tr>
<th></th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
</table>

---

Formula Node Computation of avo

\[
\begin{align*}
Av &= \text{Slope}(R3+R4)/R4; \\
R_{\text{par}} &= R2^*R1/(R2+R1); \\
Av_{\text{NI}} &= 1+R_{\text{NI}}/R_{\text{par}}; \\
avo &= Av_{\text{NI}}/(Av_{\text{NI}}/Av-1)/1000; \\
\end{align*}
\]
V<sub>OH</sub> | High-level output voltage | V
--- | --- | ---
Vid = 100 mV, RL = 100 kΩ | 8.7 | 8.9
V<sub>OL</sub> | Low-level output voltage (Vid = –100 mV) | 50 mV

**P11.6. Evaluation of the Gain with Sine-Wave and Square-Wave Signals**

**Procedure**

- **SignalAmp.vi** sends out a sine- or square-wave input signal with a frequency as selected from the Front Panel. Use a frequency of 1 or 2 Hz. It must be low as the frequency response of the amplifier is very low with the high gain of this configuration.

- Install resistor values in the Front Panel of **SignalAmp.vi.Run** the VI and compare the gain for sine- and square-wave signals. Compare for two different frequencies. Adjust Vs for a maximum output signal of
about 1 V. Save the Front Panel.

**Datasheet Large-Signal Voltage Gain**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avd</td>
<td>Large-signal voltage gain</td>
<td></td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td></td>
<td>Vo = 1 to 6 V, RL = 100 kW, Vic = 5V</td>
<td>30</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Tmin. &lt; Tamb. &lt; Tmax.</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**P11.7. Determination of the Opamp Frequency Response**

**Procedure**

- The VI sweeps the input sine-wave signal over a range of frequencies, 1Hz<f<1kHz. The gain is computed and plotted and the bandwidth of the amplifier is computed and indicated. The GBP is then computed and indicated.
- Install precision resistor values for R3 and R4 in the Front Panel of *FreqResp.vi*. Run the VI to obtain the frequency response. Verify that Vo(max) is less than about 1 V. This must less than the oscilloscope limit of 2 V. Save the Front Panel.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBP</td>
<td>Gain – Bandwidth product (Av = 40 dB, RL = 100 kΩ, CL = 100 pF, fin = 100 kHz)</td>
<td>0.7</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>

**Laboratory Project 12. Operational Amplifier Integrator and Oscillator**

**P12.1 SPICE Equations**

**P12.2 Opamp Integrator**

**P12.3 Opamp Oscillator**

Exercises and Analysis Exercise12.mcd - Project12.mcd

**P12.1. SPICE Equations**

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2V_{peak} \approx \frac{V_s}{R_yC_f} \frac{T}{2}$</td>
<td>12.4 Opamp-integrator peak voltage amplitude of the triangular-wave for applied square-wave with peak $V_s$ and period $T$ and with $R_y = R_1</td>
</tr>
</tbody>
</table>
### SPICE Equation

<table>
<thead>
<tr>
<th>Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ v_o(t) = V_s \sin\left(2\pi \frac{t}{T}\right) + \frac{T}{2\pi R_y C_f} V_s \cos\left(2\pi \frac{t}{T}\right) ]</td>
<td>Cosine-wave output for sinewave input with peak ( V_s ), period ( T ), ( R_y = R_1</td>
</tr>
</tbody>
</table>

\[ T \approx 2.2 R_f C_o \]  
12.26 Period of oscillator for \( R_f \) with \( C_o \) and \( R_1 = R_3 \).

\[ T_{\text{plus}} = R_f C_o \ln \left( \frac{V_{\text{op}} + \frac{R_3}{R_3 + R_1} V_{\text{om}}}{\frac{R_1}{R_3 + R_1} V_{\text{op}}} \right) \]  
12.18 General form for \( T_{\text{plus}} \) in terms of \( R_1 \), \( R_3 \), \( V_{\text{om}} \), and \( V_{\text{op}} \).

\[ T = T_{\text{plus}} + T_{\text{minus}} \]

\[ T_{\text{minus}} = R_f C_o \ln \left( \frac{V_{\text{om}} + \frac{R_3}{R_3 + R_1} V_{\text{op}}}{\frac{R_1}{R_3 + R_1} V_{\text{om}}} \right) \]  
12.22 General form for \( T_{\text{minus}} \) in terms of \( R_1 \), \( R_3 \), \( V_{\text{om}} \), and \( V_{\text{op}} \).

### P12.2. Opamp Integrator

![Opamp Integrator Diagram](image)

1. Offset Null 1
2. Invert. Input
3. Non-Invert. Input
4. \( V^- \)
5. Offset Null 2
6. Output
7. \( V^+ \)
8. SET

### Components

Refer to [Project 11](#) for resistor values. Use Project12.mcd to calculate the capacitor value.

Obtain \( C_f \) from the square-wave equation.
Vs+ is the voltage applied at the noninverting terminal (pin 3) of the opamp, and Vs is the voltage from Chan0_out.

Use $T_{\text{max}} = 0.1 \text{ S}$ for the initial frequency of $f=10 \text{ Hz}$.

**Procedure**

- Connect the circuit, which includes adding the capacitor and moving Chan1_in to connect to Chan0_out.

- In the Front Panel of Integrator.vi, set Vs (Chan0_out Peak(V) at 4 V to 10 V. This is adjusted to set the initial peak (lowest frequency) of the triangular wave. Also open subVI, IterateVo.vi, to observe the process of setting the output to near 0 V.

- **Run** the VI with the signal set to the SqWave mode. Re-adjust Vs for a value of Vo(Peak-to-Peak) (init) of between 5 V and 6 V. Verify that the initial and final peak-to-peak output voltage ratio is approximately 10. Note that it will be less than 10 due to the finite $R_f C_f$. The ideal integrator has infinite $R_f$. Note that only the last half of the output array is used in
the output voltage peak determination, to avoid initial transients. Also, 
the average value of the output voltage channel is subtracted from the 
waveform in the oscilloscope. Obtain a log of the Front Panel. Default 
and save.

- Now set the input waveform switch to Sine-wave and re-run. Note the 
  lower peak value. Obtain a log of the Front Panel.

![Image of oscilloscope waveform]

**P12.3. Opamp Oscillator**

**Components**

Use \( R_1 = R_3 \) from the integrator.

Make \( R_{fosc} = R_1 = R_3 \) and use \( C_f \) from the integrator.

\[ T_{osc} \approx 2.2R_{fosc}C_f \quad (12.26) \]

Note that \( T_{osc} \) is about \( \frac{1}{2} \) of the design \( T_{max} \) from the integrator or about 50 ms.
Procedure

- Turn off the power supply to reconnect the circuit into the oscillator configuration. Note the connection of Chan1_in, which measures the capacitor voltage.

- The main VI, Oscillator.vi (below), contains subVIs CountCycles.vi and T.vi. CountCycles.vi determines the number of cycles in the oscillator output data array (Chan0_in) by checking for sign changes. It then increases or decreases the sample rate (for a fixed number of samples) until the number of sign changes in the array is 4. T.vi then checks the number of samples in the positive and negative pulses and multiplies the total by the sample rate to obtain the oscillator frequency. This frequency is used to set the time base of the oscilloscope, OscOscill.vi, to display five cycles of the oscillator waveform in the Front Panel of the main VI.
• Connect the circuit with the power supply off to avoid damage to the chip. Then turn on the power supply. Open the oscillator oscilloscope VI, OscOscill.vi. Set the oscilloscope frequency, fscope, to the expected frequency of the oscillator (e.g., about 50 Hz). This sets up the scope for a full sweep of 2/fscope = 40 msec (Note that the scope is set for 2048 samples per sweep. Thus the resolution is 2/(2048fscope) = 19 μs for this example.)

• Run OscOscill.vi to verify that the circuit is oscillating. Reset fscope for a time base that includes about two cycles of oscillation and rerun. Note that this fscope setting is approximately the frequency of the oscillator.

• Open subVI CountCycles.vi. Set TimeBase (init)(msec) (full sweep time of scope) to include about two cycles of the oscillator waveform. (Use Time Base = 2/fscope.) Run the subVI to verify that the VI can find the final time base, which includes about two cycles.
Open **Oscillator.vi**. Set Time **Base(init)(msec)** to the value obtained in **CountCycles.vi**. Set in the value of **Rfosc**. **Run** the VI to obtain a final plot of the oscillator waveform and the frequency and period of the oscillator. Note the value found for the capacitor. Compare this with the value expected. The precision of the value depends on the precision of the **Rfosc**. Note that if the **Time Base(init)** is not set close to the final value, the VI will find the correct value, after some searching. Set the value of R3 for the record. It plays no role in the VI. **Save** the information in the Front Panel by obtaining a **log**.

- Replace **Rfosc** with **Rfosc ≈ 10 Rfosc** (very approximately). Set in the new value in **Oscillator.vi**. Use **Oscillator.vi** to measure the new oscillator frequency. Compare the capacitor measurement. Obtain a log for this case.

- Now replace **R3** with **R3 ≈ R3/10** (very approximately). Set in the new value of R3 for the log record. **Run** the VI. Note that the capacitor measurement is not valid for this case. The capacitor now charges to about 10% of the maximum output voltages before switching. This increases the frequency of oscillation, due to the shorter transient time. Obtain a **log** and **save**.

---

**Laboratory Project A. Communicating with the Circuit Board Using the DAQ**

**PA.1 Sending and Receiving Voltages with the Sending and Receiving VIs**

**PA.2 Sending and Receiving Voltages from the Front Panel**
PA.3 Plotting Measured Samples

PA.4 Using the Autoranging Voltmeter

PA.5 Observing the Oscilloscope Output Graph

PA.6 Discrete Output Voltage from the DAQ

PA.7 Discrete Input Voltage from the Circuit Board

PA.8 Using the Simultaneous Sending/Receiving Function

<table>
<thead>
<tr>
<th>TABLE PA.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diagram</td>
</tr>
<tr>
<td>Functions Palette</td>
</tr>
<tr>
<td>Menu Sequence:</td>
</tr>
</tbody>
</table>

| Front Panel | Tools Palette | Shift/Right Click |
| Controls Palette | Right Click–Stickpin to hold |
| Menu Sequence: | Windows>>Show Controls Palette |

**PA.1. Sending and Receiving Voltages with the Sending and Receiving VIs**

- Connect Chan0_in directly to Chan0_out on the circuit board or connector block. *Double Click* on both of the icons in the Diagram of *Measure.vi* (initial version) to bring up the VI Front Panels. These are *AO Update Channel.vi* and *AI Acquire Waveform.vi*. Set both VIs to your device number for your DAQ card and to channel 0 (using the Operating Tool or finger). Set the number of samples to 10, for example. Set the high limit and low limit in *AI Acquire Waveform.vi* to default 0.0 V. Obtain a *default* status of the settings in both VIs. For this, go to menu Operate>>Make Current Values Default.
• In the Front Panel of AO Update Channel.vi, set in a voltage of 1 V or similar (using the Operating Tool). Run the VI, AO Update Channel.vi. To run the VI, use menu sequence Operate>> Run (or, preferred, Ctrl/R). Then run Al Acquire Waveform.vi and note the voltage read (waveform array Digital Indicator). Click on the up and down arrows by the Y to scroll through more data points.

• Verify that that send and receive are consistent. Try some other voltages. Note the maximum allowed is the highlimit, 10 V. Close the send and receive VIs. Leave Measure.vi open.

PA.2. Sending and Receiving Voltages from the Front Panel

• In the Front Panel of Measure.vi (version 2), run the VI (Ctrl/R) with a variety of voltages sent out and verify that the send (output) and read
(input) agree. From the Diagram of **Measure.vi**, *Double Click* on **Mean.vi** to open the Front Panel of this VI. Note the X Array Digital Control and the mean Digital Indicator. Now *run Measure.vi* with **Send Volts** $= 0.1$ V. Note that the measurement data appear in the Array Digital Control. These are the data points that are averaged.

Now go to **Mean.vi**, *Right Click* on the indicators, select Format and Precision, and type 4 for Digits of Precision. Then scroll through the array data (by **clicking** on the up and down arrows of the Array Digital Control as shown in the sample) and compare the numbers with the mean. There will probably be some scatter in the least significant digit, due to noise. Note that the number received and averaged is not exactly the same as that requested to be sent out. This is due to the discrete nature of ADC (analog-to-digital conversion) and DAC (digital-to-analog conversion) as discussed and demonstrated in a following section.

**PA.3. Plotting Measured Samples**

- Open **PlotSamples.vi**. Prepare the Diagram for displaying the samples. For high resolution (discussed later), set the high limit and low limit as shown in the example to 1 V and 0 V, respectively. The number of samples can be 10 to 100 and is not critical at this point. We only want to gain some experience with graphs and display the point scatter.
expected under the conditions set up here. The number of samples is 40 in the example.

- Go to the Front Panel to run the VI with the voltage sent out similar to that shown in the example, 0.1 V. This must be lower than the high limit setting for the DAQ input, which is 1 V. At this voltage level, there will certainly be some data scatter. Click on the Y-axis numbers, go to Formatting..., and set the Digits of Precision to 3.

![VI Diagram]

- Now run the VI repeatedly. Note that even though there is data scatter, the average value is relatively constant (in the Received Volts Indicator). Note also that the X-axis is in msec. The total time in the graph is 40 times 1 ms (including 0) and Al Acquire Waveform.vi is set for 1000 samples/sec.

- To set (or verify) the same sample rate as in the example, open the Front Panel of Al Acquire Waveform.vi. Type in the number 1000 for the sample rate and default the value. To default, Right Click on the indicator and go to Data Operations>>Make Current Value Default. Save the VI and close.

- Re-run the VI with Send Volts = 0.015. Subtract the difference between the measured value of 0.1 V and 0.14 V sent out. Compare the difference with the resolution expected, as obtained from Table PA.2. Note that the
high limit is 1V and the mode is Unipolar.

<table>
<thead>
<tr>
<th>Range</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to +10V</td>
<td>2.44 mV</td>
</tr>
<tr>
<td>0 to +5V</td>
<td>1.22 mV</td>
</tr>
<tr>
<td>0 to +2V</td>
<td>488 μV</td>
</tr>
<tr>
<td>0 to +1V</td>
<td>244 μV</td>
</tr>
<tr>
<td>0 to +500mV</td>
<td>122 μV</td>
</tr>
<tr>
<td>0 to +200mV</td>
<td>48.8 μV</td>
</tr>
<tr>
<td>0 to +100mV</td>
<td>24.4 μV</td>
</tr>
<tr>
<td>-10 to +10V</td>
<td>4.88mV</td>
</tr>
<tr>
<td>-5 to +5V</td>
<td>2.44mV</td>
</tr>
<tr>
<td>-2 to +2V</td>
<td>1.22mV</td>
</tr>
<tr>
<td>-1 to +1V</td>
<td>488 μV</td>
</tr>
<tr>
<td>-500 to +500mV</td>
<td>244 μV</td>
</tr>
<tr>
<td>-200 to +200mV</td>
<td>122 μV</td>
</tr>
<tr>
<td>-100 to +100mV</td>
<td>48.8 μV</td>
</tr>
<tr>
<td>-50 to +50mV</td>
<td>24.4 μV</td>
</tr>
</tbody>
</table>

**PA.4. Using the Autoranging Voltmeter**

- Open a **new** VI in LabVIEW. Then **Right Click** on the Diagram, and go through Functions>>Select A VI.... and locate **ProjectA.llb**.

- **Click on Voltmeter.vi** and **Click OK**. Place the icon on the Diagram. **Double Click** on the icon to get the Front Panel.
• Now place **AO Update Channel.vi** in the Diagram of your new VI. This is in Functions>>Data Acquisition>>Analog Output.

• **Double Click** on the icon to open the VI. Set the device numbers to match that of your DAQ. Verify that output channel 0 (Chan0_out) is connected directly to input channel 0 (Chan0_in) on the connector block or circuit board. Now **run AO Update Channel.vi** repeatedly to send out a series of voltages, such as 0.09 V, 0.9 V and 9 V and for each, **run Voltmeter.vi**. Observe the automatic changing of the limits setting for the various voltages sent out. Note that the voltage is always measured with good precision. Try a negative voltage out.

**PA.5. Observing the Oscilloscope Output Graph**

• To run the oscilloscope of **Fig. A.14**, in the project library, **ProjectA.llb**, open VI **FG_A.vi**. (This VI can also conveniently be opened from the Diagram of a new LabVIEW VI.) Then under the Browse menu (from the Front Panel of **FG_A.vi**) go to Show VI Hierarchy. Locate the icon for **OscilloscopeA.vi** and **Double Click** to open the VI.
Run **FG_A.vi** at various values of Vs (Vac peak signal out) and VDCout and observe the combination waveform output in **OscilloscopeA.vi**. The limit setting is 10 V. The function generator VI, **FG_A.vi**, is discussed in a following section.

**PA.6. Discrete Output Voltage from the DAQ**

- The VIs for this exercise are in **Project A.llb**. The first example is for DAC (digital-to-analog conversion), where the receiving resolution is much smaller (better) than the sending resolution. This therefore reveals the discrete nature of the output voltage.

- The VI for assessing the discrete nature of DAQ operation is **Discrete.vi**. This VI first sweeps the requested voltage to be sent out in a quasi-continuous manner. The programmed sweep increment size is Max Volts/100. For example, for a sweep range of Max Volts = 10 mV, the sweep increments are 100 μV. However, the output voltage has a resolution of 4880 μV (bipolar).
The receiving function is set with high limit and low limit of magnitude 0.1 V. The resolution for receiving is thus 48.8 μV, that is, much less than the output voltage steps of magnitude 4880 μV.

We will examine, for example, the bipolar mode of the output channels. For this, we need to verify the DAQ configuration for bipolar output. Go to the Start Menu>>Programs>>National Instruments>>Measurements and Automation. (There may be a shortcut for this on the desktop.) Open Devices and Interfaces and then Right Click on the DAQ designator and get Properties. Click on the AO tab and set bipolar.

Open Discrete.vi. Verify that Chan0_out is connected directly to Chan0_in on the connector block or circuit board. Verify that in the Front Panel of Discrete.vi, Max Vout is set to 10 mV (for a sweep step size of 100 μV) and that the high limit is set for 0.1 V.

Run the VI. The example of this section illustrates what to expect for the case of the DAQ configured for the bipolar mode. Note that the dc offset of the DAQ has been subtracted from the plot, such that the measured voltage appears to be zero volts for zero volts sent out.

A number for the size of the measured steps is indicated [Vout Step Avg (mV)]. It is obtained by the VI as an average of all the steps. The number shown is expected, as it is twice the DAC reference voltage of $V_{ref} = 10V$ divided by $2^{12}$ or $2V_{ref}/2^{12} = 4.88mV$ where the exponent is the number of bits of the DAC. The steps are 2.44 mV for a unipolar output configuration.
• The graph on the right is a plot of input-channel samples versus sample index. The data illustrate the point scatter due to noise. The noise-free number in the plot at the end of the execution should be $2x4.88 \text{ mV} = 9.76 \text{ mV}$. Note that the scattered sample points are separated by a discrete value of $48.8 \mu \text{V}$. An Array Digital Indicator displays the samples and a Digital Indicator shows the average.

• Try other full-range sweep values such as Max Out = 20 mV and 5 mV. With Max Out = 10 mV, go to the Diagram and reset the number of samples from 50 to 500. Re-run and note the increased precision, for example, in Chan0_in Array Avg.

PA.7. Discrete Input Voltage from the Circuit Board

• For this measurement, we need a high-resolution output voltage source. If we are willing to give up voltage range, this can be accomplished with a simple resistor voltage divider. In the example here, the circuit forms an approximate 100:1 divider (270- and 2.7-kΩ resistors). This provides a source with a resolution of 49 $\mu$V (bipolar).

![Circuit Diagram](image)

• **Discrete.vi** will be used to investigate the discrete nature of the input channels. Open the VI and set high limit = 0.1 (with low limit = –0.1), for a receiving resolution that is also about 49 $\mu$V. Use Max Vout = 1 V (1000 mV). The output voltage sweep range is then Max Vout/100 = 10 mV with the voltage divider. The programmed output voltage step size is Max Vout/100 = 10 mV. Thus, after the voltage divider, this is 100 $\mu$V. The resolution of the output and input functions is similar.

• **Run Discrete.vi.** The plot is essentially a straight line with similar output and input resolution. Note that the voltage sent out (X-axis) is the actual channel voltage and that the voltage received (Y-axis) is after the voltage divider. Note also that the scatter of the input channel samples...
(right graph) reflects the discrete nature of the receiving function and the points are separated by about 49 μV.

- Set high limit = 10 V. Run the VI with the same sweep range (example below). The output voltage (after the voltage divider) has a much higher resolution (better) than the receiving function. The steps in the sweep plot have a magnitude equal to the receiving resolution. Also, the sample points are scattered by the amount of the resolution of about 4.9 mV. An example of this case is shown in Fig. A.18 (Unit A). To check the value of the differences between scattered points, run the VI on SLOW and halt the execution in a transition region. Then step through the Chan0_in Array(mV) Indicator.

- The example here illustrates the transition range of voltage between steps; that is, the transition is not abrupt. This is due to noise and the bit uncertainty that exists in the transition regions. Again, the bit-uncertainty effect may be observed during the sweep with Plot Speed set on SLOW.

- For comparing the two cases with the two limit values and with smoothing of the data with averaging, use AvgDiscrete.vi. This VI runs the subVI Discrete.vi sequentially with the high limit set to 01 and 10 (with the low limit of –0.1 and –10. The two plots appear together in a single graph in the Front Panel of AvgDiscrete.vi.

- Open AvgDiscrete.vi and Discrete.vi. In AvgDiscrete.vi, verify that Max Out = 1000 mV and that Number Avgs is set at 5 to 10. Run AvgDiscrete.vi to compare the two plots with data smoothing.

**PA.8. Using the Simultaneous Sending/Receiving Function**

- With Chan0_out and Chan0_in connected on the circuit board, open
FG_A_2.vi. Also open SR_A.vi and OscilloscopeA_2.vi. Open these from Browse>>Show VI Hierarchy. Run the top VI for various Vs and VDCout values. Run the VI at various frequencies and note the change in Cycles and Sample Rate. The number of cycles is increased with frequency automatically to offset delay between sending and receiving. Note the Number of Samples in the array as indicated in the Front Panel of SR_A.vi, for the various changes. Run the VI with SquareWave selected.

- In the example, VDCout = 5 V and Vs = 0.1 V. There is a slight offset in this example. The oscilloscope's high limit and low limit are set for 10 V and –10 V. Therefore, the resolution is about 5% of the Vs value. There may also be some DAQ offset.

Laboratory Project B. Characterization of the Bipolar Junction Transistor for Circuit Simulation

PB.1 SPICE Parameters and Transistor Diagram

PB.2 SPICE Equations

PB.3 Diode-Connected Transistor Measurements

PB.4 Measurement of $\beta_{DC}$ versus the Collector Current

PB.5 BJT Output Characteristic Measurement
PB.6 Simulation of the Output Characteristic Measurement

Exercises and Analysis ExerciseB.mcd-ProjectB1.mcd-ProjectB2.mcd-ProjectB3.mcd.

PB.1. SPICE Parameters and Transistor Diagram

<table>
<thead>
<tr>
<th>SPICE Name</th>
<th>Math Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IS</td>
<td>I_s</td>
<td>Saturation current.</td>
</tr>
<tr>
<td>NF</td>
<td>n_F</td>
<td>Forward-current emission coefficient.</td>
</tr>
<tr>
<td>ISE</td>
<td>I_SE</td>
<td>Base - emitter leakage saturation current.</td>
</tr>
<tr>
<td>BF</td>
<td>B_F</td>
<td>Ideal maximum forward current gain.</td>
</tr>
<tr>
<td>NE</td>
<td>n_E</td>
<td>Base - emitter leakage emission coefficient.</td>
</tr>
<tr>
<td>VAF</td>
<td>V_A</td>
<td>Forward Early voltage.</td>
</tr>
<tr>
<td>BR</td>
<td>B_R</td>
<td>Reverse current gain.</td>
</tr>
</tbody>
</table>

PB.2. SPICE Equations

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ \beta_{DC} = \frac{I_C}{I_B} ]</td>
<td>B.6 Dc ratio of collector current and total base current.</td>
</tr>
<tr>
<td>[ I_C = I_s e^{V_{BE}/n_v T} ]</td>
<td>From B.7 Collector current to base - emitter voltage relation for ( V_{BC} = 0 ) V.</td>
</tr>
<tr>
<td>[ I_S = I_C e^{\frac{-V_{BE}}{V_T}} ]</td>
<td>B.25 Form of (B.7) to calculate ( I_S ).</td>
</tr>
<tr>
<td>[ I_C = I_s e^{V_{BE}/n_v T} \left( 1 - \frac{V_{BC}}{V_{AF}} \right) ]</td>
<td>B.7 Active-mode collector</td>
</tr>
<tr>
<td>SPICE Equation</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>( I_B = \frac{I_S}{\beta_F} e^{V_{BE}/V_T} )</td>
<td>B.10 Ideal base current.</td>
</tr>
<tr>
<td>( I_B \approx \frac{I_S}{\beta_F} e^{V_{BE}/V_T} + I_{SE} e^{V_{BE}/n_T V_T} )</td>
<td>B.12 Total base current in the active mode.</td>
</tr>
<tr>
<td>( I_C = I_S \left[ \left( e^{V_{BE}/V_T} - e^{(V_{BE} - V_{CE})/V_T} \right) \left( 1 - \frac{V_{BE} - V_{CE}}{V_{AF}} \right) - \frac{1}{\beta_R} \left( e^{(V_{BE} - V_{CE})/V_T} - 1 \right) \right] )</td>
<td>B.23 General equation for collector current versus terminal voltages of the common emitter.</td>
</tr>
<tr>
<td>( I_C = I_S \left[ \left( e^{V_{BE}/V_T} - e^{(V_{BE} - V_{CE})/V_T} \right) \left( 1 - \frac{V_{BE} - V_{CE}}{V_{AF}} \right) - \frac{1}{\beta_{R, leak}} \left( e^{(V_{BE} - V_{CE})/n_T V_T} - 1 \right) \right] )</td>
<td>B.26 General equation for collector current with base leakage current and an artificial ( \beta_R ).</td>
</tr>
<tr>
<td>( \beta_{DC} = \frac{\beta_F \left( 1 - \frac{V_{BC}}{V_{AF}} \right)}{1 + \chi \left( \frac{I_{CO}}{I_S} \right)^{1/n_T}} )</td>
<td>B.38 Dc beta versus collector current.</td>
</tr>
<tr>
<td>( I_{CO} = I_C / \left( 1 - \frac{V_{BC}}{V_{AF}} \right) )</td>
<td></td>
</tr>
<tr>
<td>( \chi = \frac{\beta_F I_{SE}}{I_S} )</td>
<td></td>
</tr>
</tbody>
</table>
PB.3. Diode-Connected Transistor Measurements

Components

\[
R_E \approx \frac{\text{Chan0\_out\_max} - \text{Chan0\_in\_max}}{I_{E\text{max}}} \\
\text{Chan0\_out\_max} = 10 \text{ V} \\
\text{Chan0\_in\_max} = 0.6 \text{ V} \\
I_{E\text{max}} = 1 \text{ mA} \\
R_B \approx \beta_{DC\text{max}} R_E \\
\beta_{DC\text{max}} \approx 50
\]

*Exercise care* when forcing the transistor into the circuit board.

LabVIEW Computations
\[ I_C = I_E - I_B \]
\[ \beta_{DC} = \frac{I_C}{I_B} \]
\[ n_F = \frac{1}{(V_T \cdot \text{Slope})} \]

Slope is from curve fit of \( \ln(I_C) \) vs. \( V_{BE} \)

**Procedure**

- **Diode_IV.vi** is used to obtain the current - voltage characteristic for Circuits, B1 and B2. The results will be installed into two Control Graphs of **Beta.vi** (below). Running **Beta.vi** then produces values for \( I_C, \beta_{DC} \) versus \( I_C \), and parameters \( n_F \) and \( I_S \).

- Connect Circuit B1. In the Front Panel of **Diode_IV.vi**, set the value of \( R_E \). Run **Diode_IV.vi** and re-run while resetting Initial Chan 0_out for Min IE of about 0.01 mA. The VI will halt for IE=1 mA or Chan0_out=10 V. Obtain a log of the results. Default the Front Panel to save Initial Chan0_out. It is used in the next circuit.

- Connect Circuit B2. Set the value of \( R_B \). Run the VI. It will halt for Chan0_out at about 10 V. Obtain a log of the results.

- Open **Beta.vi**. Copy the IE and IB data from the graph (log scale) of **Diode_IV.vi** and paste the data into the Control Graphs IE (log scale) versus
VBE and IB versus VBE, respectively. These data are saved in the log of the Front Panel of Diode_IV.vi. (Reminder: For data copy and paste, Right Click on graph face and Data Operations/Copy or Paste.) Default and save Beta.vi.

- Run the computation VI, Beta.vi. Beta.vi will compute and plot $\beta_{DC}$ versus $I_C$ and indicate parameters $n_F$ and $I_S$. Note that the plot uses the values of VBE from the data of IE. An interpolation of the VBE values of IB then is made to find the corresponding IB values.

- Beta.vi finds the highest VBE on the low end (for IE or IB) and the smallest VBE on the high end, such that the two plots coincide over the full range of VBE in the combined-plot graph. Note the VBE scale in the right graph of Beta.vi. The computation of NF uses thermal voltage, $V_T$, computed for $T = 27^\circ C$. At the low currents of the measurements, the device heating is probably negligible and the transistor temperature is probably about $27^\circ C$.

- Obtain a data file of measured $I_B$ and $I_C$ for use in a Project B Mathcad file, ProjectB1.mcd. Open IC_IBtoFile.vi (below) from the ProjectB.llb. Copy and paste the plots in the graph on the right side of Beta.vi into the Control Graph of IC_IBtoFile.vi. Write your file path and file name. The file must appear in the folder with the ProjectB1.mcd.
• For *simulation* only, copy and paste the data stored in the log of the Front Panel of *Diode_IV.vi*. Follow the procedure for *Beta.vi* above.

**PB.4. Measurement of $\beta_{DC}$ versus the Collector Current**
Components

Use $R_B$ and $R_C$ from PB.3.

Procedure

- Connect Circuit B3 and run subVI, IterVCC.vi. The VI adjusts VCC to set $V_{CE} = V_{BE}$. Try various values of VBB at $VCC_{init} = 1$ V. Verify that the VI can adjust VCC to make $V_{BE} = V_{CE}$ ($V_{CB} = 0$). With a proper choice of resistors, as verified in PB.3, $V_{CC} \approx 10$ V for $V_{BB} \approx 10$ V. Beta_IC.vi sweeps VBB until $I_{C_{max}} \approx 1$ mA (very approximately) or Chan0_out = 10 V.

- Open Beta_IC.vi. Set values for RC and RB in the Digital Controls. Run the VI and re-run while resetting VBBinit to obtain an initial value of IC of about 0.01 mA. This should match the lowest current in the measurement of the emitter current of Circuit B1. Note that if VCC or VBB attempts to become greater than 10 V, the VI will halt with IC $< 1$ mA. A red VBB or VCC button will indicate this condition. If the maximum current in the plot is near this value, this is sufficient. Default and save the Front Panel. Note that for the case of $VCC > 10$ V for the last measured current, the last (invalid) data point set will be eliminated from the Mathcad data file.
• Obtain a data file of the graph. Set Get File Green (logic 1) to green and write the file path and file name. **Run** the VI to obtain the data file. The data file is used in ProjectB2.mcd.

• For obtaining a data set at a later time, such as for simulation only, open **Beta_IC.vi**; retrieve the data log from the Front Panel. Then go to the Diagram of **Beta_IC.vi** and open **XYtoDataFile2.vi** (or use Browse>>Show VI Hierarchy). Copy and paste data and **run** the data file VI to obtain the file.

• Open **BF_NE_ISE.vi** (below). Install your plot data and value of IS from **Beta_IC.vi** into the Control Graph and Digital Indicator, respectively. **Run** the VI to obtain IS, NE, and ISE. The VI performs a curve fit using (B.38). Three data-point sets used by the VI are nearest to 0.01, 0.1 and 1 mA.

• The VI, **CompareBetas.vi** (below), is for comparing the results from the two measurements from **PB.3** and **PB.4**. Open the VI and paste data from **Beta.vi** and **Beta_IC.vi** in the two Control Graphs. **Run** the VI to compare the plots. The results are expected to be very similar. This is experimental proof of the fact that IB is independent of VBC, unlike the collector current. Note that V_{BC} = 0 V in the measurement with **Beta_IC.vi**, but that V_{CB} = I_B R_B in the base current measurement of **Diode_IV.vi**. The latter is as high as about 9 V.
PB.5. BJT Output Characteristic Measurement

Components

Same circuit as in PB.4

LabVIEW Computations

SPICE $I_C$ versus $V_{CE}$. This is performed with subVI SPICE.vi.

Straight-line curve fit from active-region data:

$$I_C \approx \frac{I_{Co}}{V_{Ar}} \times V_{CE} + I_{Co} = \text{Slope} \times V_{CE} + I_{Co}$$

$I_{Co} \equiv I_C (V_{CE} = 0)$ (active-region extrapolation)

$VAF = \frac{\text{Slope}}{I_{Co}}$

Procedure

- Open subVI, IC_VCESub.vi. This VI will send out a value of VBB and sweeps VCC to sweep VCE. The maximum VCE is set for 4 V. Set the value of the resistors. Run and re-run while setting VBB for an active-region collector current of about 0.5 mA. Note that at this collector current, a maximum VCE of 4 V should be attainable as the circuit was designed (PB.3, PB.4) for $I_{Cmax} \approx 1$ mA for $V_{Re} \approx 9$V. Default and save.
Now open VI, **IC_VCE.vi**. Set the value of the resistors. Set VBB from the subVI, **IC_VCEsub.vi**. Set VCEmax at 1 V. **Run** the VI and adjust BR for a best fit. Then re-**run** the VI with VCEmax set at 4 V to obtain a good value for VAF. VAF is computed from data points in the range 1 < VCE < VCEmax. **Default and save** the Front Panel. **Double check** to be sure that the subVI is **defaulted and saved**. The data are used in the output characteristic measurement simulation.

**PB.6. Simulation of the Output Characteristic Measurement**

**Procedure**

- **SimIC_VCE.vi** simulates the output characteristic measurement and associated curve fitting. Data are supplied from an actual measurement
from any sample IC_VCEsub.vi. The data include $I_C$ versus $V_{CE}$ and $V_{BE}$ versus $V_{CE}$.

- Copy and paste the two data sets from the sample (saved Front Panel or log data) IC_VCEsub.vi. Set up all values in the Digital Controls. The information will be used to compute and display the output characteristic, measured and SPICE, and various parameters and dc variables in the Digital Indicators. Parameters $\beta_{DC}$ and $I_S$ are computed for $V_{CE} = V_{BE}$, according to the definitions. $VAF$ is computed from a selected range of $\beta_{DC}$ from the active region. (Continued below.)

- Run the VI and re-run while adjusting $BR$ for the best fit. Use a small $V_{CEmax}$ for this. Verify that $V_{CEmin} < V_{CEmax}$ for this simulation. Note that for the best fit, the SPICE curve goes from slightly greater to slightly less than the measured data with increasing $V_{CE}$ in the saturation region. Re-run for computing $VAF$ in various ranges (e.g., 1 V to 3 V, 2 V to 4 V, etc). Note that $VAF$ varies, and depends on the voltage range, unlike the ideal SPICE basic model. Of primary interest is the evaluation range of 1 V to 3 V, as this brackets the bias voltage of 2 V of the amplifier project, Project C1. Default this case.

- Note also that the curves will fit in the active region for any combination of $V_{BB}$ and $RB$. However, the $\beta_{DC}$ value will only be correct for the actual circuit values. For clarity on this point and others, the computations will be repeated in the Mathcad project file. Save the
## Laboratory Project C1. NPN Common-Emitter Amplifier

### PC.1 SPICE Equations and Pin Diagram

#### PC.2 DC Circuit Setup and Parameter Determination

#### PC.3 Amplifier Gain at One Bias Current

#### PC.4 Amplifier Gain versus Bias Current

#### PC.5 Gain-Measurement Frequency Response

Exercises and Analysis ExerciseC1.mcd - ProjectC1.mcd

### PC.1. SPICE Equations and Pin Diagram

<table>
<thead>
<tr>
<th>SPICE Equation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_{vb} = -g_m R_C \frac{g_m}{I_c/V_T}$</td>
<td>Base-to-collector gain. (C.17)</td>
</tr>
<tr>
<td>$a_v = -\beta \frac{R_C}{R_s}$</td>
<td>Circuit gain with large source resistor. (C.22)</td>
</tr>
<tr>
<td>$a_{vb} = -g_m \frac{R_C r_o}{R_C + r_o}$</td>
<td>Precision base-to-collector gain. (C.28)</td>
</tr>
<tr>
<td>$r_\pi = \beta \frac{V_T}{I_C}$</td>
<td>Transistor input resistance. (C.15)</td>
</tr>
<tr>
<td>$r_{on} = \frac{V_{AFn}}{I_C}$</td>
<td>Transistor output resistance. (C.40)</td>
</tr>
</tbody>
</table>
PC.2. DC Circuit Setup and Parameter Determination

Components

\[
R_B = \frac{(V_{BB} - V_{BE})I_{DC}}{I_{C_{max}}} \\
V_{BE} \approx 0.55 \text{ V} \\
R_C = \frac{(V_{CC} - V_{CE})}{I_{C_{max}}} \\
V_{CE} \approx 2 \text{ V} \\
I_{C_{max}} \approx 1 \text{ mA} \\
V_{CC} = V_{BE} = 9 \text{ V}
\]

Use ProjectC1.mcd for calculations. Verify bias of Circuit C3 (i.e. \(V_{CC} < 10 \text{ V}\)).

Procedure

- Type in RC. Run SetVCE.vi while re-adjusting VBB to verify that 0.1 mA<\(I_C<1 \text{ mA}\) can be obtained without VCC>10V. VCC is ramped up to obtain VCE=2 V. This will be the operating point (bias) voltage in the gain measurement. Determine VBB for IC=0.1 mA, as in the example.
**PC.3. Amplifier Gain at One Bias Current**

Components

Compute $C_b$ for Circuit C3. (Use ProjectC1.mcd.) It will be more than adequate for Circuit C2.

\[
f_{3dB} \approx \frac{1}{2\pi C_b r_{\pi}} \quad f_{3dB} \approx 30\text{Hz}
\]

\[
R_s = 10r_{\pi}
\]

SubVIs
SetVSD.vi (Set Bias)

FG_10.vi (Function Generator)

FG_12.vi (Function Generator)

SR_10.vi (Send – Receive Function)

SR_12.vi (Send – Receive Function)

Oscilloscope_10.vi (Chan0_in)

Oscilloscope_12.vi (Chan2_in)

LabVIEW Computations

\[
\beta_{DC} = \frac{(\text{Chan0}_\text{out} - \text{Chan0}_\text{in})/R_C}{(\text{Chan1}_\text{out} - \text{Chan1}_\text{in})/R_B}, \quad \beta_{DC} = \frac{(\text{Chan0}_\text{in}_{\text{acPeak}})/R_C}{(\text{Chan2}_\text{in}_{\text{acPeak}})/R_B}
\]

\[
r_{\pi} = g_m V_T / I_C
\]

Procedure

- Connect the additional components in Circuit C2, Rs, and Cb. Connect Chan2_in for reading for reading the base signal voltage.

- GainSub.vi sends out bias and signal voltage (Chan1_out). (The signal is superimposed on the bias; the bias is modulated with signal.) Chan0_in reads the response (output of amplifier). The VI then resends the input signal (Chan1_out) and reads the response at the base (Chan2_in). These results are displayed in the two graphs. The ac peak values are used to calculate the gain. The VI also computes and displays \( r_{\pi} \), \( \beta_{DC} \), and \( \beta_{ac} \).
• Open GainSub.vi. Set the Digital Controls for collector resistor, RC, base resistor, RB, and Rs. Rs is used to compute the signal current through Rs. Set Frequency at between 10 and 1000 Hz. Set VBB for 0.1 mA as determined with SetVCE.vi. VCC(init) must be less than or equal to 2 V. Default the Front Panel to hold these values for when GainSub.vi is used as a subVI.

• Ratio VBB/Vs is set at 5. The VI uses this to set \( V_s = \frac{V_{BB}}{5} \), producing, roughly, \( I_B/I_b = 5 \). This results from \( I_B = \frac{(V_{BB} - V_{BE})}{R_B} \) and \( I_b = \frac{V_s}{R_B} \). This current ratio provides for operation in the linear mode.

• Run GainSub.vi and verify \( I_C \approx 0.1 \text{mA} \). Verify that signals for \( V_{bc} = V_{in} \) and \( V_{cc} = V_o \) appear to be undistorted (maintain sine-wave integrity). Assess all numbers in the Digital Indicators. At the low current of the measurement, Gain should be very close to \( g_m \cdot RC \). Default and save the Front Panel to save settings for the next VI.

PC.4. Amplifier Gain versus Bias Current

Procedure

• Gain.vi is the main VI that obtains the voltage gain as a function of collector bias current. Open Gain.vi and verify that VBB(init) is set to your value for IC=0.1 mA and VBB/Vs=5. VCC(init) will be forced to 1 V in the execution of Gain.vi. Keep subVI GainSub.vi open to help observe the measurement in progress and to obtain Front Panel information for the maximum current. Verify that the correct data are defaulted in the Front Panel of GainSub.vi. The resistors values are not
reset in the top VI.

- Open 5COLDATA.vi. Open VIs using Browse>>Show VI Hierarchy from the main VI.

- **Run Gain.vi** to obtain the gain for a range of collector current with maximum $I_C \approx 1\,\text{mA}$. Note that there is a 500 ms delay between bias steps to allow the capacitor to charge to steady state. Verify that Chan1_out(Max) (bias plus signal) does not exceed 10 V. Set the file mode switch to Get File. **Run** the VI to obtain a data file.

- The data file includes results for $I_C$, $\alpha_v$, $\beta_{DC}$, and $\beta_{ac}$ and $r_e$. The data provide for making a comparison between measured data and SPICE computations in the Mathcad project file. **Default and save** the Front Panel of 5COLDATA.vi for a data file backup. **Default** the Front Panel of Gain.vi to save the value of VBB for the maximum current. **Default and save** the Front Panel of GainSub.vi to save the value of VBE at the maximum current.

- For obtaining a file from the saved data in Gain.vi, use GainData.vi. Transfer the data from the three Indicator Graphs of Gain.vi to the three equivalent Control Graphs in GainData.vi. **Run** GainData.vi to obtain the data file.
**PC.5. Gain-Measurement Frequency Response**

**Procedure**

- Circuit C3 has the input signal applied through the coupling capacitor. Chan0_out V(CCV) provides the input and output circuit bias. The base signal with \( \text{dc} \) removed is measured again with Chan2_in.

- Reconnect the circuit according to Circuit C3. Connect the top of \( R_B \) to Chan2_out and the bottom of \( R_s \) to Chan2_out.

- Open SetVCEC3.vi and run to determine circuit bias \( I_C \) and \( V_{CC} \). Note that if \( V_{CC} > 10 \) with \( V_{CE} < 2 \) V, a smaller value of \( R_C \) or larger value of \( R_B \) is required; that is, there is not a valid solution. (If \( V_{CE} \approx 2 \) V for \( V_{CC} = 10 \) V, this is satisfactory.) This situation could occur if the value of \( \beta_{DC} \) used in the resistor design calculation was not representative of the value for your transistor. When the circuit operates properly, \textit{default} the Front Panel to save the values. This saves a set of variable values for the Mathcad project file.

- The VI for the frequency-response measurement is FreqResp.vi (below). The VI sends out a signal through out Chan1_out over the frequency range of \( \text{Freq(init)} \) to 1 kHz. The response at the base input node on the source side of the capacitor is measured with in Chan2_in as in Circuit C2.

- Open FreqResp.vi and install your value of \( R_C \) in the Front Panel. Select \( V_s \) such as to obtain \( V_{bc} \approx 5 \text{m} \) based on \( V_{bc} \approx (r_n/R_s) V_s \). Recall that \( r_n \) versus current is contained in the data file obtained from Gain.vi and in the Front Panel of Gain.vi. The information should also be saved in the Front Panel of 5ColData.vi.

- Open subVI FG1Chan.vi to monitor the waveform of the signal from in Chan2_in. Keep SetVCEC3.vi open to verify that the \( \text{dc} \) setup functions properly. Note that the \( \text{dc} \) setup process is configured to be
slow to allow the capacitor transient to be completed.

- **Run FreqResp.vi.** Verify that in Chan2_in (ac peak) is about 5 to 10 mV at the highest frequency. Adjust Vs accordingly. Verify that a flat response is obtained at the higher frequencies. If not, a larger capacitor is needed. *Default and save* the Front Panel to preserve the f3dB information.

- From the ProjectC1.llb, open XYToDataFile.vi. Copy and paste the graph data to obtain a frequency-response data set.

**Laboratory Project C2. NPN – PNP Common-Emitter Amplifier with Current-Source Load**

PC.6 SPICE Equations and Pin Diagram

PC.7 Measurement of the PNP Parameters

PC.8 DC Circuit Setup

PC.9 Measurement of the Amplifier Gain

Exercises and Analysis ExerciseC2.mcd - ProjectC2.mcd

**PC.6. SPICE Equations and Pin Diagram**

<table>
<thead>
<tr>
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</tr>
<tr>
<td>----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>$a_v = -\beta_{acn} \frac{R_{onp}}{R_{Pn}}$</td>
<td>C.52 Amplifier gain.</td>
</tr>
<tr>
<td>$a_{vb} = -g_m \frac{R_{onp}}{r_{on} + R_{op}}$</td>
<td>C.44 Base-collector gain.</td>
</tr>
<tr>
<td>$R_{onp} = \frac{r_{on} R_{op}}{r_{on} + R_{op}}$</td>
<td>C.53 Amplifier load.</td>
</tr>
<tr>
<td>$r_{on} = \frac{V_{AFn}}{I_c}, \quad r_{op} = \frac{V_{AFp}}{I_c}$</td>
<td>C.40, C.41 NPN and PNP output resistance.</td>
</tr>
<tr>
<td>$R_{op} = \left(1 + g_m \frac{R_{Ep}}{\frac{R_{Ep}}{I_{Ep} + R_{Ep} + R_{Ep}}} \right) r_{op}$</td>
<td>C.47 Transistor output resistance.</td>
</tr>
<tr>
<td>$f_{3dB} = \frac{1}{2\pi \beta_{acp} R_{Ep} C_b} \sqrt{\left(\frac{r_{on} + r_{op}}{r_{op}}\right)^2 - 2}$</td>
<td>C.67 Design frequency of the amplifier.</td>
</tr>
</tbody>
</table>

### PC.7. Measurement of the PNP Parameters

![Circuit Diagram](image)

**Components, PNP**

Calculate $R_{Ep}$

\[0.5 < I_{Ep} R_{Ep} < 1 \text{ V} \quad V_{REP} < 1 \text{ V} \text{ at } I_{Ep} = 1 \text{ mA}\]

\[I_{Ep} = \left(\frac{(1+\beta_{DCp})}{\beta_{DCp}}\right) I_c \quad \beta_{DCp} \approx 50\]
Calculate $R_{Bp}$

\[ I_C \approx I_E \approx 1.5 \text{ mA} \quad |V_{BBp}| = 10 \text{ V} \]

\[ V_{EB} \approx 0.6 \text{ V} \quad \beta_{DCp} \approx 50 \]

\[ R_{Bp} \approx \left| \frac{V_{BBp} - V_{EB} - V_{Re}}{I_C} \right| \beta_{DCp} \quad V_{CC} = \text{Chan0_out} \quad V_{BBp} = \text{Chan1_out} \]

**Procedure**

- Circuit C4 is for obtaining the relevant SPICE parameters for the pnp. Of interest are $V_{AFP}$, $\beta_{DCp}$, and $I_{Sp}$. To obtain the parameters, connect Circuit C4 using the resistors calculated for this part (pnp). These will also be used in the complete amplifier. The VI for obtaining the parameters is **IC_VEC.vi**.

- Open **IC_VEC.vi**. Install, in their Digital Indicators, RBp and REp. **Run** the VI **IC_VEC.vi** with subVI **IC_VECTsub.vi** open to observe the plot in progress. Reset VBB as necessary to obtain an active-region IC of about 1 mA. Verify that $IC = 1$ mA with $|VBB| < 10$ V can be obtained. $|VBB|$ should be roughly 10 V at $IC = 1$ mA for maximum measurement precision. Adjust parameter $\beta_R$ for a curve fit using $VCE_{max} = 1$ V. Note that $VCE_{min}$ is automatically set to 0.5 V for small $VCE_{max}$. 
• Determine the value of VAF specifically for the range that includes the bias value of VCE for the amplifier, which is VCE ≈ 5 V. Set VCEmin = 4 V and VCEmax = 6 V. Run the VI to obtain VAF. Compare the result with VCEmin = 3 V and VCEmax = 7 V. Note that in both cases the range brackets the operating point VCE = 5 V. Default and save the Front Panel to preserve the parameter values.

• The computational subVI, SPICE_IV_Rep.vi, computes the SPICE plot, which is plotted along with the measured data. The Formula Node from the Diagram of SPICE_IV_REp.vi is shown below. A solution for IC as a function of VEC using the circuit and device equations is obtained. This is also explored in the project Mathcad file.

```
IB = (VBB - VEB) * (1 + 1/(1 + 1)) / (1 + 1) * (1 + 1) / (1 + 1)
VEB = VBB * ln(1 + 1) / (1 + 1) * (1 + 1) * exp(VEC / 1)
VCB = VEB * VEC
IC = S * [exp(VEB / 1) * exp(VCB / 1) * early(1 + 1) * exp(VCB / 1)]
```

PC.8. DC Circuit Setup

Components NPN

\( R_{Bp} \approx R_{Bn} \)

If slightly different, use \( R_{Bp} > R_{Bn} \).
Design $I_C = 1mA$.

$$I_C = \frac{V_{BB} - V_{BE}}{R_{Sn}} \beta_{DCn}$$

$$V_{CC} = \text{Chan0}_\text{out} \quad V_{BB} = \text{Chan1}_\text{out}$$

$$\beta_{DCn} \approx \beta_{DCp} \quad \text{and} \quad V_{BE} = 0.6 \text{ V}$$

**Procedure**

- **SetVCE2.vi** ramps $V_{BB}$ downward from the maximum, $V_{BB}(\text{init}) = V_{CC}(\text{init})$. Thus, initially, the npn will be in saturation and $V_{CE}$ will be very approximately 100 mV. The first check is for one point, maximum $V_{BB} = V_{CC} = 10 \text{ V}$. The initial goal is verify that the npn is in saturation and that the current is greater than 1 mA for $V_{CC} = 10 \text{ V}$.

- Connect Circuit C5. Note that the bottom of RBp is now ground and Chan1_out moves to the bottom of RBn. Also, the collectors are connected together and Chan1_in moves to the base of the npn. Move the plus side of Chan2_in and the top of REp to Chan0_out.

- Set in resistor values in **SetVCE2.vi**. Verify that $V_{BB}(\text{init}) = 10 \text{ V}$ and $V_{CC}(\text{init}) = 10 \text{ V}$. Set the Run Mode switch to One VCC (logic 1). **Run** the VI. Verify that $IC > 1 \text{ mA}$ and and that $V_{CE}$ is 50 to 300 mV (in saturation).

- **SetVCE2.vi** calculates the $V_{CE}$ operating point (bias voltage) as $(V_{CC} - V_{REp})/2$ for any $V_{CC}$ (optimum signal swing magnitude). When the Run Mode is set to Set VCE, the execution of the VI halts when this level of $V_{CE}$ is reached.
Set the Run Mode switch to Set VCE. Run the VI. Verify that the execution halts when VCE is about equal to VCE(V)Op.Pt. Note that in the example, IC = 1.14 mA for VCC = 10 V and VBB = 9.02 V. Verify that the final VCE is close to VCE(V)Op.Pt. Default the Front Panel to save the values of RBn and REp.

SetIC.vi runs SetVCE2.vi as a subVI. It ramps VCC downward to find the VCC corresponding to the design IC = 1 mA. Open SetIC.vi and have SetVCE2.vi open as well. SetIC.vi will be a subVI in the gain measurement VI. Run the VI to verify that the VI can determine the VCC corresponding to IC = 1 mA. In the example, VCC has been ramped down to 9.0 V and VBB is now down to 8.1 V. The routine will occur automatically in the execution of the gain measurement VI.
PC.9. Measurement of the Amplifier Gain

Component Computation
Procedure

- **AmpGain.vi** sweeps the signal frequency over the range $f_{\text{init}} < f_s < 1000$ Hz. Note that on the low end of the sweep, this is a fairly slow process. The functiongenerator VI sends several cycles at each frequency, which is, e.g., 1 sec/cycle at $f_s = 1$ Hz. The amplifier voltage gain is calculated at each frequency step. This is the signal output voltage, $V_o$, divided by the signal input voltage, $V_s$. $V_s$ is corrected for digital-to-analog error. The correction is performed by subVI, **DAC.vi**.

- The first measurement is made without $C_b$. Enter the value of $R_Bn$ in the Front Panel of **AmpGain.vi**. Although it is defaulted in **SetVCE2.vi**, it is needed in the Top VI in the calculation of $a_vb$. Also open subVI's **SetIC.vi** and **FG1Chan.vi** to observe the program in progress. At least temporarily open **SetVCE2.vi** to verify that the component values in the Front Panel are correct and have been made the default values.

- Set Freq(init) to 10 Hz in the Front Panel of **AmpGain.vi**. Verify that $VCC(init)$ and $VBB(init)$ are set to 10 V. Run the VI. Upon completion of the execution there should be a low-frequency plateau in the response curve. The VI uses the maximum in the plot for the amplifier (circuit) gain. The roll-off at high frequencies is due to circuit board and transistor capacitance. Note that the example is with the capacitor in place. There will be no low-frequency roll-off without the capacitor.

- Now reset $VCC(init)$ and $VBB(init)$ to match the values in the Digital Indicators (in lieu of 10 V as in the example). The dc set up will be considerably faster. Re-run **AmpGain.vi** to verify that it functions properly.

\[
f_{3\text{dB}} = \frac{1}{2\pi \beta_{\text{ACP}} R_E P C_b} \sqrt{\left(\frac{r_{\text{on}} + r_{\text{op}}}{r_{\text{op}}}\right)^2 - 2}
\]

\[
C_b = \frac{1}{2\pi \beta_{\text{DCP}} R_E P f_{3\text{dB}}} \sqrt{\left(\frac{r_{\text{op}} + r_{\text{on}}}{r_{\text{op}}}\right)^2 - 2}
\]

\[
f_{3\text{dB}} \approx f_{av} = 1 \text{ Hz} \quad \beta_{\text{ACP}} \approx \beta_{\text{DCP}}
\]
• If the gain curve appears already to be in the high-frequency roll-off at the lowest frequencies, re-run the VI with Freq(init) set to 1 Hz.

• Re-run the VI and adjust X (downward for increasing Vs) to obtain a Vo (signal sine-wave peak) of about 1 V or about one-third of VCE (operating point). Note that the DAQ limit must be set at 10 V to accommodate the dc + signal measured with Chan0_out. Therefore, the output signal voltage must be relatively large to have sufficient measurement resolution. Log the Front Panel.

• Add the capacitor, C_b, to Circuit C6. Set Freq(init) to 1 Hz. Run AmpGain.vi. If a proper selection of C_b was made, the response curve should have a flat portion as in the example. The flat segment contains the gain value. Note that if f3dBlo indicates 1 Hz, then it is less than 1 Hz. In this case, lower Freq(init) to obtain a curve that includes the f3dB frequency. It may be necessary to increase X (decrease Vs) for a satisfactory value of Vo, as the gain is higher with the capacitor. Log the Front Panel when a satisfactory result has been obtained.