# A Low Voltage CMOS Bandgap Reference without Using an Opamp

**Edward K.F. Lee**
Alfred Mann Foundation, 25134 Rye Canyon Loop, Suite 200, Santa Clarita, CA, USA
edl@aemf.org

## ABSTRACT

**A simple low voltage CMOS bandgap voltage reference that does not require an opamp is proposed. The major advantage of this design is in its low current consumption. Most of the total current consumption in the circuit is used for generating the output voltage. To improve the line regulation as well as the robustness of the design against process variations, a technique for modifying the feedback loop in the circuit was also proposed. Such modification does not require additional die area and power consumption. The proposed techniques were demonstrated with two low voltage bandgap reference designs using a conventional 0.18μm CMOS process. The reference that was designed with the proposed modified feedback loop achieved a temperature coefficient of < 10ppm/°C and a line regulation of < 0.4mV/V with a current consumption of ~5μA from a 1V supply.**

## 1. Introduction

Voltage reference is one of the most important analog building blocks and used in many digital and analog circuits such as DRAMs, flash memories, voltage regulators, analog-to-digital converters, etc. Most voltage references are usually designed based on a bandgap reference, which typically provides an output voltage of approximately 1.25V. As a result, the supply voltage for the reference needs to be greater than 1.25V. With the advance in CMOS processes, bandgap references with low supply voltages, such as < 1V, are required. To reduce the supply voltage, different voltage reference techniques have been developed [1] – [5]. Some of these techniques utilized devices that are compatible with CMOS processes such as Schottky diodes [2], dynamic threshold transistors (DTMOSTs) [3], gate-voltage difference of a MOSFET [4], etc. In this paper, bandgap voltage references based on parasitic bipolar devices are studied since they provide a more predictable voltage output even with process variations. As demonstrated in [5], a voltage reference circuit with a supply voltage of less than 1V was achieved using parasitic bipolar devices and a low voltage opamp. In this paper, an alternate low voltage bandgap reference topology that does not require an opamp is proposed. The main advantage of the proposed design is that, without an opamp, the main current consumption of the circuit is that for generating the reference output voltage. As a result, the proposed bandgap reference can achieve low power consumption.

## 2. Existing CMOS Bandgap References

A typical CMOS bandgap reference without the use of an opamp [6] is shown in Fig. 1. With the feedback loop, which consists of $M_1$ – $M_4$, the source voltage of $M_1$ is approximately equal to $V_{EB2}$. The voltage across $R_1$, referred to as $\Delta V_{EB}$, is ideally equal to the difference of the emitter voltages of $Q_1$ and $Q_2$. $\Delta V_{EB}$ can be written as $V_t \cdot \ln(N)$, where $V_t = kT/q$ and N is the emitter area ratio of $Q_2$ and $Q_1$. Assuming that the W/L ratios between $M_1$ and $M_2$ as well as among $M_3$ – $M_5$ are the same, $V_{ref}$, can be written as

$$V_{ref} = V_{EB3} + \frac{R_2}{R_1}\Delta V_{EB} \qquad (1)$$

Since the negative temperature coefficient of $V_{EB3}$ cancels out the positive temperature coefficient of $\Delta V_{EB}$, $V_{ref}$ has relatively small temperature dependence. Comparing with other conventional bandgap references that use an opamp, the advantage of this bandgap reference is that all the currents are used for generating $V_{ref}$ directly. However, the minimum required supply voltage, min[$V_{DD}$], is approximately given by $V_{EB} + V_T + 2V_{DSsat}$. With $V_T > 0.5V$ and $V_{DSsat} > 0.1V$ for a MOSFET, min[$V_{DD}$] > 1.4V.

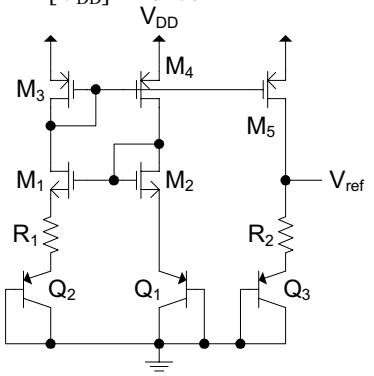


Fig. 1: Conventional bandgap without using an opamp

The bandgap reference described above has a relatively poor line regulation and this is mainly due to the differences in the MOSFET drain voltages. The line regulation can be shown to be inversely proportional to the output impedances of the MOSTETs, which can be improved using cascode technique.

To reduce the supply voltage to a value below 1V, the bandgap reference shown in Fig. 2 was proposed in [5]. With the feedback loop which utilized an opamp, the drain voltage of $M_3$ is forced to be almost the same as $V_{EB1}$ and hence, $I_{D3}$ is equal to $V_{EB1}/(R_2 + R_3) + \Delta V_{EB}/R_1$. Assuming that the W/L ratios of $M_3 - M_5$ are the same, $V_{ref}$ can be expressed as

$$V_{ref} = \frac{R_4}{R_2 + R_3}\left(V_{EB1} + \frac{R_2 + R_3}{R_1}\Delta V_{EB}\right) \quad (2)$$

Since the input common mode voltage of the opamp is shifted to a lower value by $R_2$ and $R_3$ given as $V_{EB1}\cdot R_3/(R_2 + R_3)$, an opamp with PMOS input stage can be used and the supply voltage requirement for the opamp can be reduced. If the supply voltage is not limited by the opamp, min[$V_{DD}$] will only be limited to about $V_{EB} + V_{DSsat}$. Therefore, sub-1V operation is possible. Nevertheless, extra current is consumed by the opamp that is not directly used to generate the output voltage. A bandgap reference with low current consumption can be achieved if a bandgap reference similar to Fig. 1 can be designed for low voltage operation as discussed in the next section.

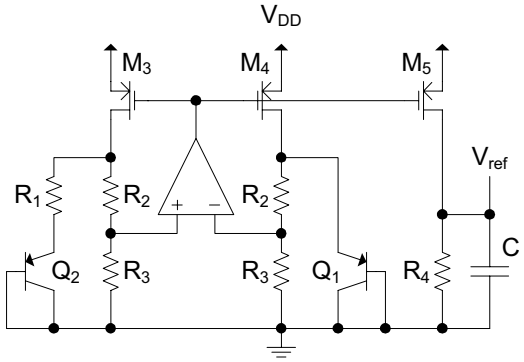


Fig. 2: Low voltage bandgap utilizing an opamp

## 3. Proposed Low Voltage Bandgap Reference

The supply voltage limit in Fig. 1 is mainly due to the direct voltage addition of $V_T + 2V_{DSsat}$ and $V_{EB}$. To eliminate this direct addition, one can use resistors to lower the source voltages of $M_1$ and $M_2$ in Fig. 1, similar to the concept of shifting down the opamp input common mode voltage in Fig. 2. Based on this concept, the proposed bandgap reference is shown in Fig. 3. Unlike the case shown in Fig. 2, there are current flows from the sources of $M_1$ and $M_2$ at nodes x and y to the two $R_3$'s. Assume that $(W/L)_{3\text{-}4} = \alpha\cdot(W/L)_{5\text{-}8}$ for $0 < \alpha$ such that $I_{D3\text{-}4} = \alpha\cdot I_{D5\text{-}8} = \alpha\cdot I$. Then the node equations at nodes x and v can be written as follow since nodes x and y (and hence, nodes u and v) are forced to be the same due to the feedback loop that consists of $M_1 - M_6$.

$$I = \frac{\Delta V_{EB}}{R_1} + \frac{V_{EB} - V_x}{R_2} \quad (3)$$

$$\frac{V_x}{R_3} = \alpha\cdot I + \frac{V_{EB} - V_x}{R_2} \quad (4)$$

After solving for I, $V_x$ and hence, $V_{ref}$ can be derived as

$$V_x = \frac{R_3(1+\alpha)}{R_2 + (1+\alpha)R_3}\left(V_{EB1} + \frac{R_2}{R_1}\frac{\alpha}{1+\alpha}\Delta V_{EB}\right) \quad (5)$$

$$V_{ref} = \frac{R_4}{R_2 + (1+\alpha)R_3}\left(V_{EB1} + \frac{R_2 + R_3}{R_1}\Delta V_{EB}\right) \quad (6)$$

Both (5) and (6) have a form similar to that in (2) and therefore, with proper selection of $\alpha$ and resistor values, either $V_{ref}$ or $V_x$ can have relatively low temperature dependence, but not simultaneously. If $V_x$ is selected to be an output, the branch that consists of $M_8$ and $R_4$ can be eliminated for further current saving. However, the range of $V_x$ is limited to a value less than $V_{EB}$, which is ~0.4V at high temperature. The headroom requirement due to the PMOS current mirror is alleviated by utilizing an NMOS source follower – $M_{11}$ and $M_{10}$ in the diode connected PMOS $M_3$ such that the gate voltages of the PMOSs can be lower than the drain voltages. The min[$V_{DD}$] can be written as

$$\min[V_{DD}] = \max[V_{EB} + V_{DSsat}, V_x + V_T + 2V_{DSsat}] \quad (7)$$

With proper choices for the values of $R_2$ and $R_3$, min[$V_{DD}$] is limited by $V_{EB} + V_{DSsat}$, and the supply voltage can be less than 1V for $V_{TN} < 0.5$V.

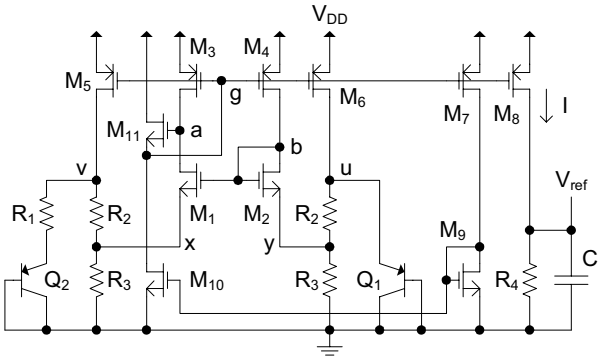


Fig. 3: Proposed low voltage bandgap

The above bandgap reference has a relatively poor line regulator property similar to the conventional bandgap reference shown in Fig. 1. This can be improved by increasing the output impedance of the PMOSs using the self-cascode technique as shown in Fig. 4a. To ensure that the circuit can start properly, a startup circuit shown in Fig. 4b can be used. The input, *in*, is connected to the nodes u, x or Vref and the output node g is connected to the node g in Fig. 3. When the input voltage is lower than the inverter threshold value, $M_{14}$ will conduct a current to turn on the PMOSs. $M_{12}$ and $M_{13}$ have to be properly size for a given power supply and an input voltage range to ensure that $M_{14}$ turns off during normal operation.

## 4. Loop Gain Improvement

The relatively poor line regulation for the proposed reference is due to the mismatch in the currents through $M_1$ and $M_2$ that results in a voltage difference between $V_x$ and $V_y$. Alternatively, this voltage difference can also be explained as a result of not having a sufficient loop gain to keep $V_x$ and $V_y$ the same under different parameter variations, including power supply variations as well as process variations. If the feedback loop consisted of $M_1$ – $M_4$ in Fig. 3 is broken at the gate of $M_1$, the open loop gain from the source of $M_1$ to node b can be shown to be approximately equal to $g_{m1}\cdot(1/g_{m2} + z_y)$ where $z_y$ is the impedance from the source of $M_2$ looking into node y. To improve the loop gain, a modification on the feedback loop is proposed as shown in Fig. 5. The MOSFETs – $M_1$ and $M_3$ are split into $M_{1a}$ and $M_{1b}$ as well as $M_{3a}$ and $M_{3b}$ with a ratio of 1:k. In this case, the open loop gain is increased to $\sim g_{m1a}\cdot[(g_{m2}\cdot r_{ds2}\cdot z_y)//r_4]$ where $r_4$ is the output impedance of the self-cascode PMOS, $M_4$, and has a value of $\sim g_m\cdot r_{ds}^2$, which is usually greater than $z_y$. Notice that the small signal voltage change on node d does not affect the loop gain significantly since this voltage change on the gate of $M_2$ is degenerated by $z_y$. Nevertheless, the increased overall loop gain will keep the voltage on node b close to the voltage on node d. Hence, the current flows through $M_{1b}$ and $M_2$ will match closely according to their W/L ratios. However, the ratio of the currents flowing through $M_{1a}$ and $M_{1b}$ will have a small error comparing to their W/L ratio values due to the difference in voltages between nodes a and d. Nevertheless, the overall current flowing through nodes x and y will have a relatively small overall matching error if k is large. Hence, the voltage difference between nodes x and y will be relatively small under different parameter variations. This modification does not cost any additional area and current consumption and reduce the variation on the output voltage significantly for different supply voltages and process variations as discussed in the next section. Nevertheless, depending on the current level of each branch, sometimes a small capacitor may be required to add between nodes a (or g) and b to ensure the stability of the feedback loop.

## 5. Simulation Results

The proposed bandgap references were designed based on a conventional 0.18µm CMOS process that provides parasitic PNP transistors, 1.8V MOSFETs as well as 3.3V MOSFETs for I/O circuits. The nominal $V_T$ is ~0.5V for the 1.8V MOSFETs and ~0.7V for the 3.3V MOSFETs. The currents $I_{D5\text{-}8}$ were selected to be ~1.1µA. The ratio between $I_{D5\text{-}8}$ and $I_{D3\text{-}4}$, $\alpha$, was set to 0.5. The emitter area ratio, N, was set to 8. For the voltage reference with the modified feedback loop shown in Fig. 5, the k factor was selected to be 3 and a compensation capacitor of 0.5pF was used. In both cases, $V_{ref}$ was taken as the output voltage. The nominal output voltages were ~0.550V and ~0.563V for the bandgaps shown in Fig. 3 and Fig. 5, respectively. For the typical process corner, Fig. 6 shows the output voltages, $V_{ref}$, of the two proposed references at room temperature when the supply voltages were changed from 0 to 2V. Both references started to operate correctly for $V_{DD}$ > ~0.85V and consumed ~5µA at 1V. The reference shown in Fig. 3 had a higher dependence on $V_{DD}$. The line regulations were 29.9mV/V and 0.37mV/V for the two bandgaps shown in Fig. 3 and Fig. 5, respectively. The supply rejections at 10Hz were 29dB and 64.7dB for the two bandgaps shown in Fig. 3 and Fig. 5, respectively. Due to the compensation capacitor used in the bandgap shown in Fig. 5 and the relatively low bias currents in both references, the supply rejection decreased at high frequencies. When the k factor changed from 3 to 1 and 7, the corresponding line regulations for the bandgap shown in Fig. 5 were 0.97mV/V and 0.19mV/V, respectively. These results demonstrated that the proposed reference with the modified feedback loop had compatible performances with the low voltage bandgap reference that used an opamp, which had a line regulation of ~7mV/V found in [5].

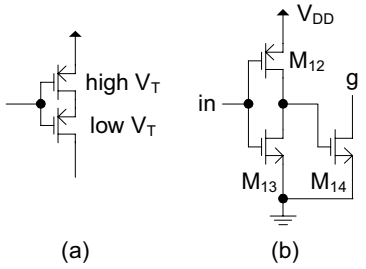


Fig. 4: (a) self-cascoded PMOS and (b) startup circuit

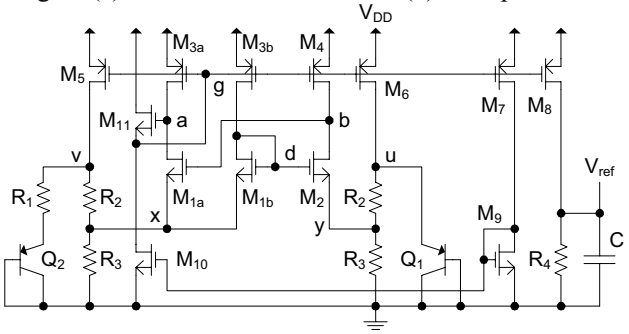


Fig. 5: Proposed bandgap with modified feedback loop

The two references were also simulated for different process corners with a supply voltage of 1V over a temperature range of –20°C and 100°C. To better illustrate the effects of the feedback loop alone, only

the typical model for the bipolar transistors was used. The results are shown in Fig. 7a and 7b. For the typical process corner, the temperature coefficients were found to be < 9.0ppm/°C for both designs. However, $V_{ref}$ varied significantly over different process corners and temperatures for the reference shown in Fig. 3. The overall % changes on $V_{ref}$ were between –1.28% and +1.51%. For the reference shown in Fig. 5, the overall % changes were between –0.14% and +0.22%. Based on the simulation results, it was demonstrated that the proposed bandgap reference with the modified feedback loop could operate at supply voltages less than 1V and was very robust against supply voltage and process variations. Table 1 summarizes the performances of the two proposed bandgap references.

## 6. Summary and Conclusion

In this paper, a low voltage bandgap voltage reference topology without the use of an opamp was proposed. The design required a low supply voltage that could be lower than 1V, and this was achieved by shifting down the operating voltage of the feedback loop using resistors. The reference voltage could be taken from two different nodes in the circuit. The required conditions for generating low temperature dependent output voltages taken from both nodes were described briefly. To improve the robustness against power supply and process variations, a modification of the feedback loop within the circuit was introduced. No increases in area and power are required with this modification. The two sub-1V bandgap references were designed based on a conventional 0.18µm CMOS process to demonstrate the proposed techniques. Over 30dB improvement in the line regulation and approximately seven times improvement against the temperature and process variations were observed when the feedback loop was modified. The proposed topologies are relatively simple and easy to design. It can be used in many low voltage analog and digital ICs.

## REFERENCES


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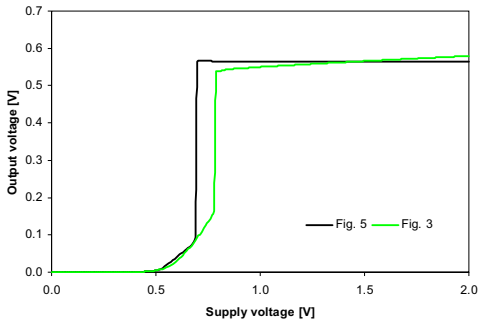
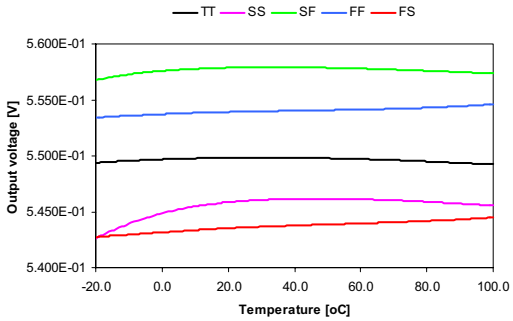
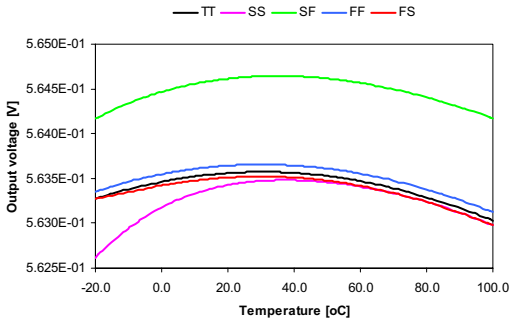



Fig. 6: Output voltages vs. $V_{DD}$ for Fig. 3 and Fig. 5




(a)




(b)

Fig. 7: Output voltages vs. temperature with different process corners for (a) Fig. 3 and (b) Fig. 5

Table 1: Performance summary

| Parameters | Fig. 3 | Fig. 5 |
|---|---|---|
| Current consumption | 4.95µA @ 1V | 5.07µA @ 1V |
| $V_{DD}$ range | 0.85V – 1.8V | 0.85V – 1.8V |
| Nominal output voltage | 549.65mV | 563.42mV |
| Line regulation | 29.9mV/V | 0.37mV/V |
| Power supply rejection | 29.0dB @ 10Hz | 64.7dB @ 10Hz |
| | 25.1dB @ 10kHz | 8.7dB @ 10kHz |
| Temperature coefficient | 9.0ppm/°C | 8.0ppm/°C |
| Changes on temperature and process variations | –1.28% / +1.51%<br>–7.0mV / +8.3mV | –0.14% / +0.22%<br>–0.8mV / +1.2mV |