CMOS Bandgap Voltage Reference With 1.8-V Power Supply

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Abstract—To overcome the limitation of the silicon energy gap in electron volts 1.2V which leads to that the voltage reference is fixed at about 1.2V, a design of current-mode (CM) architecture CMOS bandgap voltage reference with arbitrary voltage value by setting the resistor value is presented here with low 1.8-V power supply. The simulation results indicate a temperature coefficient (TC) of 5ppm/°C from -20°C to 125°C after trimming and a power supply rejection ratio (PSRR) of 64dB.

I. Introduction

Voltage reference source circuitry of high stability and high precision is a very important block in the integrated circuit such as A/D, D/A and other communication systems. In the past, the conventional implementation of the bandgap voltage reference [1][2] provides a fixed output voltage almost equal to the silicon energy gap voltage 1.2V, measured in electron volts. With the development of CMOS technology, low voltage and low power become two essential design criteria in both the analog and digital systems. So the conventional architecture is improperly used in the latest deep-submicron technologies whose power supply is equal to or lower than 1.2V. This paper presents a low-voltage current-mode CMOS bandgap reference [3][4] which architecture can provide arbitrary voltage reference value from 0 to near to the power supply by adjusting current mirror or the resistor R_3 indicated in Figure 1. The complete circuit consists of a start-up circuit, an operational amplifier and the core block including two PNP bipolar junction transistors (BJTs).

II. CM CMOS Bandgap Voltage Reference

Figure 1 shows the structure of proposed CM Bandgap voltage reference. The resistor R_{2A} and R_{2B} are connected to the differential inputs of the amplifier by nodes A and B respectively. There exists a feedback loop from the output to the inputs of the op amp formed by M1, M2, Q1, Q2 and R_1. If the dimension of M1 and M2 are equal, the currents through them are equal which are both referred to I. The amplifier forces the nodes A and B have the same potential, so the currents through R_{2A} and R_{2B} are same when $R_{2A} = R_{2B}$. For PNP BJTs Q1 and Q2, the current through emitter is relative to V_{EB} as the following:

$$I_1 = I_2 = I_s e^{qV_{EB}/kT} \quad (1)$$

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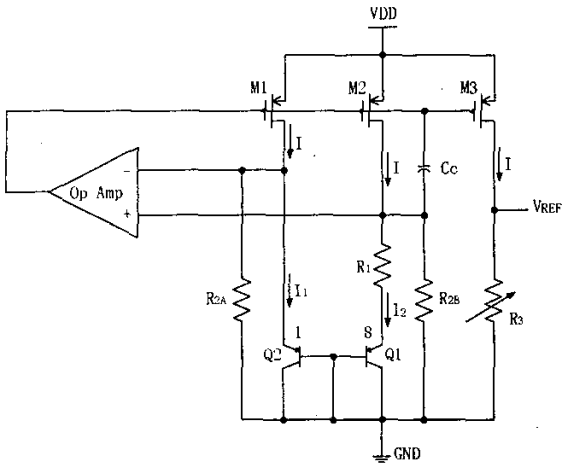

Fig.1. Structure of CM CMOS Bandgap Voltage Reference

The difference ΔV_{EB} between Q1 and Q2 is given by

$$\Delta V_{EB} = V_{EB2} - V_{EB1} = \frac{kT}{q} \ln N = V_T \ln N \qquad (2)$$

V_T is thermal voltage and N means the emitter area ratio of Q1 and Q2. So the current through M1 or M2 is given by

$$I = \frac{V_{EB2}}{R_{2A}} + \frac{\Delta V_{EB}}{R_1} = \frac{1}{R_{2A}}(V_{EB2} + \frac{R_{2A}}{R_1}\Delta V_{EB}) \qquad (3)$$

The current I_3 through PMOS M3 is a current mirror by means of M2. Assuming the size of width and length for M2 and M3 is equal, current I will be mapped directly to I_3 with the same value. So an arbitrary V_{REF} can be obtained as the voltage drop on low-temperature coefficient resistor R_3

$$V_{REF} = I \cdot R_3 = \frac{R_3}{R_{2A}}(V_{EB2} + \frac{R_{2A}}{R_1} V_T \ln N) \qquad (4)$$

V_{EB2} has the positive temperature coefficient (TC), and the difference ΔV_{EB} between V_{EB1} and V_{EB2} has the negative TC. So appropriately trimming the ratio of R_{2A} and R_1, bandgap voltage reference V_{REF} with both low sensitivity to the varying temperature and the high PSRR is obtained. C_c plays a role of compensation capacitor to ensure the stability of the feedback loop.

The complete circuit structure includes a self-bias circuit and a start-up block other than an op amp, which is presented in figure 2.

A. Design of Operational Amplifier

As is shown in figure 2, MA1 and MA2 consistent of the differential input pair of the op amp. The design of op amp is also crucial. The offset voltage V_{os} of the amplifier is one of the most main factors of which leads to drifts and instability of the absolute value of the reference voltage V_{REF}. According to the formula (5), V_{os} is amplified by a ratio factor R_3/R_1.

$$V_{REF} = \frac{R_3}{R_{2A}}[V_{EB2} + \frac{R_{2A}}{R_1}(V_T \ln N + V_{os})] \qquad (5)$$

Mainly the offset voltage V_{os} depends on the effect of the mismatches of transistor size and threshold voltage of the input differential pair of the op amp. V_{os} is also relative to the gain of the amplifier in open loop. To reduce V_{os} and depress the disturbance due to the fluctuation of the power supply resulted in by the abrupt interfere from the surrounding circumstance, it is essential to improve the gain and PSRR of the amplifier as impossible as we can. In the design the peripheral M1 and M2 outside the amplifier can be taken as a virtual amplifier stage of which the output impedance is $1/g_m$ that decided by the size of M1 or M2. In addition, sufficient consideration for symmetrical and compact layout of the circuit system is absolutely necessary.

Inevitably the reference suffers from not only the effect of MOS transistor offset but also the noise that is also increased by the resistor ratio R_3/R_1 as the offset. However, most of the noise is wide-band thermal noise and can be reduced by adding an RC low-pass filter at the output terminal V_{REF}.

B. Bias circuit

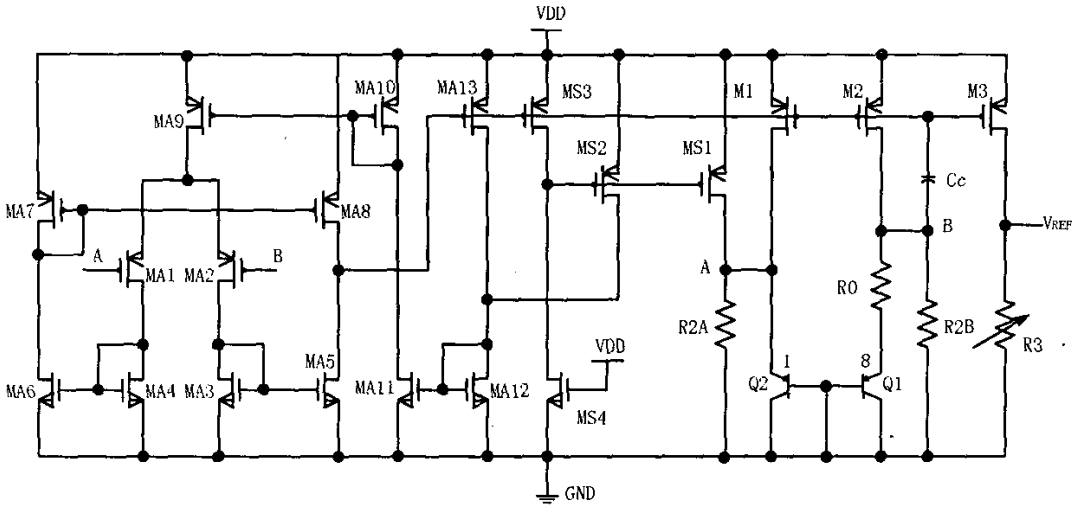

Fig.2. Complete Circuit of Bandgap Voltage Reference

It can be seen in figure 2 that MA13, MA12, MA11, MA10 and MA9 form current mirrors to provide bias current source for the input stage of the amplifier. Synchronously MA3, MA5, MA4, MA6 and MA7 also form a group of current mirrors to provide bias current for output transistor MA8. In fact, bias voltage for the primary stage current source MA13 is provided by the output of the amplifier, i. e. there forms a self-feedback access from MA8 drain output to bias current source MA9 through current mirror MA13 inside the amplifier. The structure ensures the op amp has considerably stable bias current source as long as the output V_{REF} keeps invariable.

C. Start-up circuitry

As is indicated in figure2, the start-up circuit is composed of MS1, MS2, MS3 and MS4. It will provide start-up current for Q2 and op amp. MS4 is always working no matter whether the amplifier or the other parts of the system works normally or not. When the circuit operates in zero-current state, the gate voltages of M1~M3, the same as that of MS3, are pulled high and close to supply V_{DD}. The drain voltage of MS3 or MS4 is pulled low, and this turns on MS1 and MS2 to inject current to the bandgap core circuitry by MS1 and to the amplifier by MS2. Then the amplifier starts to operate and gradually pulls down it's output voltage. With the decrease of the gate voltage of M1, the amplifier forces the drain voltage of M1 to increase. So the current is injected to M1 and Q2. Then the drain voltages of MS3 and MS4 pull high and cut off MS1 and MS2.

The W/L ratio of MS4 is critical since the loop of the reference core is destroyed if MS1 and MS2 can't be completely cut off after start-up. To ensure a complete cut-off of MS1 and MS2, the W/L ratio of MS4 is chosen to be much less than one.

III. Simulation Results

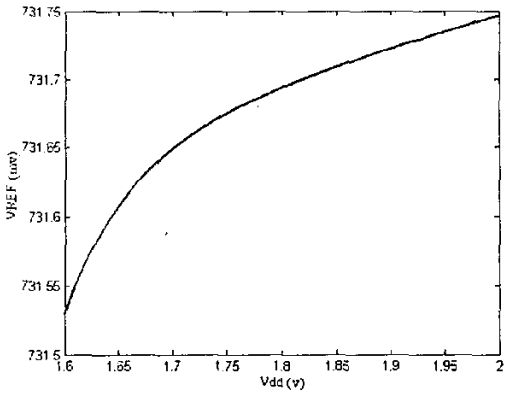

Fig.3. PSRR of the Bandgap Reference

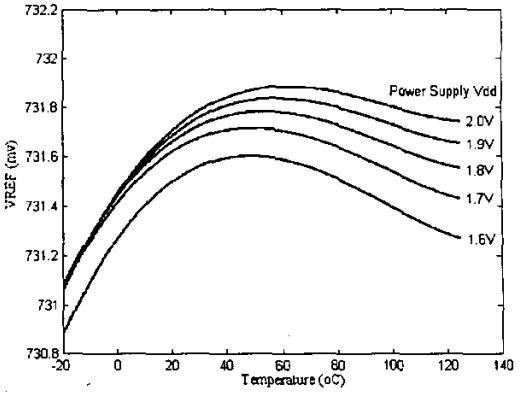

Fig.4. TCs of the Bandgap Reference

The CM CMOS bandgap voltage reference circuitry has been simulated with HSPICE. The results as showed in figure 3 presents that the design is reasonable when N=8.

The mean voltage reference is about 731.64mV when the resistor R_3 was set at 33K ohm, and changes $\pm$ 0.12mV at room temperature 25°C when the power supply changes from 1.60 to 2.0V and so the PSRR is 64dB by calculation. The measured TCs from -20°C to 125°C at different power supply voltage V_s=1.60, 1.70, 1.80, 1.90, and 2.00V are shown in Fig. 3. The minimum TC is close to 5ppm at V_s=1.70. With the extension of the temperature range, the TC increases rapidly and with the decrease of power supply the PSRR descends. From figure 4, the zero TC appears when room temperature is about 50°C. Compared with the structure mentioned in reference [6], this voltage reference circuit with a low power supply consumes much less power of 2.8mW.

IV. Conclusion

A 1.8V supply CMOS current-mode bandgap voltage reference is exhibited in this paper. The concise and regulable design structure of the reference brings much convenience for implementation. It can synchronously provide the current reference by current mirror I as well as the voltage reference by the resistor R_3. And the reference V_{REF} is adjustable which won't be fixed at the silicon energy gap voltage 1.2V. The advantages mentioned above go beyond that of the conventional structure. The simulation results of that TC≈5ppm/°C and PSRR≈64dB reveal the design feasible.

Acknowledgments

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