

## TAREFAS 1 – JUNÇÃO PN

1. Utilizando recursos de simulação do site [WWW.nanohup.org](http://WWW.nanohup.org) para simulação, obter as seguintes características da junção pn abrupta:
  - 1.1. Perfis da densidade volumétrica de cargas, densidade volumétrica de portadores, campo elétrico e potencial para tensões de -0.6, 0.0 e 0.6 V;
  - 1.2. Dependência da capacitância da junção em função do potencial aplicado na faixa de tensões de polarização  $-0,6 \text{ V} < V_D < 0,6 \text{ V}$ ;
  - 1.3. Dependência da corrente com a tensão aplicada no intervalo  $-0,6 \text{ V} < V_D < 0,6 \text{ V}$ .

Represente o eixo x, de posição, de tal forma a dar boa visibilidade nos perfis do item 1. As dopagens dos lados p e n são:

a)  $N_A = 6.25 \cdot 10^{15} \text{ cm}^{-3}$ ,  $N_D = 6.25 \cdot 10^{16} \text{ cm}^{-3}$

b)  $N_A = 6.25 \cdot 10^{15} \text{ cm}^{-3}$ ,  $N_D = 6.25 \cdot 10^{17} \text{ cm}^{-3}$

Comentar os resultados e comparar com a aproximação de depleção

## TAREFAS 2 – MEMÓRIAS

2. Descrever o princípio de funcionamento (escrita e leitura) e organização das memórias SRAM, DRAM, flash. Incluir discussão sobre tempos de acesso de escrita e leitura.

## TAREFAS 3 – MULTIPLICADOR DE TENSÃO

### PROJECT: Voltage multiplier and Dickson charge pump

**1 – Objective:** The purpose of this experiment is to convert a clock (square) signal into a dc output of either 3 V or 5 V to supply a given current to the load. For the ac/dc converter you will use either a voltage multiplier or a Dickson charge pump.

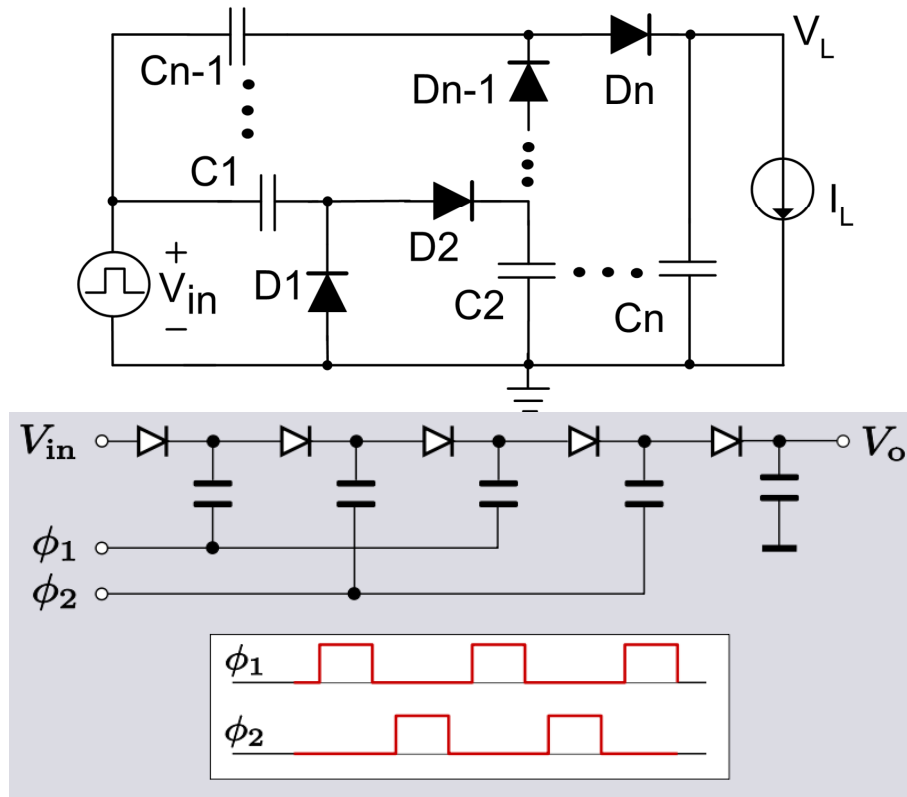


Fig.1 – Voltage multiplier and Dickson charge pump.

**2 – Components and specifications:** The diodes to be used are either Schottky diodes or 1N4148 (see curves in Fig. 2). Choose  $125 \text{ kHz} \leq f_{ck} < 1 \text{ MHz}$ . For the Dickson circuit  $V_{in}$  is the peak voltage of the clock. Capacitor values should be chosen in order to keep the voltage ripple smaller than 5%. Choose one of the specifications below for your ac/dc converter

Diode	Converter type	dc output voltage	Load current	Input voltage
Schottky	Voltage multiplier	3 V	1 uA	$\pm 0.3 \text{ V}$
Schottky	Dickson	5 V	1 uA	$\pm 0.5 \text{ V}$ ( $V_{in}=0.5 \text{ V}$ )
1N 4148	Voltage multiplier	5 V	1 uA	$\pm 0.5 \text{ V}$
1N 4148	Dickson	3 V	4 uA	$\pm 0.5 \text{ V}$ ( $V_{in}=0.5 \text{ V}$ )

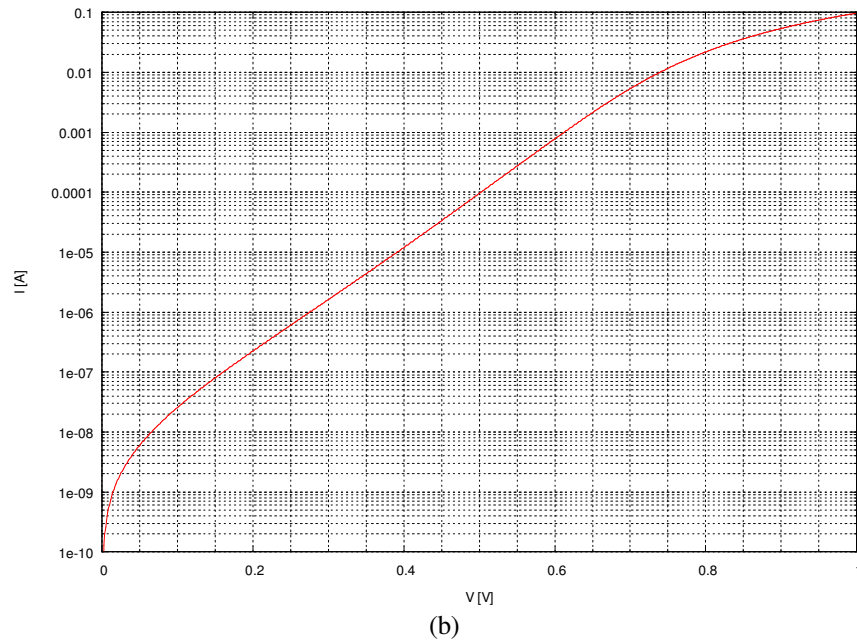
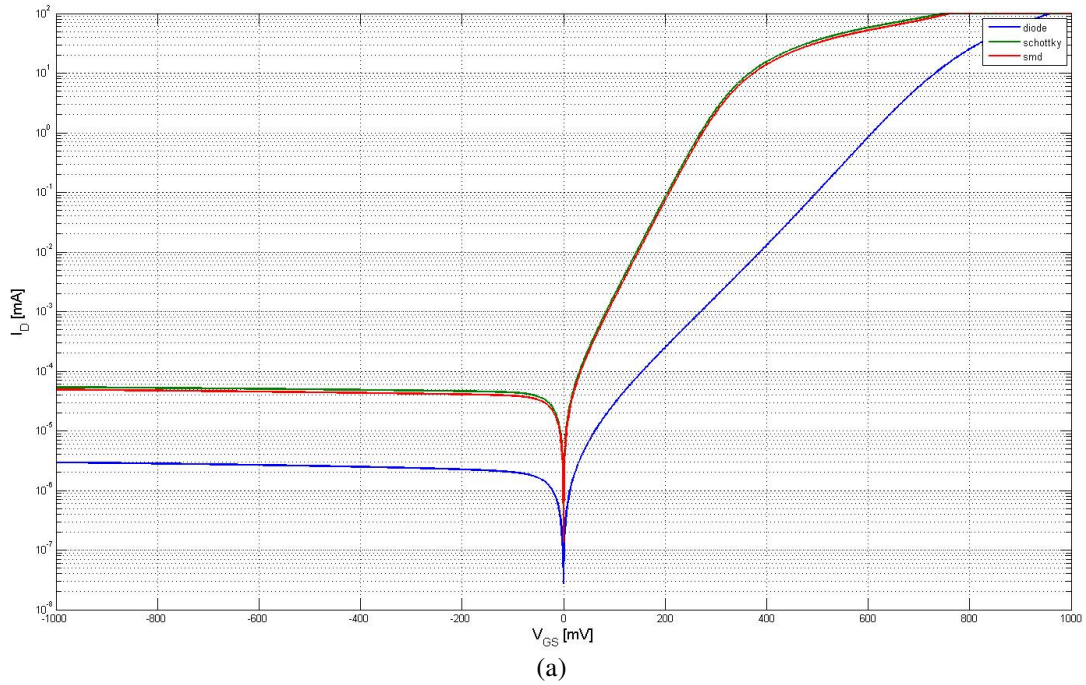


Fig.2 – (a) dc characteristics of the Schottky diode (red lines) that will be used in the experiments and of the 1N4148 diode and (b) dc characteristics of the 1N4148 diode in the forward region.

### 3 – DC characterization of the diode

The I-V diode equation for the characteristics shown in Fig. 2 can be written as:

$$I_D = I_S \left( e^{\frac{V_D - R_S I_D}{n \phi_t}} - 1 \right) \quad (1)$$

Find parameters  $I_S$ ,  $n\phi_t$ , and  $R_S$  for the diode that will be used in your project. Compare the plot of the resulting equation with the measurements in Fig. 2.

Using the results of references below, find the number of stages required for your design specifications. Before going to the lab to build the converter prototype, you must run simulations to check whether the prototype complies with the specifications.

- A. J. Cardoso, L. G. de Carli, C. Galup-Montoro, and M. C. Schneider, "Analysis of the Rectifier Circuit Valid Down to Its Low-Voltage Limit," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no.1, pp. 106 - 112, .-January 2012.
- A. J. Cardoso, Modelagem e projeto de conversores ac/dc de ultrabaixa tensão de operação, Tese de doutorado, UFSC, 2012
- L. G. de Carli, Modelagem e projeto de retificadores de múltiplos estágios para ultrabaixa tensão de operação, Trabalho de conclusão de curso, UFSC, 2013.

#### **4 – Simulations and experiment**

Use a simulator such as Spectre from Cadence or any other available simulator to find out what follows:

- 4.1. The transient response – run the transient simulation with the load not connected to the converter output. After the output voltage reaches the nominal dc voltage at the output, connect the load and observe the output voltage. Plot the graphs of the results.
- 4.2. Calculate the steady-state power delivered by the input (clock and dc voltage source). Compare with the results obtained from the simulator. What are the theoretical and simulated power conversion efficiencies (PCEs) of the converter?
- 4.3. Build the converter prototype and measure the output voltage for the nominal input voltage. Measure the input current and calculate the PCE. Compare the measurements with the results obtained in item 4.2.
- 4.4. Verify the effect of a  $\pm 20\%$  variation of the input voltage on the output voltage.

### **TAREFA 4 – SCHMITT TRIGGER**

- 4.1. Describe the operation of the Schmitt trigger in a CMOS technology.
- 4.2. For the Schmitt trigger, show how the VH and VL can be controlled by properly sizing the NMOS and PMOS transistors. Verify the appropriateness of your analysis/project using simulation in the 0.18  $\mu\text{m}$  technology

### **TAREFAS 5 – SCHMITT TRIGGER E OSCILADOR DE RELAXAÇÃO**

- 5.1 Describe the operation of the relaxation oscillator in a CMOS technology.
- 5.2. Design a relaxation oscillator in a 0.18 CMOS technology

### **Technical report and presentation**

The technical report is due on May 26. The technical report should contain, at least, the equations you used to design the prototype, and the simulation and experimental results of Section 4.

You must also prepare a ppt file for a 15-minute presentation (week May 26-30 and/or June 02-04).