Associate Professor at the University of California, Berkeley. His actual field of research is design of integrated-circuits and computer-aided design.

Mr. Vanparys has been a Fellow of the Belgian Science Foundation (IWONL) since 1972.

René A. Vanparys was born in Knokke, Belgium, on May 7, 1949. He received the Engineer's degree in electrical and mechanical engineering from the Catholic University of Leuven, Leuven, Belgium, in 1972.
In 1972 he was employed at the Catholic University of Leuven as a Research Member of the Laboratorium Fysica en Elektronica van de Halfgeleiders. In 1975 he joined the Regie van Telegrafie en Telefonie (The Belgian Post Office).

Roger Cuppens was born in Zonhoven, Belgium, on March 10, 1948. He received the Engineer's degree in electrical and mechanical engineering from the Catholic University of Leuven, Leuven, Belgium, in 1972.
He is currently a Research Member of the Laboratory for Electronics, Systems, Automatization and Technology (formerly the laboratory of Physics and Electronics of Semiconductors) at the Catholic University of Leuven, where he is working towards the Ph.D. degree.
His main interests are in semiconductor technology.

CMOS Analog Integrated Circuits Based on Weak Inversion Operation

ERIC VITTOZ, MEMBER, IEEE, AND JEAN FELLRATH

Abstract—A simple model describing the dc behavior of MOS transistors operating in weak inversion is derived on the basis of previous publications. This model includes only two parameters and is suitable for circuit design. It is verified experimentally for both p- and n-channel test transistors of a Si-gate low-voltage CMOS technology. Various circuit configurations taking advantage of weak inversion operation are described and analyzed: two different current references based on known bipolar circuits, an amplitude detector scheme which is then applied to a quartz oscillator with the result of a very low-power consumption (<0.1 μW at 32 kHz), and a low-frequency bandpass amplifier. All these circuits are insensitive to threshold and mobility variations, and compatible with a CMOS technology dedicated to digital low-power circuits.

I. INTRODUCTION

IT IS WELL KNOWN that when the gate-to-source voltage of a MOS transistor is reduced below the threshold voltage defined by the usual strong inversion characteristics, the channel current decreases approximately exponentially. This sub-threshold region of the characteristics, inside which the device operates with a weakly inverted channel, has been studied by many authors.

Barron [1] has developed the pertinent theory and has obtained a solution in closed form by introducing some approximations. Swanson and Meindl [2] have elaborated a similar expression in order to describe the behavior of CMOS inverters at a low voltage. Troutman and Chakravarti [3] have derived a model valid for any substrate bias and extendable to short channel lengths; they have shown that channel current, in weak inversion, flows by diffusion. Van Overstraeten et al. have demonstrated that this diffusion current is a function of the inversion charge at the source and drain [4], and have pointed out the influence of surface potential fluctuations on the I_D - V_G characteristics [4], [5]. In subsequent papers, Troutman has analyzed in more detail the effect of substrate bias [6] and the slope of the exponential characteristics [7]. Masuhara et al. [8] have presented a model in closed form describing accurately the behavior of MOS transistors in their whole range of operation, with excellent experimental agreement.

Recently, Barker [9] has proposed to use weak inversion operation for small signal amplification and has derived an appropriate model.

The purpose of this paper is to demonstrate that weak inversion (or subthreshold) operation of MOS transistors can be used advantageously to implement interesting analog circuits, especially in CMOS technology. A very simple model, based on previously mentioned work and suitable for circuit design, is derived in Section II and supported by experimental evidence in Section III. On this basis, Section IV describes various circuit configurations taking advantage of the weak inversion behavior and reports results obtained with experimental circuits.

II. Simple Model in Weak Inversion

Let us make the following assumptions.

1) The channel is sufficiently long so that the gradual channel approximation can be used and channel-length modulation effects are negligible.

2) Generation currents in the drain, channel, and source depletion regions are negligible; source and drain currents are then equal.

3) The density of fast surface states and the fluctuations of surface potential are negligible.

The basic derivation of Barron [1] may then be used and can be easily extended to the case of nonzero source-to-substrate voltage. His approximate expression (25) for the weak inversion current may then be rewritten, for an n-channel transistor, as

$$I_D = S\mu U_T^2 \left(\frac{1}{2}q\epsilon_s n_i\right)^{1/2} e^{-(3\phi/2U_T)} \frac{e^{\psi_s/U_T}}{(\psi_s - U_T)^{1/2}}$$
$$\cdot (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}) \tag{1}$$

where

S = geometrical shape factor of the transistor (effective width over effective length of the channel),

μ = mobility of carriers in the channel,

$U_T = kT/q$,

ϵ_s = permittivity of Si,

$\phi = U_T \ln(N_B/n_i)$ bulk Fermi potential,

N_B = constant bulk impurity concentration,

n_i = intrinsic carrier concentration,

ψ_s = surface potential, constant along the channel in weak inversion [1],

V_S = source-to-substrate voltage,

V_D = drain-to-substrate voltage,

V_G = gate-to-substrate voltage, and

I_D = drain current.

This result can also be derived from [3, eq. (16)] or from the results summarized in [8, table I].

It is valid for

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S \tag{2}$$

that is within a range $\phi - 4U_T$ of ψ_s below the value $2\phi + V_S$ for which strong inversion starts at the source end of the channel.

On the other hand, the surface depletion capacitance C_d can be expressed as [4]

$$C_d = \left(\frac{\frac{1}{2}\epsilon_s q n_i}{\psi_s - U_T}\right)^{1/2} e^{\phi/2U_T}. \tag{3}$$

It may be inserted into (1), which yields

$$I_D = S\mu U_T^2 C_d e^{-(2\phi/U_T)} e^{\psi_s/U_T} (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}). \tag{4}$$

Due to the very slow variation of C_d with ψ_s, I_D is essentially depending exponentially on ψ_s/U_T.

Variations of the gate-to-substrate voltage V_G are shared between the oxide capacitance per unit area C_{ox} and the semi-
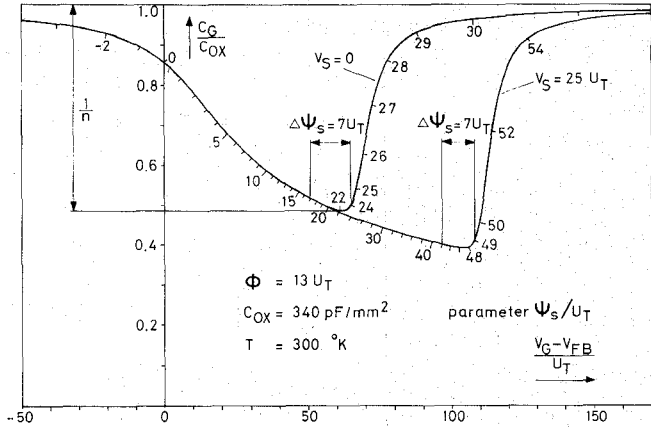

Fig. 1. Normalized $C_G - V_G$ curve at the source end of the channel calculated for typical parameters. The range $\Delta\psi_s$ of surface potential corresponding to weak inversion operation is located at the minimum of the curve. The slope factor n is closely related to the value of this minimum.

conductor total surface capacitance per unit area C_s. Therefore,

$$\frac{\partial\psi_s}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_s} = 1 - \frac{C_G}{C_{ox}} \tag{5}$$

where C_G is the gate capacitance per unit area.

Fig. 1 shows typical normalized $C_G - V_G$ curves calculated [10] at the source end of the channel by assuming a negligible density of fast surface states. The first part of the curves corresponding to a decrease of C_G with increasing V_G is valid for the whole channel as long as $V_D \geqslant V_S$.

Corresponding values of the surface potential ψ_s have been reported along the curves. It can be seen that C_G is fairly constant for

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S - 2U_T \tag{6}$$

that is within a range $\Delta\psi_s = \phi - 6U_T$ of ψ_s included in the limits of validity (2) of (4), which corresponds to more than three orders of magnitude for I_D if $\phi \geqslant 13U_T$.

According to (5), ψ_s is linearly depending on V_G inside this range and (4) takes the simple form

$$I_D = S I_{DO} e^{V_G/nU_T} (e^{-(V_S/U_T)} - e^{-(V_D/U_T)}) \tag{7}$$

where I_{DO} is a characteristic current and n a slope factor.

As a negligible density of fast surface states is assumed, C_s is equal to C_d within the range of interest and (5) yields the slope factor

$$n = 1 + \frac{C_d}{C_{ox}}. \tag{8}$$

As shown in Fig. 1, n can be evaluated at the minimum of the $C_G - V_G$ curve for which $\psi_s \cong 2\phi + V_S - 4U_T$, so that (3) and (8) yield

$$n = \frac{1}{1 - (C_G/C_{ox})_{\min}} = 1 + \frac{1}{C_{ox}}\left(\frac{qN_B\epsilon_s}{2(2\phi - 5U_T + V_S)}\right)^{1/2}. \tag{9}$$

This result may be deduced directly from [7, eq. (10)].

Thanks to the slow variation of C_d with ψ_s, the slope factor n may be considered as a constant for transistors biased by

similar values of V_S. The same is true for the characteristic current I_{DO} for transistors on the same chip. Meanwhile, I_{DO} is very poorly controlled from batch to batch and, therefore, its absolute value is of no use to the circuit designer; the designs must be based on drain current ratios, as is common practice for bipolar circuits. On the contrary, n is a reproducible parameter available for circuit design.

As shown by (9), n takes different values for transistors biased by widely different values of V_S. The same is true for I_{DO}, so that the technique of drain current ratios can only be applied to transistors with differential values of V_S not exceeding a few U_T. This is not a real limitation to design flexibility, as will be demonstrated by examples in Section IV.

Expression (7) is seen to be symmetrical in V_D and V_S, as can be expected from the symmetrical structure of the device. It is applicable to p-channel transistors as well by changing the signs of V_G, V_S, and V_D.

The transconductance in weak inversion is

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_D}{nU_T}. \tag{10}$$

For $V_D - V_S \gg U_T$, a source transconductance can be defined as

$$g_{mS} = \frac{\partial I_D}{\partial V_S} = \frac{I_D}{U_T}. \tag{11}$$

The upper limit of validity for (7) is obtained by introducing in (4) the upper limit of ψ_s given by (6) and by replacing C_d by its value taken from (8); this yields, for $V_D - V_S > 3U_T$ (saturated drain current),

$$I_D \lesssim \frac{n-1}{e^2} S\mu C_{ox} U_T^2. \tag{12}$$

The minimum value of S ensuring weak inversion operation can be calculated from this relation; the factor $(n-1)/e^2$ can be dropped if a rough order of magnitude is all that is needed, so that this upper limit is a direct function of the strong inversion transfer parameter

$$\beta = S\mu C_{ox}. \tag{13}$$

Van Overstraeten et al. have shown that surface potential fluctuations may affect the slope of the $I_D - V_G$ characteristics [5], but have practically no effect on the $I_D - V_D$ curve [11]. The model of (7) is therefore still valid, with an increased and less controllable value of n.

For a nonnegligible density of fast surface states N_{ss} [2], [11], the $I_D - V_G$ curve keeps its exponential shape, but the slope factor n is increased. Furthermore, the $I_D - V_D$ curve is also affected, so that the simple model (7) should be modified. Anyhow, this dependence of the characteristics on the badly controlled value of N_{ss} would make questionable the design of analog circuits operating in weak inversion.

The influence of surface states is negligible as long as $qN_{ss} \ll C_d + C_{ox}$. This condition is always fulfilled for $N_{ss} \ll 2 \cdot 10^{11}$ cm^{-2} eV^{-1} if the oxide thickness does not exceed 120 nm.
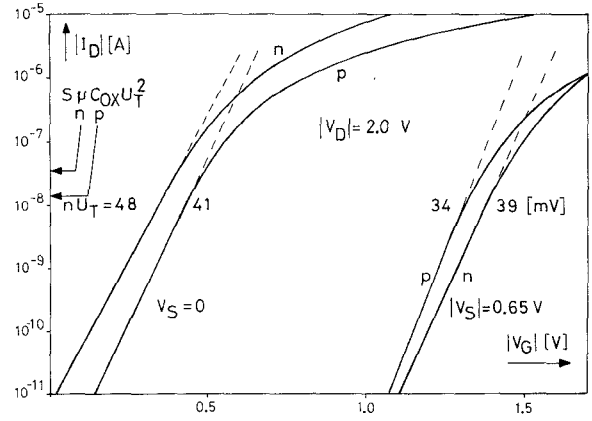

Fig. 2. Gate transfer characteristics measured for $|V_D| - |V_S| \gg U_T$; the slope factor n is slightly decreasing with increasing reverse source-to-substrate voltage $|V_S|$.

TABLE I
MEASURED AND CALCULATED VALUES OF nU_T

	n-channel		p-channel	
nU_T [mV]	$V_S = 0$	$V_S = 0.65$ V	$V_S = 0$	$V_S = 0.65$ V
Measured	48	39	41	34
Calculated	47	40	40	35

III. EXPERIMENTAL DATA ON MOS TRANSISTORS

The features of weak inversion operation described by (7) have been verified experimentally with a CMOS silicon-gate technology similar to the one described earlier in [12]. Main parameters are: n-type substrate and p-type wells doping of $2 \cdot 10^{15}$ cm^{-3} and $5 \cdot 10^{15}$ cm^{-3}, respectively, after processing, and $C_{ox} = 340$ pF/mm^2. Test transistors have a channel of 20-μm length and 60-μm width. All measurements have been made at room temperature.

Fig. 2 shows the measured $I_D - V_G$ transfer characteristics for $V_D - V_S \gg U_T$. The curves are seen to follow the exponential law up to the limit predicted by (12). The corresponding nU_T products reported in Table I are in good agreement with values obtained from (9). It should be pointed out that as I_D decreases from strong inversion, the value of g_m/I_D increases until it reaches its maximum value $1/nU_T$ given by (10) as soon as weak inversion is reached.

Fig. 3 shows the effect of V_S for $V_D - V_S \gg 0$. As predicted by (7), the behavior is again exponential, with a negative slope corresponding to a characteristic voltage equal to U_T for both types of transistors. The dc transfer characteristics in common gate configuration are, therefore, identical to that of a bipolar transistor in the common base configuration, which is in agreement with (11).

Fig. 4 shows the $I_D - V_D$ output characteristics of the transistors measured in weak inversion. As given by (7), the drain currents saturate exponentially with a characteristic voltage equal to U_T. The maximum drain current is practically attained for $|V_D - V_S| = 3U_T$, which corresponds to an excellent behavior as a dc current source. As for strong inversion, the flatness of these output characteristics is degraded
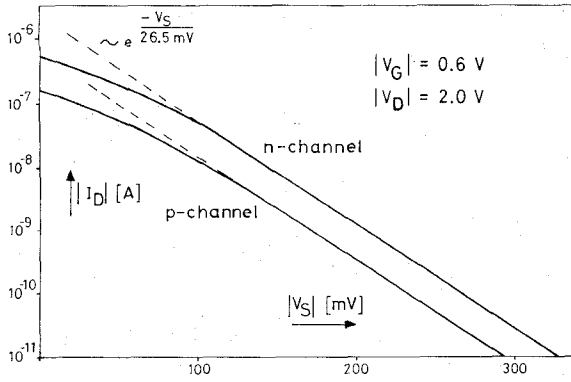
Fig. 3. Source transfer characteristics measured for $|V_D| - |V_S| \gg U_T$. This behavior in weak inversion is identical to that of a bipolar transistor in common base configuration.
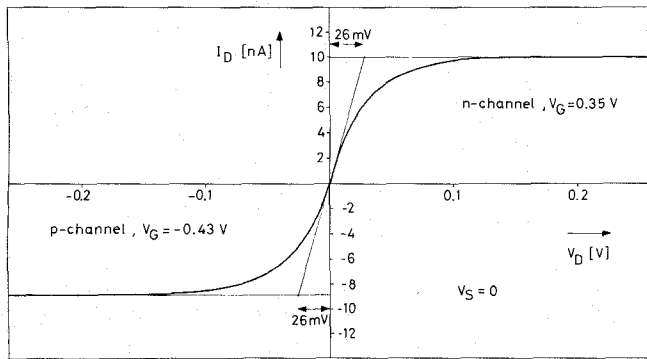

Fig. 4. Output characteristics of p- and n-channel transistors measured in weak inversion. They correspond to an excellent behavior of the transistors as dc current sources.

by channel-length modulation effects if the channel length is reduced.

The differential value of V_G for two transistors close to each other has been found to follow a Gaussian law. Standard deviations ranging from 10-17 mV for n-channel, and 9-14 mV for p-channel have been measured on a few slices in samples of more than 150 pairs of small size transistors (width 16 μm, length 6 μm on masks). This corresponds to a standard deviation of the characteristic current I_{DO} ranging from 23-42 percent. This spread is considerably larger than that of bipolar transistors and is a limitation to the design of analog circuits. Meanwhile, further measurements suggest that this mismatch can be considerably reduced by using larger transistors and optimum layout techniques.

Seeking for simplicity, we shall assume perfect matching of I_{DO} in the derivations of Section IV; as shown by (7), the spread of I_{DO} is equivalent to an equal spread of the shape factors S.

Statistical measurements of $(C_G/C_{ox})_{min}$ over 16 batches yield a standard deviation of the slope factor n smaller than 5 percent.

IV. EXAMPLES OF CIRCUITS BASED ON WEAK INVERSION OPERATION

The well-controlled exponential transfer characteristics and excellent dc current source behavior of both types of MOS transistors operating in weak inversion suggest some circuit
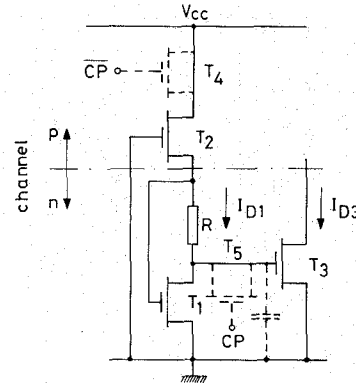

Fig. 5. Circuit diagram of a first current reference; transistors represented in dotted line allow a reduction of power consumption by using a dynamic scheme.

schemes used for bipolar transistors; further refinements can take advantage of the truly negligible gate current, and of the wide range of shape factor S practically realizable.

As a first example, Fig. 5 shows a current reference based on a known bipolar circuit [13]. It is made up of a simple badly controlled primary reference T_2 combined with a current stabilizer (T_1, T_3, R). Application of the relation (7) with $V_S = 0$ (sources connected to a common p-well) and $V_D \gg U_T$ to transistors T_1 and T_3 yields

$$I_{D3} = \frac{S_3}{S_1} I_{D1} \exp\left(-\frac{RI_{D1}}{nU_T}\right) \tag{14}$$

where the subscripts refer to those of the transistors. I_{D3} reaches a maximum

$$I_{D3\,max} = \frac{S_3}{S_1} \cdot \frac{nU_T}{eR} \tag{15}$$

for

$$I_{D1} = I_{D1\,opt} = \frac{nU_T}{R}. \tag{16}$$

Stabilization is obtained by centering the nominal value of I_{D1} at $I_{D1\,opt}$.

Fig. 6 is a microphotograph of this circuit integrated experimentally with $S_1/S_3 = 10$. The resistance R of nominal value 70 kΩ has been implemented as a strip of p-well. To reduce the total power consumption without increasing the value of R, two transistors T_4 and T_5 (represented by a dotted line on Fig. 5) have been included to pulse the current I_{D1} by the low duty cycle clock CP; I_{D3} is kept constant by the gate capacitance of T_3. This advantage would not be available in bipolar technology.

Experimental results on one sample circuit are reported in Fig. 7 for continuous operation. Both I_{D1} and I_{D3} have been measured as a function of the supply voltage V_{CC}. Although the primary reference current I_{D1} is very voltage dependent, I_{D3} is constant within 15 percent in the range 2.6 to 3.8 V for which the circuit was designed.

Measurements on 40 circuits yield an average value of 27.7 nA for $I_{D3\,max}$, which is close to the theoretical value of 25 nA calculated from (15), and a standard deviation of 11 nA.
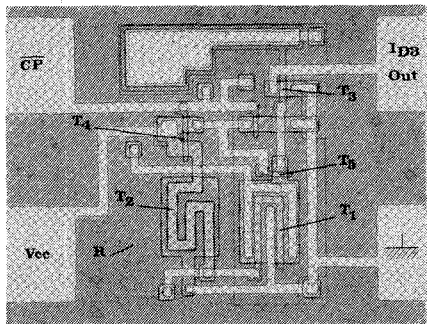
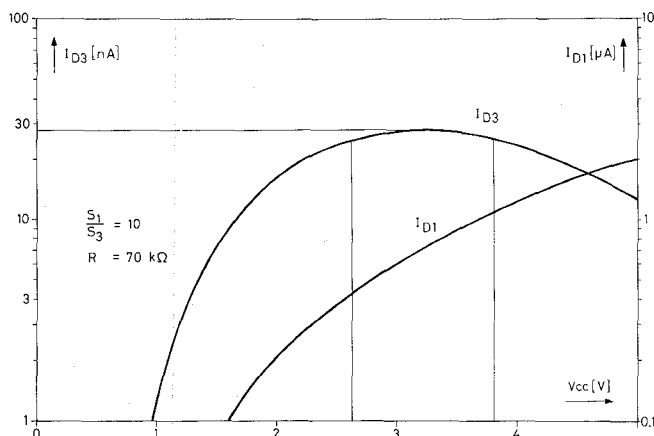Fig. 6. Microphotograph showing the circuit of Fig. 5 integrated experimentally.

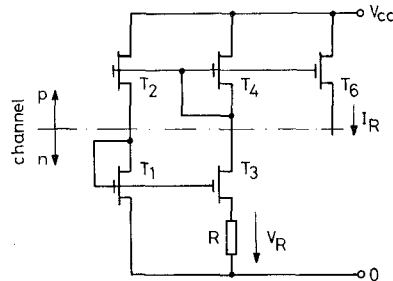Fig. 7. Measured characteristics of the circuit shown in Fig. 6.

Fig. 8. Circuit diagram of a second current reference. Voltage V_R is fully defined by the slope factor n of n-channel transistors and by the various shape factors.
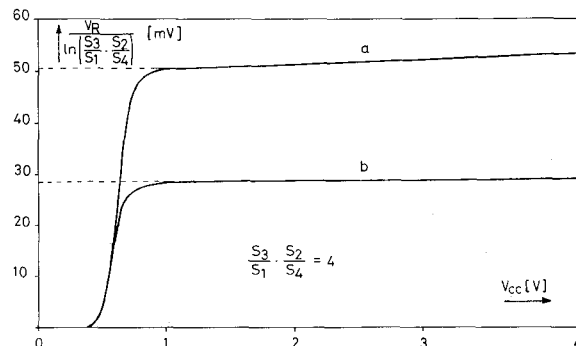

Fig. 9. Experimental results on a discrete circuit corresponding to Fig. 9; (a) T_3 in a special p-well connected to its source; (b) T_1 and T_3 in a common p-well connected to 0.

The latter corresponds to the statistical mismatch of I_{DO} reported in Section III and can be reduced by an increase in size of the transistors.

Another current reference based on a known bipolar circuit is shown in Fig. 8. The two p-type transistors T_2 and T_4 form a first current mirror of gain S_2/S_4. The two n-type transistors T_1 and T_3 form a second current mirror of gain S_3/S_1 if the current is small enough so that the resistance R can be neglected. These two current mirrors are interconnected into a closed loop, the loop gain being the product of the two gains. This loop gain for small currents is chosen higher than one, so that the current in both branches increases until an equilibrium is reached, when the gain is reduced to one by the voltage drop V_R across resistance R.

If T_1 and T_3 operate in weak inversion, the equilibrium voltage can be calculated from the previous model, assuming that the supply voltage V_{CC} is high enough to ensure drain current saturation of T_2 and T_3.

If T_1 and T_3 are in the same p-type well, then $V_{S3} = V_R$ and $V_{G3} = V_{G1}$; the application of relation (7) to these two transistors yields the equilibrium voltage

$$V_R = U_T \ln\left(\frac{S_3}{S_1} \cdot \frac{S_2}{S_4}\right). \tag{17}$$

If T_3 is in a separate well connected to its source, then $V_{S3} = 0$ and $V_{G3} = V_{G1} - V_R$ and the result is

$$V_R = n U_T \ln\left(\frac{S_3}{S_1} \cdot \frac{S_2}{S_4}\right). \tag{18}$$

The reference current proportional to V_R/R is extracted by the current mirror $T_4 - T_6$. Thanks to the small value of V_R, a total current drain of less than 1 μA is possible with a value of resistance R below 100 kΩ. In practice, this reference resistor can be realized as a strip of p-well. As in the previous circuit, the power consumption can be reduced further by using a dynamic scheme.

Fig. 9 shows the reference voltage V_R normalized to the logarithm of the low-current loop gain, measured as a function of the supply voltage V_{CC} on a circuit made up of discrete selected transistors. It is seen that this normalized reference voltage saturates at a value very close to U_T or nU_T, depending on the way the substrate of T_3 is connected.

As another example, Fig. 10 shows an amplitude detector. This circuit is biased by a reference current I_R which is mirrored by T_2 and T_4. The various shape factors are chosen such as $S_3/S_1 > S_4/S_2$, so that the drain current of T_3 overcomes that of T_4 for zero amplitude U_1 of input voltage V_{in}; the dc output voltage is then zero. As amplitude U_1 increases, the average gate voltage $\overline{V}_{G1}$ of T_1 must decrease to keep the average current drain of this transistor constant in spite of the nonlinear transfer characteristics (variations of drain voltages of T_1 and T_2 are avoided by the capacitor C_3).

The ac component is filtered out by R_2C_2, therefore, $V_{G3} = \overline{V}_{G1}$, hence, the drain current of T_3 decreases as U_1 increases. As U_1 reaches a critical value U_{1C}, the drain current of T_4 overcomes that of T_3 and V_{out} jumps to V_{CC}.

For a sinusoidal input signal $U_1 \sin \omega t$, and for transistors T_1 and T_3 operating in weak inversion with $V_{S1} = V_{S3} = 0$ (sources connected to a common p-well) and $V_{D3} \gg U_T$, the
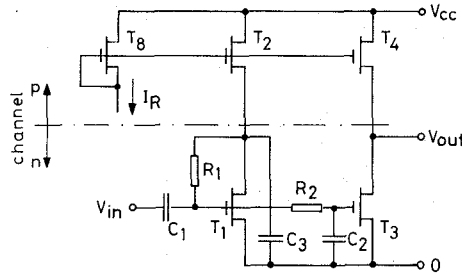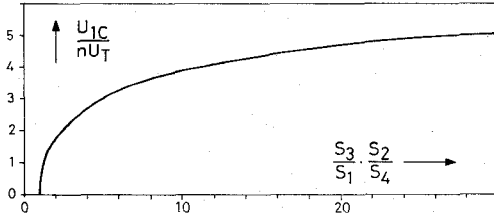
Fig. 10. Circuit diagram of an ac amplitude detector.

Fig. 12. Low-current quartz oscillator using the scheme of Fig. 10 for amplitude limitation.

Fig. 11. Theoretical threshold U_{1C} of the amplitude detector for a sinusoidal signal.

Fig. 13. Microphotograph showing the oscillator of Fig. 12 integrated experimentally; output amplifier is not included; R_1 and R_2 are implemented as lateral diodes in the polycrystalline gate layers.

drain current of T_1 may be written from (7):

$$I_{D1} = S_1 I_{DO} \exp \left(\frac{V_{G3} + U_1 \sin \omega t}{n U_T} \right); \qquad (19)$$

averaging over one period gives

$$\bar{I}_{D1} = S_1 I_{DO} e^{V_{G3}/n U_T} I_0 \left(\frac{U_1}{n U_T} \right) = \frac{S_1}{S_3} I_{D3} I_0 \left(\frac{U_1}{n U_T} \right) \qquad (20)$$

where I_0 is the 0-order modified Bessel function [14]. Equating $\bar{I}_{D1}/I_{D3}$ to S_2/S_4 yields the following relation defining the critical voltage U_{1C}:

$$I_0 \left(\frac{U_{1C}}{n U_T} \right) = \frac{S_3}{S_1} \cdot \frac{S_2}{S_4}. \qquad (21)$$

The threshold U_{1C} of the detector depends only on the well-controlled voltage $n U_T$ and the various shape factors. As shown in Fig. 11, U_{1C} becomes fairly insensitive to the shape factors (and to fluctuations of the characteristic current I_{DO}) as soon as it exceeds 4–5 $n U_T$.

This circuit has not yet been integrated in this form, but the scheme has been applied to stabilize the amplitude of a quartz oscillator, as shown in Fig. 12.

The quartz resonator QR, the transistor T_1, and the two capacitors C_3 and C_4 constitute a Pierce oscillator biased by the resistance R_1 and the current source T_2. The dc gain of the closed loop made up of transistors T_1, T_3, T_4, and T_2 is higher than one so that the currents in both branches increase to high values limited by the output characteristics of T_2 and T_3. The drain current I_{D1} of T_1 is high and, therefore, oscillation builds up. As the amplitude U_1 at the gate of T_1 reaches the value U_{1C} given by (21), I_{D1} suddenly falls down to the value just necessary to keep this amplitude of oscillation. This value corresponds by relation (10) to a transconductance g_{m1} of T_1 somewhat larger than the critical transconductance for oscillation; the maximum value of g_m/I_D reached in weak inversion is, therefore, used advantageously to reduce power
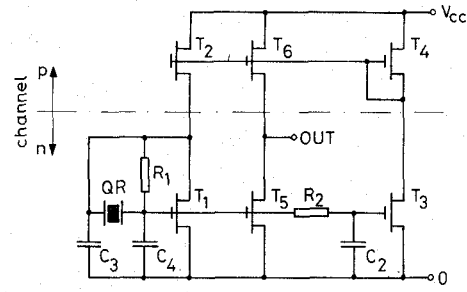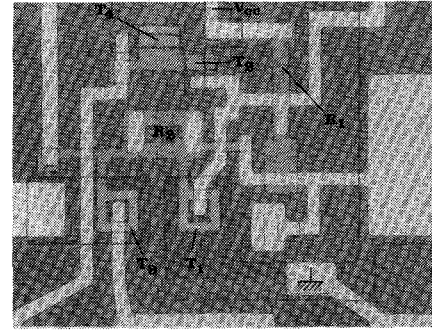
consumption. The signal can be amplified to reach the logic swing by the directed coupled stage $T_5 - T_6$.

Fig. 13 is a microphotograph of this oscillator integrated experimentally without the amplifier stage. To ensure weak inversion operation, the channel width of T_1 and T_3 has been increased by the use of closed structures. The noncritical high value resistance R_2 of the low-pass filter is implemented as a quad of polycrystalline lateral diodes. This type of diode is obtained naturally with silicon-gate technology at every p to n transition of the gate layer. A differential resistance in the range 1–10 GΩ at zero voltage has been measured on 10-μm width diodes fabricated with the doped-oxide technology [12]. The biasing resistor R_1 is a single lateral diode.

Fig. 14 shows experimental results obtained with this circuit. It is seen that the amplitude of oscillation U_1 at the gate, and the current drain I, are both fairly independent of the supply voltage V_{CC} in the range of 1–3 V. The amplitude is very close to the calculated critical value U_{1C}. With the typical values of components chosen for the experiment, the current drain is of the order of 30 nA. Another 60 nA would be sufficient for the output amplifier, so that a total current of less than 100 nA is feasible. The current increases to a much higher value if the quartz is removed.

Due to the quasi-independence of U_{1C} on the current level, the current has a tendency to fluctuate around its nominal value. This can be easily avoided by adding a noncritical series resistance of a few 100 kΩ in the source of T_3. This resistance reduces the feedback gain but has a negligible effect on the amplitude.

Weak inversion operation can help to control the biasing conditions of an amplifier, and hence, its frequency response.
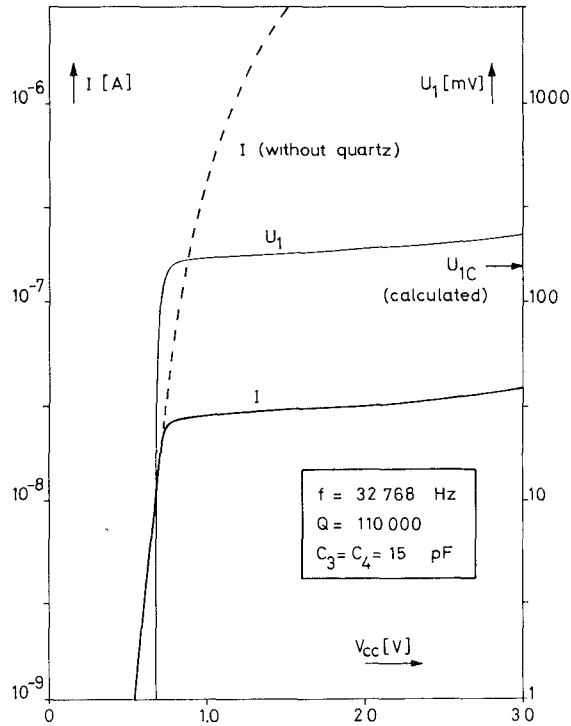
Fig. 14. Experimental results obtained with the circuit shown in Fig. 13; amplitude of oscillation U_1 and total current I are fairly independent of the supply voltage V_{CC}. A standard watch quartz resonator with quality factor Q is used.
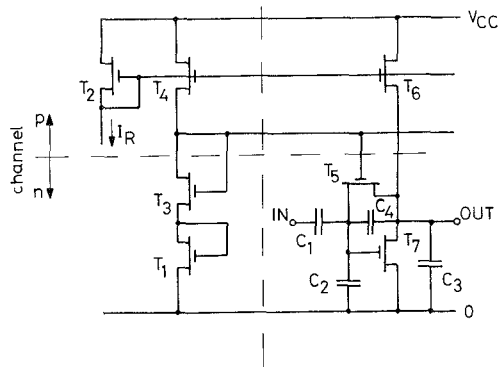

Fig. 15. Voltage reference (a) and one stage (b) of a multistage bandpass amplifier.

As an example, Fig. 15 shows a multistage bandpass amplifier made up of a cascade of amplifier stages (b) and a single voltage reference (a) common to all stages. The circuit is biased by a current I_R.

The basic parameters defining the frequency response of one stage are the various capacitors, the transconductance g_{m7} of T_7 and the differential output resistance R_5 of T_5 is defined as

$$\frac{1}{R_5} = \frac{\partial I_{D5}}{\partial(V_{D5} - V_{S5})}\bigg|_{V_{D5} = V_{S5}}. \tag{22}$$

As a matter of fact, by assuming $C_1 \gg C_2 + C_3$, $C_4 \cong 0$ and $R_5 g_{m7} \gg 1$, the gain of a single stage of a long chain is found to have the following asymptotic values:

low frequency $A_L = -j\omega C_1 R_5$,   (23)

medium frequency $A_0 = -\sqrt{R_5 g_{m7}}$,   (24)

high frequency $A_H = -g_{m7}/j\omega(C_2 + C_3)$.   (25)

The combination of expressions (7) and (22) yields

$$\frac{1}{R_5} = S_5 \frac{I_{DO5}}{U_T} e^{V_{G5}/n_5 U_T} e^{-(V_{S5}/U_T)} \tag{26}$$

where I_{DO5} and n_5 take special values due to the large value of V_{S5}. If the condition

$$\frac{S_6}{S_4} = \frac{S_7}{S_1} \tag{27}$$

is fulfilled, $V_{S3} = V_{S5}$ so that I_{DO5} and n_5 are also valid for T_3. As $V_{G3} = V_{G5}$, the combination of (26) and (7) applied to transistor T_3 yields the simple result

$$R_5 = \frac{S_3}{S_5} \cdot \frac{U_T}{I_{D3}} = \frac{S_3}{S_5} \cdot \frac{S_2}{S_4} \cdot \frac{U_T}{I_R}. \tag{28}$$

On the other hand, (10) gives

$$g_{m7} = \frac{S_6}{S_2} \cdot \frac{I_R}{nU_T}. \tag{29}$$

Therefore, the frequency response of the amplifier is entirely defined by the reference I_R, the various shape factors, the well-controlled parameters n and U_T, and the various capacitors. In particular, the medium frequency gain per stage A_0, given by (24), becomes

$$A_0 = \left(\frac{1}{n} \cdot \frac{S_3}{S_5} \cdot \frac{S_6}{S_4}\right)^{1/2}. \tag{30}$$

V. CONCLUSION

The dc behavior of MOS transistors operating in weak inversion can be described by a very simple model suitable for circuit design. This model has been verified experimentally and contains two parameters only: the slope factor n which is closely related to the well-controlled minimum value of the C_G/C_{ox} curve, and the characteristic current I_{DO} which is poorly controlled from batch to batch, but reasonably constant for transistors close to each other. Both n and I_{DO} are only slightly depending on the source-to-substrate voltage V_S and, therefore, different values must be taken only for transistors having widely different V_S. The behavior of MOS transistors in weak inversion is in many aspects comparable to that of bipolar transistors with the advantage of a truly negligible control current.

Theoretical considerations based on this model, as well as experimental results, show that it is possible to take advantage of this behavior in designing analog CMOS circuits: both dc circuits, such as current references, and ac circuits, such as an amplitude detector, a very low-current quartz oscillator, and a bandpass amplifier are found to be very attractive applications. The circuits described are insensitive to threshold and mobility variations, and are fully compatible with a low-voltage Si-gate CMOS technology dedicated to digital circuits. They could be implemented with other CMOS technologies as well.

Meanwhile, it must be pointed out that weak inversion operation is fundamentally limited to low-speed circuits; this is due to the reduced channel conductance for given device dimensions, when compared with strong inversion operation.

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Eric Vittoz (A'63–M'72) was born in Lausanne, Switzerland, on May 9, 1938. He received the M.S. and Ph.D. degrees in electrical engineering from the Federal Institute of Technology, Lausanne, in 1961 and 1969, respectively.

After spending one year as a Research Assistant, he joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1962, where he was involved in micropower integrated circuits development for the watch, while preparing a thesis in the same field. As Associate Director of this Laboratory in charge of the Applications Division, he is now supervising advanced electronic watch developments, with a main interest in CMOS digital and analog circuits. He also lectures in integrated-circuit design at the Federal Institute of Technology, Lausanne.

Jean Fellrath was born in Le Locle, Switzerland, on September 6, 1936. He received the M.S. degree in electrical engineering from the Ecole Polytechnique de l'Université de Lausanne, Lausanne, Switzerland, in 1960.

After spending one year as a Research Assistant at the Ecole Polytechnique, one year at Siemens Semiconductors Laboratory in Munich, and three years at the Research Department of the Swiss PTT, he joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1965, where he is presently involved with micropower IC's and watch systems developments.