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An Ultra Low Voltage, Dynamic Bulk Biasing CMOS Schmitt Trigger

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Abstract *– This paper presents an ultra low voltage Schmitt trigger for low-voltage low-power applications with a power supply down to 0.2V, The proposed trigger utilizes dynamic forward biasing of bulk-source junction of MOSFET inverter to create a hysteresis, The simulation has been performed using 0.18u TSMC PSPICE CMOS technology for Vdd= 0.2V and 0.3V.*

1 Introduction

The current trends of analog design are leading to battery-less systems through a combination between energy harvesting and low-voltage low-power techniques. The energy harvesting is the methods and mechanisms by which the surrounding ambient power can be accumulated in a temporary power storing device. Anywhere around, the ambient power may exist in many forms such as mechanical energy in vibrations, thermal energy from heating sources or human body, solar energy, light sources, radio waves, and electromagnetic energy[1]. Those sources can produce a sufficient power for many applications but with tiny voltages. However, if the produced voltage is less than the needed one, a DC to DC converter is used to step up this output voltage to the rated voltage of the application; in this case, a small transformer is used with power management chip[2] such as LTC3108 to perform the conversion task and thus increasing device size and weight which is inconvenient in some applications.

On the other hand, the implementation of low-voltage low-power techniques is necessary to make use of energy harvesting techniques. For example, a full bridge rectifier is needed to convert the harvested voltage from AC to DC, and definitely this rectifier must operate under ultra low voltage conditions in order to get high performance and efficiency [3].

The low-voltage low-power techniques can be concluded in the following terms as discussed in [4]:

- Sub-threshold region
- Bulk-Driven MOSFETs
- Floating gate MOSFETs
- Level shifter approach

Except in sub-threshold technique, the minimum biasing voltage of MOSFET gate in the other techniques is equal to threshold voltage V_t which is rather high comparing with ultra low voltage requirements. However, most of low voltage researches are concentrating on removing threshold voltage constraint from the path of the input signal regardless of biasing voltage on the gate of the MOSFET. Thus, among previous techniques, sub-threshold and bulk driven are the keywords to design low-voltage low-power applications that taking into account MOSFET gate biasing demands.

In this paper, the forward biasing of bulk-source junction of MOSFET will be illustrated. Also, the enhancement in threshold voltage requirements will be confirmed through a numerical example, whereas the rest of paper investigates the bulk effect on CMOS inverter characteristics and the switching threshold voltages. Finally, the dynamic bulk biasing Schmitt trigger will be introduced and simulated using PSPICE.

2 The Bulk Driven MOSFET

A MOSFET device consists of 4 terminals: drain (D), source(S), gate(G), and bulk(B). Usually, bulk terminal is connected to the source or to the lower voltage in the circuit according to fabrication process and used technology. However, bulk terminal has gained more attention from researchers in last decade due to its impact on threshold voltage, thus the threshold voltage constraint can be removed from the path of the input signal while the gate remains in need for biasing voltage equals or higher than MOSFET threshold voltage.

In general, the bulk driven technique suggests to fix gate terminal to a steady voltage by which an inversion layer can be built inside the MOSFET, then the input signal is delivered to bulk terminal. Figure 1 illustrates output characteristics of bulk driven MOSFET.

The drain current of gate driven MOSFET in strong inversion region is given by:

$$I_D = \frac{K_P W}{2L}(V_{GS} - V_t)^2(1 + \lambda V_{DS}) \qquad (1)$$

where K_P is the transconductance parameter, W is the channel width, L is the channel length, λ is the channel length modulation parameter, and V_t is the threshold voltage.

The relationship between V_{BS} and threshold voltage can

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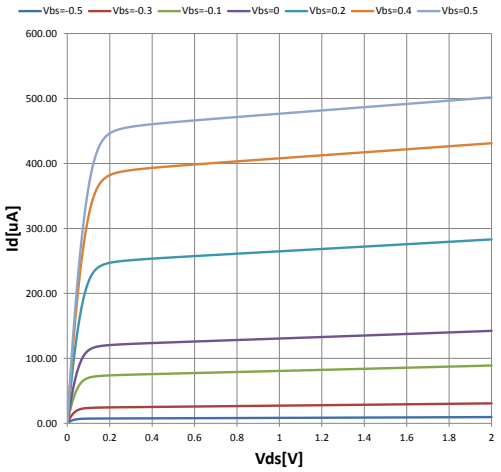

Figure 1: Output characteristics of bulk driven MOSFET Vgs=0.5V W/L=200u/2u

be expressed as:

$$V_{th} = V_{th0} + \gamma \left[\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|} \right] \tag{2}$$

where V_{th0} is the threshold voltage when $V_{BS} = 0$, γ is the body effect parameter, and Φ_F is Fermi potential.

Substituting 2 in 1 and neglecting channel length modulation λ we get:

$$I_D = \frac{K_P W}{2L} \left(V_{GS} - V_{th0} - \gamma \left[\sqrt{2|\Phi_F| - V_{BS}} - \sqrt{2|\Phi_F|} \right] \right)^2 \tag{3}$$

The bulk driven transconductance is given by:

$$g_{mB} = \left. \frac{di_D}{dv_{BS}} \right|_{V_{GS}=const} \tag{4}$$

$$g_{mB} = \frac{\gamma \sqrt{K_P \frac{W}{L} I_D}}{2\sqrt{2|\Phi_F| - V_{BS}}} \tag{5}$$

$$g_{mB} = \frac{\gamma g_m}{2\sqrt{2|\Phi_F| - V_{BS}}} \tag{6}$$

It's obvious that bulk terminal is a real control terminal of the MOSFET. However, equation 6 shows that g_{mB} is lower than g_m with a ratio of coefficient η which is given by:

$$\eta = \frac{\gamma}{2\sqrt{2|\Phi_F| - V_{BS}}} \approx 0.2 \to 0.4 \tag{7}$$

$$g_{mB} \approx (0.2 \to 0.4) g_m \tag{8}$$

3 Forward Biasing of Bulk-source junction

A closer review of equation 9 reveals that g_{mB} can exceed g_m when [5]:

$$V_{BS} \geq 2|\Phi_F| - 0.25\gamma \tag{9}$$

Equation 9 reveals that we have a better amplification possibilities when using bulk as input terminal with voltages more than $2|\Phi_F| - 0.25\gamma$ regardless of frequency response decrease due to bulk-source capacitance. Unfortunately, this situation only improves transconductance while a DC biasing of bulk is still needed. Furthermore, the voltage on bulk terminal is a critical value since it may set the bulk-source junction in forward biasing and sink a current between bulk and source. Consequently, the input impedance of bulk driven MOSFET will take a finite value when bulk-source junction has been biased forwardly, which obviously increase power dissipation ratio.

A different approach is needed to make benefit of the previous enhancement by feeding signal into gate terminal as usual, while applying a fixed positive voltage on bulk terminal. The bulk biasing voltage should not exceed the built-in potential of bulk-source junction which is given by: (see reference [6], page 14)

$$V_{bi} = \frac{kT}{q} ln \left(\frac{N_{DEP} N_{SD}}{{n_i}^2} \right) \tag{10}$$

where k is Boltzmann constant, T is the absolute temperature of the bulk-source junction, q is the electron charge, N_{DEP} is the doping concentration in the channel, N_{SD} is the doping concentration of source/drain diffusions, and n_i is the intrinsic carrier concentration in the channel region.

The gate transconductance with $V_{BS} \neq 0$ can expressed by:

$$g_{mG} = \left. \frac{di_D}{dv_{GS}} \right|_{V_{BS}=const} \tag{11}$$

$$g_{mG} = 2\beta \left(V_{GS} - V_{th0} - \gamma \left[\sqrt{|2|\Phi_F| - V_{BS}|} - \sqrt{2|\Phi_F|} \right] \right) \tag{12}$$

where $\beta = \frac{K_P W}{2L}$.

Figure 2 presents a plotting for equation 12 as a function of V_{BS} with $V_{GS} = 0.42V$ and $\Phi_F = 0.4V$, whereas γ is changing form 0.2 to 1. Theoretically, maximum g_{mG} is achieved when $V_{BS} = 2|\Phi_F|$ and it is proportional to body effect coefficient.

As mentioned previously, the maximum value of V_{BS} should not exceed the built-in potential of bulk-source junction, which is approximately 0.5V.

The circuit in figure 3 utilizes two MOSFET transistors to compare g_m curves between traditional gate driven method and the proposed method. Both of the transistors have W/L ratio = 100u/1u. The bulk–source potential of M1 and M2 are 0.4V and 0V respectively. A DC sweep of V_{GS} is ranged from 0V to 0.5V which results the curves in figure 4.

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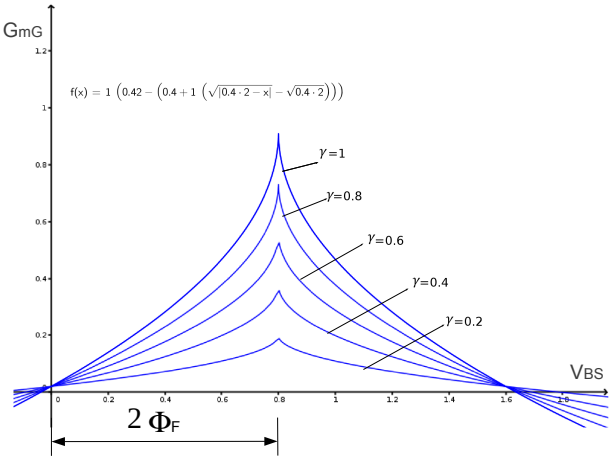

Figure 2: Gate Transconductance versus V_{BS}

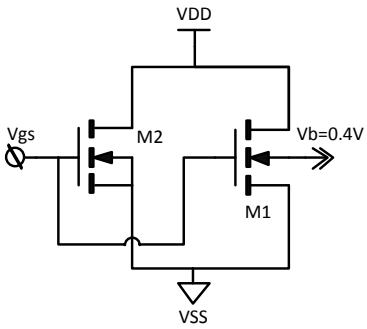

Figure 3: Test Circuit to compare g_m and g_{mG}

4 Threshold voltage enhancement

One of the current challenges in analog design is the threshold voltage of the MOSFET by which the transistor can be biased either in strong inversion or in sub-threshold.

The previous study investigated the effects of forward biasing of bulk-source junction in terms of transconductance. In addition, it can be noticed that threshold voltage is also improved.

Assuming equation 2 with default values of PSPICE MOSFET model BSIM4.6.0 introduced in [6], then V_t is calculated as follows:

γ can be derived form [6] (page 169):

$$\gamma = K_1 = 0.5V^{\frac{1}{2}} \tag{13}$$

And Fermi potential can be derived from [6] (page 11):

$$2|\Phi_F| = \varphi_S = 0.4 + \frac{kT}{q} ln\left(\frac{N_{DEP}}{n_i}\right) \tag{14}$$

The typical values of N_{DEP} and n_i are $1.7 \times 10^{17} cm^{-3}$ and $1.5 \times 10^{10} cm^{-3}$ respectively (see reference [6] page 169),

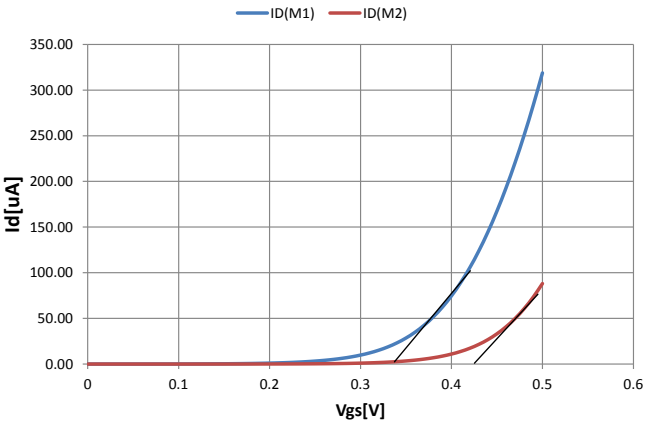

Figure 4: g_m and g_{mG} curves and threshold enhancement

then:

$$\varphi_S = 0.4 + 0.026 \times ln\left(\frac{1.7 \times 10^{17}}{1.5 \times 10^{10}}\right) = 0.82V \tag{15}$$

$$V_t|_{V_{BS}=0.4V} = 0.3669 + 0.5 \times \left[\sqrt{0.82 - 0.4} - \sqrt{0.82}\right] = 0.23V \tag{16}$$

It can be realized that threshold voltage has decreased by:

$$\Delta V_t = 0.3669 - 0.23 = 0.1369V \tag{17}$$

Returning to simulation results in figure 4, ΔV_t can be derived as the distance between the tangent lines of g_m curves. It is reduced by approximately 100mV which coincides with the theoretical calculations.

5 Bulk-Biasing Gate-Driven inverter

A direct application of bulk biasing approach was introduced in [7]. it presents an ultra low voltage ring oscillator. Figure 5 demonstrates the basic unit in this oscillator which is the CMOS inverter. It utilizes two MOSFET transistors, P channel and N channel as usual. However, the bulk terminal of the channel N MOSFET (V_{bN}) is connected to the most positive voltage in the circuit (V_{DD}). Similarly, the bulk terminal of the channel P MOSFET (V_{bP}) is connected to the minimal voltage in the circuit (V_{SS}). The measured transfer characteristics reflects a very good performance under $V_{DD} = 0.2V$.

The calculation of switching threshold voltage and voltage transfer characteristics of this inverter is essential issue for designer. Figure 6-a presents the ideal transfer function of the inverter, while figure 6-b presents the real one. The keyword for determining the switching threshold voltage V_{SW} is embedded in the red dot in figure 6-b in which the two transistors are working in saturation and input voltage is equal to output voltage.

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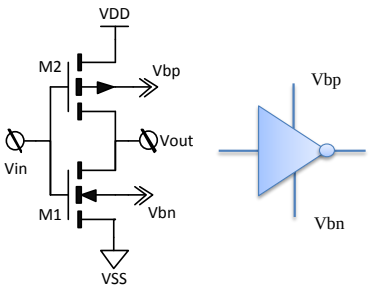

Figure 5: Forward Bulk Biased CMOS Inverter [7]

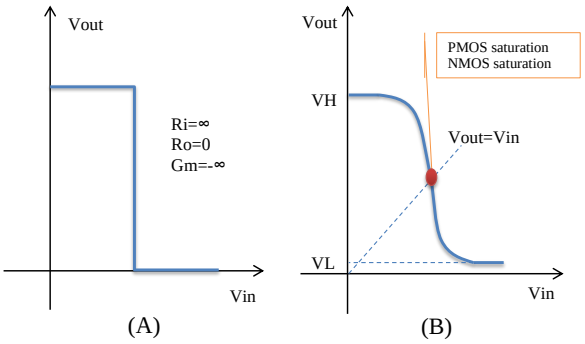

Figure 6: Transfer characteristics of CMOS inverter

V_{SW} can be calculated via CMOS equations in saturation as follows:

By using subscript N and P to refer to nMOS and pMOS respectively, then the current of M2 is given by:

$$I_{DM2} = \beta_P (V_{SGP} + V_{tP})^2 \tag{18}$$

Similarly, The current of M1 is given by:

$$I_{DM1} = \beta_N (V_{GSN} + V_{tN})^2 \tag{19}$$

The transient occurs when $V_{in} = V_{out} = V_{SW}$, then we can write:

$$I_{DM1} = I_{DM2}, V_{GSN} = V_{SW}, V_{SGP} = V_{DD} - V_{SW}$$
$$\beta_P (V_{DD} - V_{SW} + V_{tP})^2 = \beta_N (V_{SW} - V_{tN})^2 \tag{20}$$

$$V_{SW} = \frac{V_{tN} + \sqrt{\frac{\beta_P}{\beta_N}}(V_{DD} + V_{tP})}{1 + \sqrt{\frac{\beta_P}{\beta_N}}} \tag{21}$$

6 Dynamic bulk biasing Schmitt trigger

Figure 7 demonstrates the proposed trigger, which consists of two bulk-biased gate-driven CMOS inverters. The V_{bP} and V_{bN} terminals of the first inverter are connected to the output. The trigger presented in [8] assumes that the second inverter utilizes gate driven approach with $V_{BS} = 0$V.

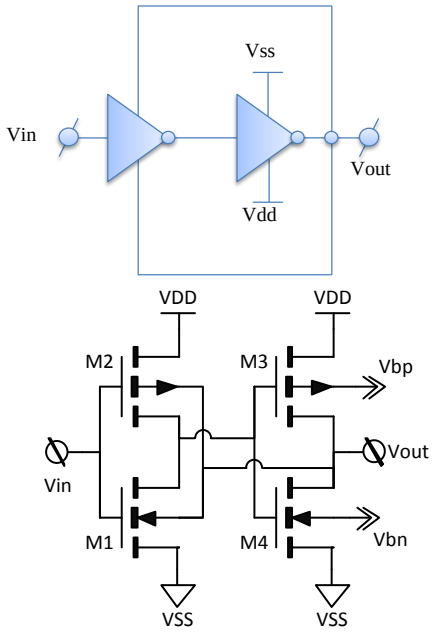

Figure 7: Proposed Schmitt Trigger

However, in this paper, V_{bP} and V_{bN} terminals of the second inverter are connected to V_{SS} and V_{DD} respectively reducing supply voltage constraints and improving load driving performance (sinking and sourcing) due to g_m improvement.

The main idea of the trigger is that V_{SW} of the first inverter is a function of V_{out} and thus composing a feedback loop with two different V_{SW} potentials associated with the two states of the output.

The second inverter is providing a shift of 180 degree to the output of the first inverter which is essential to bind the low V_{SW} to the high state of the output and the high V_{SW} to the low state of the output building up the typical hysteresis of Schmitt trigger.

Recalling equations 21 and 2, the low threshold and the high threshold can be calculated as follows:

Assuming initial state of the output is low (V_L), then:

$$V_{tNH} = V_{thN0} + \gamma \left[\sqrt{2|\Phi_{FN}| - V_L} - \sqrt{2|\Phi_{FN}|} \right] \tag{22}$$

$$|V_{tPH}| = V_{thP0} + \gamma \left[\sqrt{2|\Phi_{FP}| - (V_{DD} - V_L)} - \sqrt{2|\Phi_{FP}|} \right] \tag{23}$$

where V_{tNH}, V_{tPH} is the threshold voltages of the transistors $M1$, $M2$ respectively when V_{out} is low.

And when the output is high (V_H):

$$V_{tNL} = V_{thN0} + \gamma \left[\sqrt{2|\Phi_{FN}| - V_H} - \sqrt{2|\Phi_{FN}|} \right] \tag{24}$$

$$|V_{tPL}| = V_{thP0} + \gamma \left[\sqrt{2|\Phi_{FP}| - (V_{DD} - V_H)} - \sqrt{2|\Phi_{FP}|} \right] \tag{25}$$

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where V_{tNL}, V_{tPL} is the threshold voltages of the transistors $M1$, $M2$ respectively when V_{out} is high.

the high switching threshold is given by:

$$V^+ = \frac{V_{tNH} + \sqrt{\frac{\beta_P}{\beta_N}}(V_{DD} + V_{tPH})}{1 + \sqrt{\frac{\beta_P}{\beta_N}}} \quad (26)$$

And the low switching threshold is given by:

$$V^- = \frac{V_{tNL} + \sqrt{\frac{\beta_P}{\beta_N}}(V_{DD} + V_{tPL})}{1 + \sqrt{\frac{\beta_P}{\beta_N}}} \quad (27)$$

The hysteresis is:

$$\Delta V = V^+ - V^- = \frac{V_{tNH} - V_{tNL} + \sqrt{\frac{\beta_P}{\beta_N}}(|V_{tPH}| - |V_{tPL}|)}{1 + \sqrt{\frac{\beta_P}{\beta_N}}} \quad (28)$$

Figure 8 illustrates hysteresis and the overall parameters.

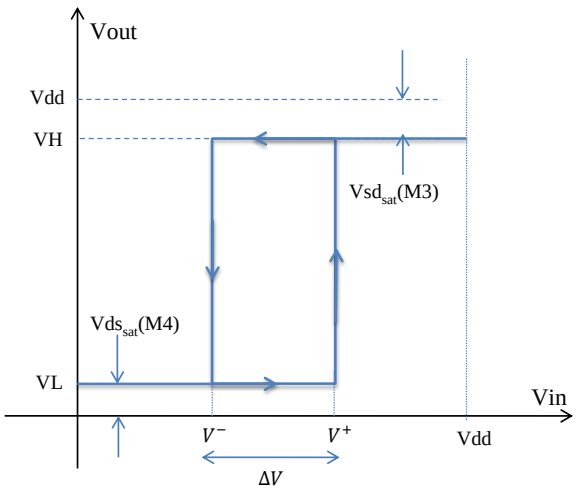

Figure 8: Hysteresis characteristics of the trigger

For simplicity, we can consider that $V_L = 0, V_H = V_{DD}, \beta_P = \beta_N$, $V_{thN0} = V_{thP0}, and \Phi_{FN} = |\Phi_{FP}|$, Then:

$$V_{SWL,H} = V^{\pm} = \frac{V_{DD} + V_{tNL,H} - |V_{TPL,H}|}{2} \quad (29)$$

By substituting in equations 22 and 23 and recalling numerical model in [6] for $V_{DD} = 0.3V$ we get:

$$V_{tNH} = 0.366 + 0.5\left[\sqrt{0.82 - 0} - \sqrt{0.82}\right] = 0.366V \quad (30)$$

$$V_{tPH} = 0.366 + 0.5\left[\sqrt{0.82 - 0.3} - \sqrt{0.82}\right] = 0.273V \quad (31)$$

$$V_{SWH} = V^+ = \frac{0.3 + 0.366 - 0.273}{2} = 0.196V \quad (32)$$

Similarly for equations 24 and 25:

$$V_{tNL} = 0.366 + 0.5\left[\sqrt{0.82 - 0.3} - \sqrt{0.82}\right] = 0.273V \quad (33)$$

$$V_{tPL} = 0.366 + 0.5\left[\sqrt{0.82 - 0} - \sqrt{0.82}\right] = 0.366V \quad (34)$$

$$V_{SWL} = V^- = \frac{0.3 + 0.273 - 0.366}{2} = 0.103V \quad (35)$$

The hysteresis is:

$$\Delta V = V^+ - V^- = 0.196 - 0.103 = 93mV \quad (36)$$

7 Simulation Results

A DC transfer simulation of the inverter in figure 5 is introduced in Figure 9 using nested DC sweep that varying Vin from 0V to 0.3V for $V_{bP} = V_{bN} = V_b = 0$ and for $V_{bP} = V_{bN} = V_b = V_{DD}$.

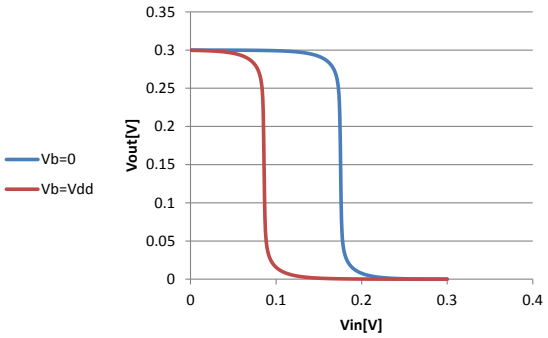

Figure 9: Simulated transfer characteristics of the first inverter in figure 7

On the other hand, a transient simulation of Schmitt trigger represented in Figure 7 has been implemented using input signal of sinuous wave with $amplitude = 0.15V$, $V_{offset} = 0.15V$ and $frequency = 10KHZ$. Power supply is equal to $V_{DD} = 0.3V$ and W/L ratio of all transistors is equal to 30/1u. Simulation results are introduced in Figure 10 which are very close to theoretical calculation in this paper.

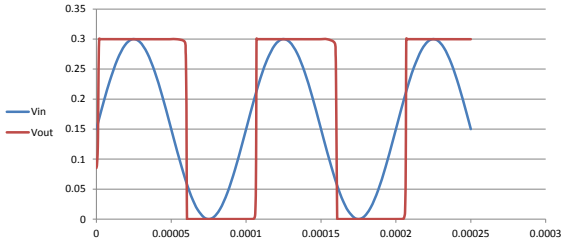

Figure 10: Transient Response of The Proposed Schmitt Trigger for Vdd=0.3V

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Furthermore, a second transient simulation has been performed with power supply down to 0.2V, shows an increment in the ratio of hysteresis to power supply, which confirm the theoretical fact in equation 28 that the hysteresis is independent on power supply voltage as shown in Figure 11.

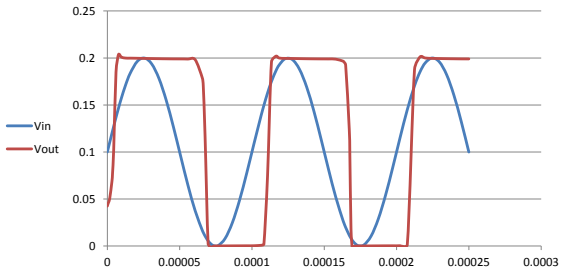

Figure 11: Transient Response of The Proposed Schmitt Trigger for Vdd=0.2V

Finally, the power dissipation of the trigger has been simulated as a function of input voltage. A DC sweep analysis has been implemented by varying V_{in} from 0V to 0.3V. The results are illustrated in figure 12 showing that the overall current I_{DD} provided by power supply $V_{DD} = 0.3V$ has its maximum value between the two switching voltages V^+ and V^- which is 17nA, resulting power dissipation equals $0.3 \times 17 = 5.1nW$.

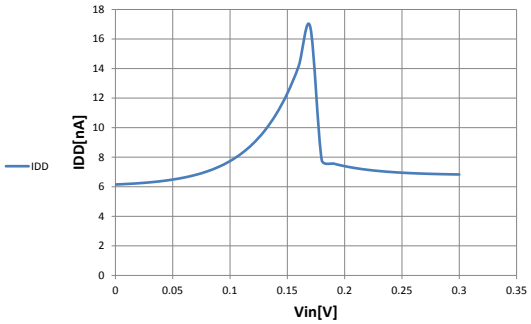

Figure 12: Voltage supply current as function of V_{in}

8 Conclusion

An ultra low voltage Schmitt trigger has been introduced. The trigger depends on dynamic bulk biasing of bulk-source junction of MOSFET and thus reducing threshold voltage and power supply down to 0.2V. The simulation show good correspondence with theoretical terms and independence of trigger hysteresis to power supply variations.

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