Design of CMOS Schmitt Trigger

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Abstract— This paper presents comparison among various Schmitt triggers on the basis of their hysteresis width and average power consumed. Hysteresis width is improved by using two feedback loops as compared to conventional CMOS Schmitt trigger whose hysteresis width is fixed. All Schmitt trigger circuits have been realized using .25um and .18µm CMOS technology and simulation results are presented.

Index Terms— Hysteresis Width, Static Power Dissipation, Dynamic Power Dissipation.

I. INTRODUCTION

Schmitt triggers are bistable networks that are widely used to enhance the immunity of a circuit to noise and disturbances. It is good as a noise rejecter. Schmitt trigger make use of waves, therefore it is widely used for converting analog signals into digital ones and to reshape sloppy, or distorted rectangular pulses. Hysteresis of the trigger eliminates noise making a cleaner and more reliable signal. The output of a Schmitt trigger changes state when a positive going input passes the upper trigger point (UTP) voltage and when negative going input passes the lower trigger point voltage. The conventional Schmitt trigger has fixed hysteresis width [1].

This paper shows how to increase the hysteresis width of conventional Schmitt trigger by using two layers of feedback devices. In section II design of conventional Schmitt trigger is described. In section III, circuit to increase the hysteresis width is described with the description of adjustable Schmitt trigger. In section IV comparison between conventional Schmitt trigger and new Schmitt trigger on the basis of hysteresis width, static power dissipation and dynamic power dissipation is discussed. These circuits use a standard CMOS technology. The experimental results are presented in Section IV.

II. DESIGN OF CONVENTIONAL CMOS SCHMITT TRIGGER

In this section, design of Schmitt trigger which covers transient as well as dc analysis will be discussed [2]. Effect of W/L on hysteresis curve will also be discussed. The Schmitt circuit is a general inverter circuitry (double transistor inverter) with two extra transistors for providing the hysteresis. The double transistor inverter is used because the transistors (M2 and M5) have some higher threshold voltage than M1 and M4 due to body bias effect and due to which the output switches to high from low or low from high when after the ON condition of M2 or M4 respectively.

Now after addition of two more transistors M6 and M3 the circuit is capable to provide hysteresis [3]. When 0 input voltage is applied at the input, both M1 andM2 are in OFF condition while M4 and M5 are in ON condition and output is at high logic level. When the input reaches to threshold voltage of M1 transistor then M1 will be on , while M2 remains OFF and at this time output will be high M3 will be on , so M1 Try to pull down the node between M1 and M2 while M3 try to pulls up this node to voltage VDD-VT , so transistor M2 stays the output to HIGH logic level , now when the input rises up to the threshold voltage of M2 then output switches to low logic level, so effectively our switching point shifted to higher voltage referred as VIH. Similar in case when input is falling from higher logic level then PMOS's comes into picture and switching point at output is shifted to some lower voltage referred as VIH. The difference between the VIH and VIL is referred as HYSTERISIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output , the output logic level's will remain same. Similar in case when input is falling from higher logic level then PMOS's comes into picture and switching point at output is shifted to some lower voltage referred as VIH. The difference between the VIH and VIL is referred as HYSTERISIS voltage. This refers to an extra amount of voltage added to low logic level at output or subtracted to high logic level at output , the output logic level's will remain same. If we examine the conditions from transistors (M1, M2, M3). When output switches from high to low just before that: M2 in off condition. M1 and M3 in saturation condition.

$$I_{DM3} = \beta_3/2\left(V_{GS} - V_{TH3}\right)^2$$
$$= \beta_3/2\left(V_{DD} - \left(V_{in} - V_{TH2}\right) - V_{TH3}\right)^2$$
$$= \beta_3/2\left(V_{DD} - V_{in} + V_{TH2} - V_{TH3}\right)^2$$

But
$$V_{TH2} = V_{TH3}$$
$$I_{DM3} = \beta_3/2\left(V_{DD} - V_{in}\right)^2$$
$$I_{DM1} = \beta_1/2\left(V_{GS} - V_{TH1}\right)^2$$
$$= \beta_1/2\left(V_{in} - V_{TH1}\right)^2$$
$$I_{DM1} = I_{DM3} \quad \text{(Both are in saturation)}$$
$$\beta_3/2\left(V_{DD} - V_{in}\right)^2 = \beta_1/2\left(V_{in} - V_{TH1}\right)^2$$
$$V_{DD} - V_{in} = \sqrt{\beta_1/\beta_3}\left(V_{in} - V_{TH1}\right)$$
$$V_{in} = \left[V_{DD} + \left\{\sqrt{(\beta_1/\beta_3)}\right\}V_{TH1}\right]\Big/\left\{1 + \sqrt{\beta_1/\beta_3}\right\}$$

This Vin is called VIH. Now Similarly for the VIL.
Transistors M4 and M6, will be in saturation.

$$I_{DM6} = \beta_6/2\left(V_{SG} - |V_{TH6}|\right)^2$$

$$= \beta_6/2\left(0 - \left(V_{in} - V_{TH5}\right) - V_{TH6}\right)^2$$

But

$$V_{TH5} = V_{TH6}$$

$$= \beta_6/2\left(V_{in}\right)^2$$

$$I_{DM4} = \beta_4/2\left(V_{SG} - |V_{TH4}|\right)^2$$

$$= \beta_4/2\left(V_{in} - V_{DD} - V_{TH4}\right)^2$$

$$I_{DM4} = I_{DM6}$$

(Both are in saturation)

$$\beta_6/2\left(V_{in}\right)^2 = \beta_4/2\left(V_{in} - V_{DD} - V_{TH4}\right)^2$$

$$V_{in} = \sqrt{(\beta_4/\beta_6)}\left(V_{DD} - |V_{TH4}|\right)/1 + \sqrt{(\beta_4/\beta_6)}$$

This $V_{in} \approx V_{IL}$

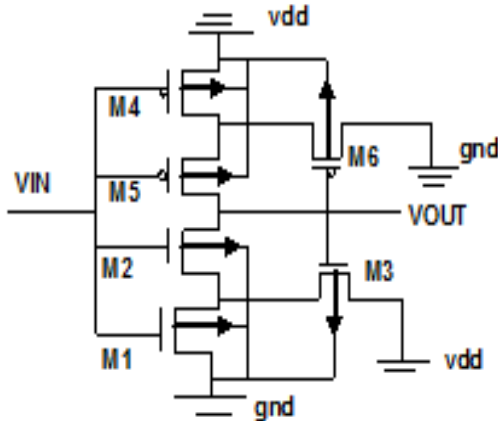The circuit designed for V_{IL} = 2V and V_{IH} =3 is shown in Fig. 1. And results are shown in Fig. 2 and Fig.3.

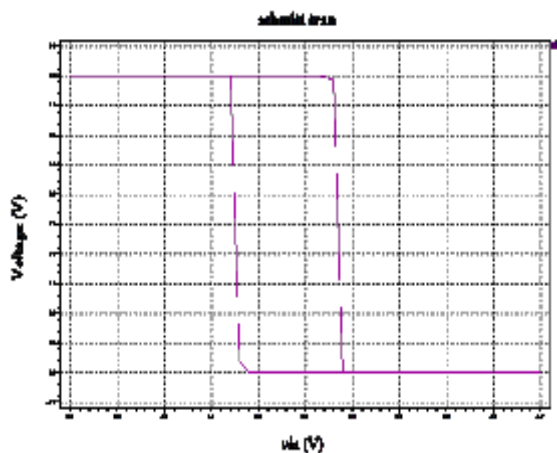**Fig.1 Conventional CMOS Schmitt Trigger**
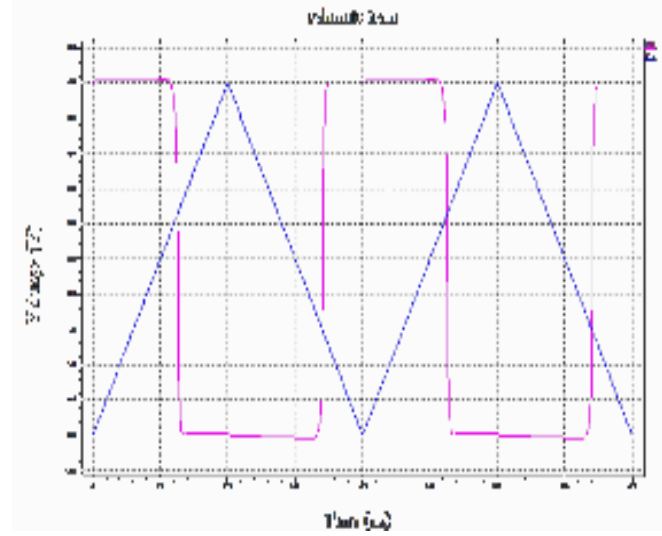

Fig. 2 DC Analysis

Fig. 3 Transient Analysis

A. Effect of Variation of W/L Ratio of Transistors on Hysteresis Curve

On increasing the W/L of transistor M1 the curve will shift towards the LEFT side, because in this case our NMOS will strong and pulls the output sharply to low logic level. Second case when M4 will strong then it will maintain the output to logic level high for greater duration so the curve will shift to RIGHT side. There will no effect on the hysteresis curve on changing the sizes of transistors M2 and M5. This can be also verified from the equations derived for VIH and VIL in previous section.
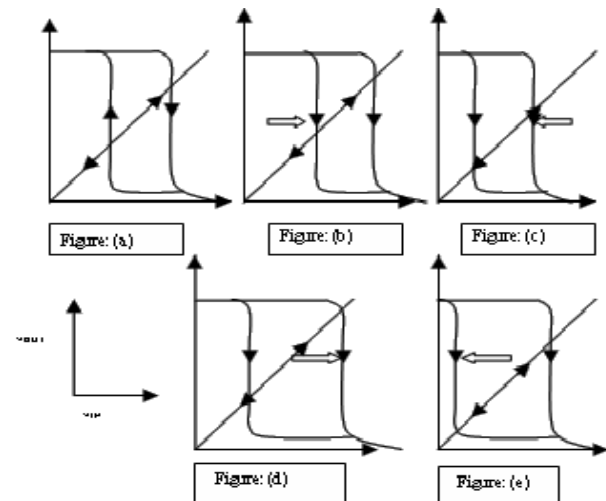

Fig. 4 Effect of W/L Ratio of Various Transistors on Hysteresis Curve. A) Typical Case, B) When W/L of M4 Increases, C) When W/L of M1 Increase, D) When W/L of M3 Increase, E) When W/L of M6 Increase

If the size of transistor M3 is increased then it will affect only on VIH level, because when we increase from low to high then lower portion of SCHMITT comes into picture to control the VIH level, hence by increasing the size the VIH will increase while in same way transistor M6 affect only on VIL level. When size of M6 is increased then VIL will be reduced. We can also conclude that the aspect ratio of M4

and M4 transistors affect the VIL level while the aspect ratio of M1 and M3 affect the VIH level. The area of hysteresis curve determines the amount of noise immunity provided be the circuit. Greater the difference between the VIH and VIL level means more immunity. Hysteresis width of conventional CMOS Schmitt trigger is increased by new circuit which consist of two layers of feedback devices. This new circuit will be discussed in the next section. The effect of varying W/L is shown in Figure 4.
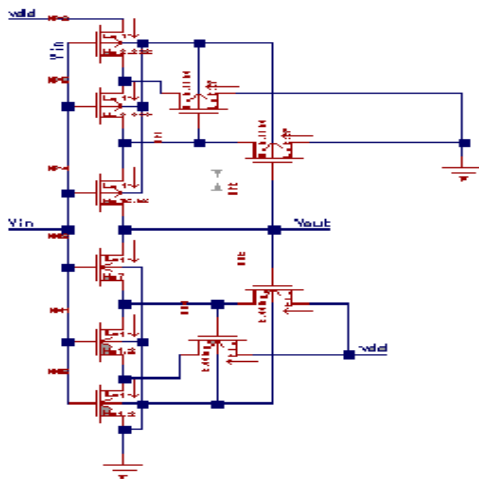
B. Circuit to Improve the Hysteresis Width

Fig. 5 New Circuit to Improve Hysteresis Width

Large hysteresis width can be achieved with two layers of feedback devices for both VIH and VIL trigger edges. Design considerations are almost same as in conventional Schmitt trigger. Hence higher VIH and lower VIL can be achieved by two layers of feedback devices [4]. The circuit is shown in Fig 5. And transient analysis is shown in Fig. 6.
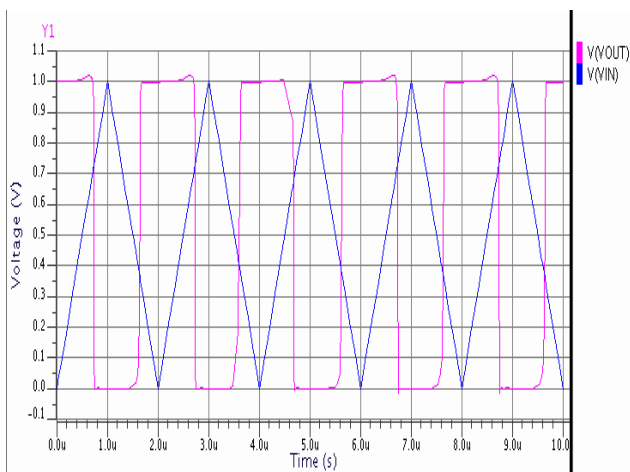

Fig. 6 Transient Analysis of New Circuit at 1V

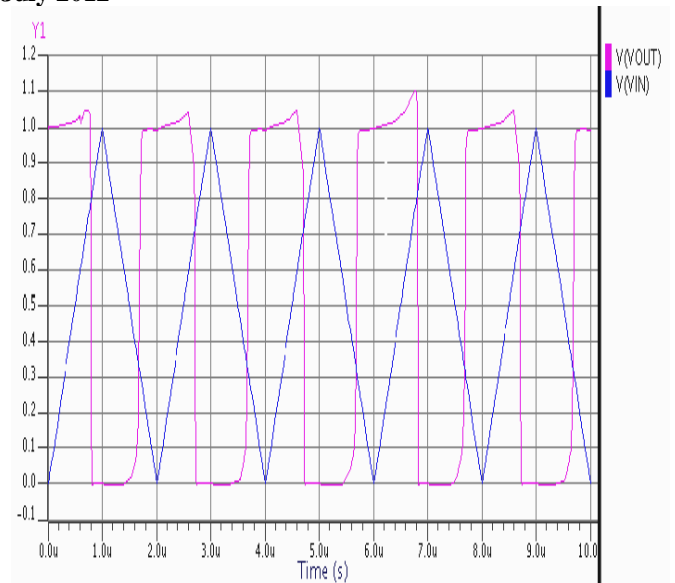Transient analysis of conventional Schmitt trigger at 1V is shown in Fig.7.

Fig: 7 Transient Analysis of Conventional Schmitt at 1V

III. SIMULATION RESULTS

For the simulation of conventional and new circuit BSIMV3 Ver 3.1 models of TSMC 0.18μm CMOS process were used. Tanner tool with 0.25μm CMOS process were also used to compare the hysteresis width and average power consumed of conventional and new Schmitt trigger circuits. Simulations results are reported in Table 1 and Table 2. These results show that high hysteresis width is achieved with modified Schmitt Trigger.

Table 1. Comparison between Hysteresis Width, Static Power Dissipation, and Dynamic Power Dissipation.

Voltage (V)	Hysteresis width Old/new circuit	Dynamic power dissipation Old/new (nW)	Static power dissipation Old/new (pW)
0.8	0.33/0.45	245.4 / 297.952	11 / 25.8
0.9	0.33/0.45	392.6664 / 555.273	13 /29.7
1.0	0.33/.5	612.7 / 729.63	15 /23.8
5	1/2	0.5550 / 0.585	215.187 / 452.3

Table 2. Comparison Between Hysteresis Width and Average Power Consumed.

Voltage (Volt)	Hysteresis Width (Volt) Old / New	Average Power Consumed (watts)
5V	1.2 / 2.1	7.999 e – 004 / 3.930 e – 004
3V	0.8 / 1.3	2.4499 e – 004 / 8.0565 e

		– 004
1.5V	0.4 / 0.85	1.08310 e – 004 / 1.1150 e – 004

IV. CONCLUSION

The new Schmitt trigger provides larger hysteresis width as compared to conventional Schmitt trigger. The dynamic power dissipation is almost comparable but static power dissipation of new circuit is almost double as compared to conventional one. This circuit is useful where we require large hysteresis width to improve noise margin.

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