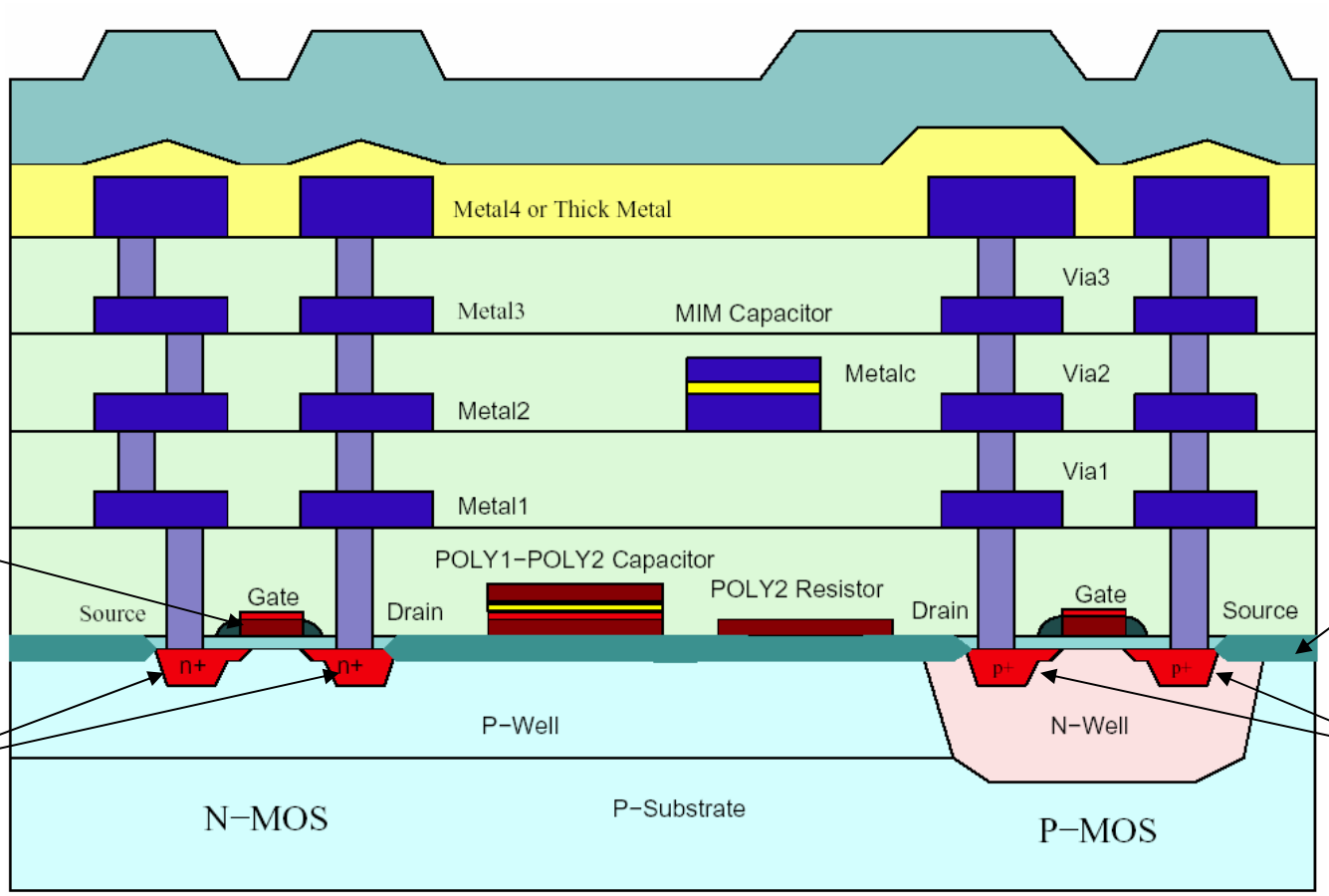
# ECEN4827/5827

Process example: 0.35u CMOS
Spice models

Introduction to schematic capture and Spice simulations
using LTspice

8/22/2008

# Typical CMOS process (minimum channel length: 0.35µm)



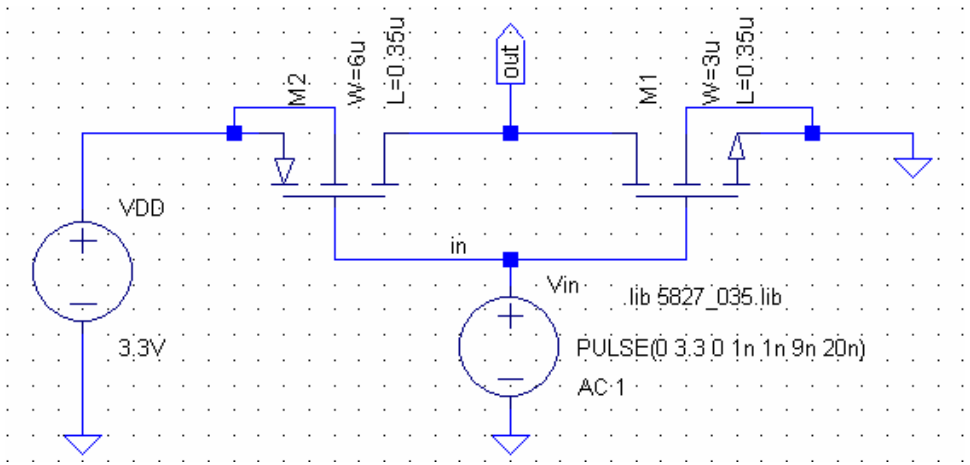

Polysilicon (POLY): NMOS and PMOS gates

n+ diffusion (S and D of NMOS)

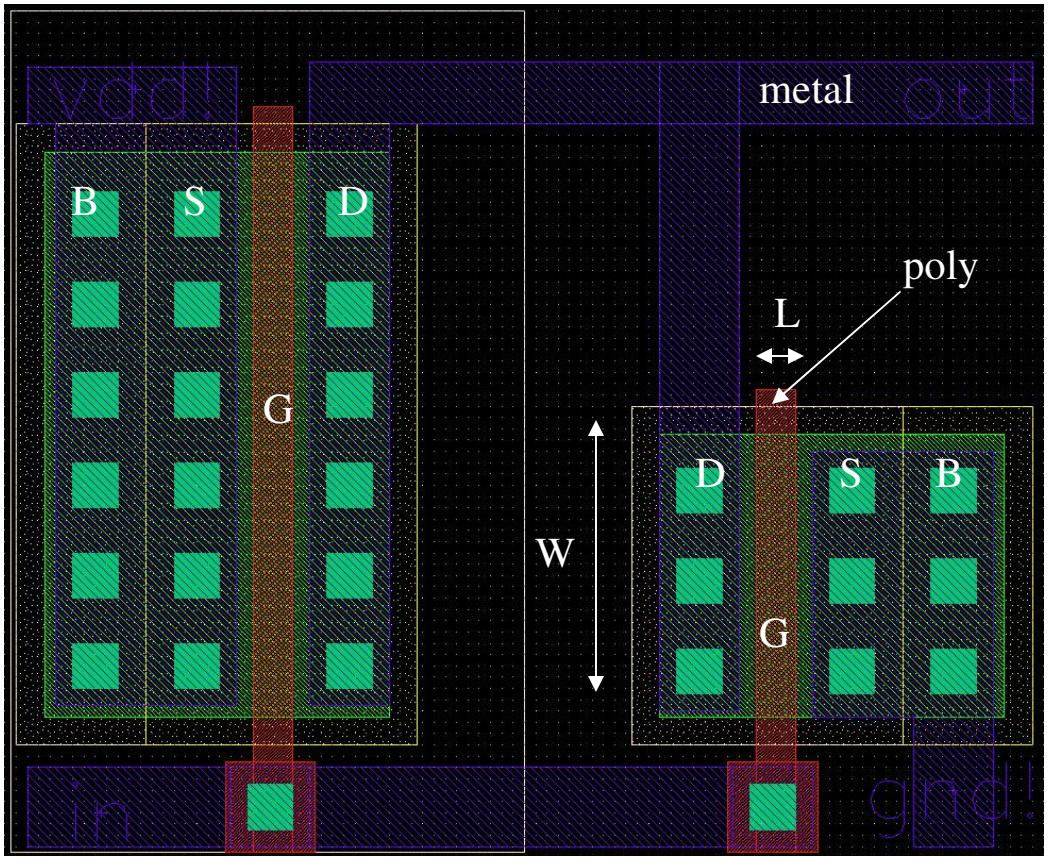
Thick field $SiO_2$ oxide (FOX)

p+ diffusion (S and D of PMOS)

- *p* substrate
- *p* well (body) for NMOS transistors, *n* well (body) for PMOS transistors
- *n*+ and *p*+ source/drain diffusions
- 1 or more polysilicon layers (2 POLY layers in this example)
- 2 or more metal layers (4 metal layers in this example)



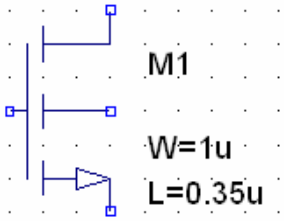

inverter_intro.asc




layout

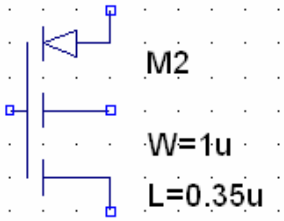
# Spice model library: 5827_035.lib

NMOS
nmos_035.asy



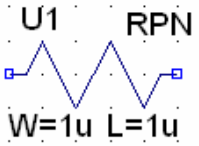

NMOS transistor
B (*p* substrate) must be tied to most negative supply rail

PMOS
pmos_035.asy



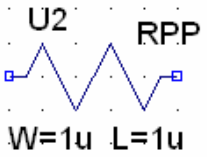

PMOS transistor
B is *n*-well, usually most positive supply rail

RPN
rpn_035.asy



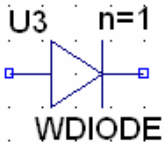

Rsheet = 1.2 kΩ/square, TC = –400 ppm/°C
"square" = L/W

RPP
rpp_035.asy




Rsheet = 50 Ω/square, TC = +830 ppm/°C
"square" = L/W

WDIODE
wdiode.asy



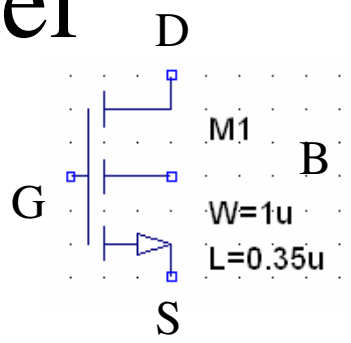

Unit-area (5µ*5µ) *p*+ diffusion to *n*-well diode
*n* = area multiple. Cathode must be tied to the most negative supply rail

# Example: NMOS model

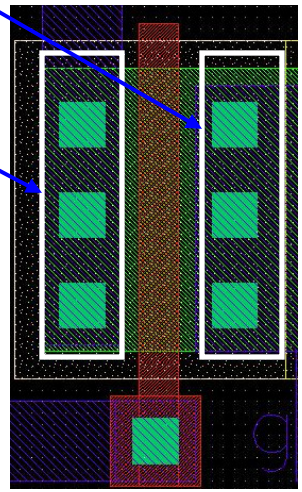
```
*---------------------------------------------------------------------------
.subckt NM D G S B
+params: W=10u L=1u
M1 D G S B NM L={L} W={W} AS={2u*W} PS={2*(2u+W)} AD={2u*W} PD={2*(2u+W)}
.ends

* ---------------------------------------------------------------------------
* NMOS transistor model
* ---------------------------------------------------------------------------
.MODEL NM NMOS LEVEL=8
* ---------------------------------------------------------------------------
************************* SIMULATION PARAMETERS ************************
* ---------------------------------------------------------------------------
* format    : LTspice
* model     : MOS BSIM3v3
* ---------------------------------------------------------------------------
*                          TYPICAL MEAN CONDITION
* ---------------------------------------------------------------------------
*         *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00
+NOIMOD =3.000e+00
*         *** Threshold voltage related model parameters ***
+K1      =5.0296e-01
+K2      =3.3985e-02 K3      =-1.136e+00 K3B     =-4.399e-01
+NCH     =2.611e+17 VTH0    =4.979e-01
+VOFF    =-8.925e-02 DVT0    =5.000e+01 DVT1    =1.039e+00
+DVT2    =-8.375e-03 KETA    =2.032e-02
+PSCBE1 =3.518e+08 PSCBE2 =7.491e-05
```

… more (BSIM3 model is very detailed and complicated)…




nmos_035.asy



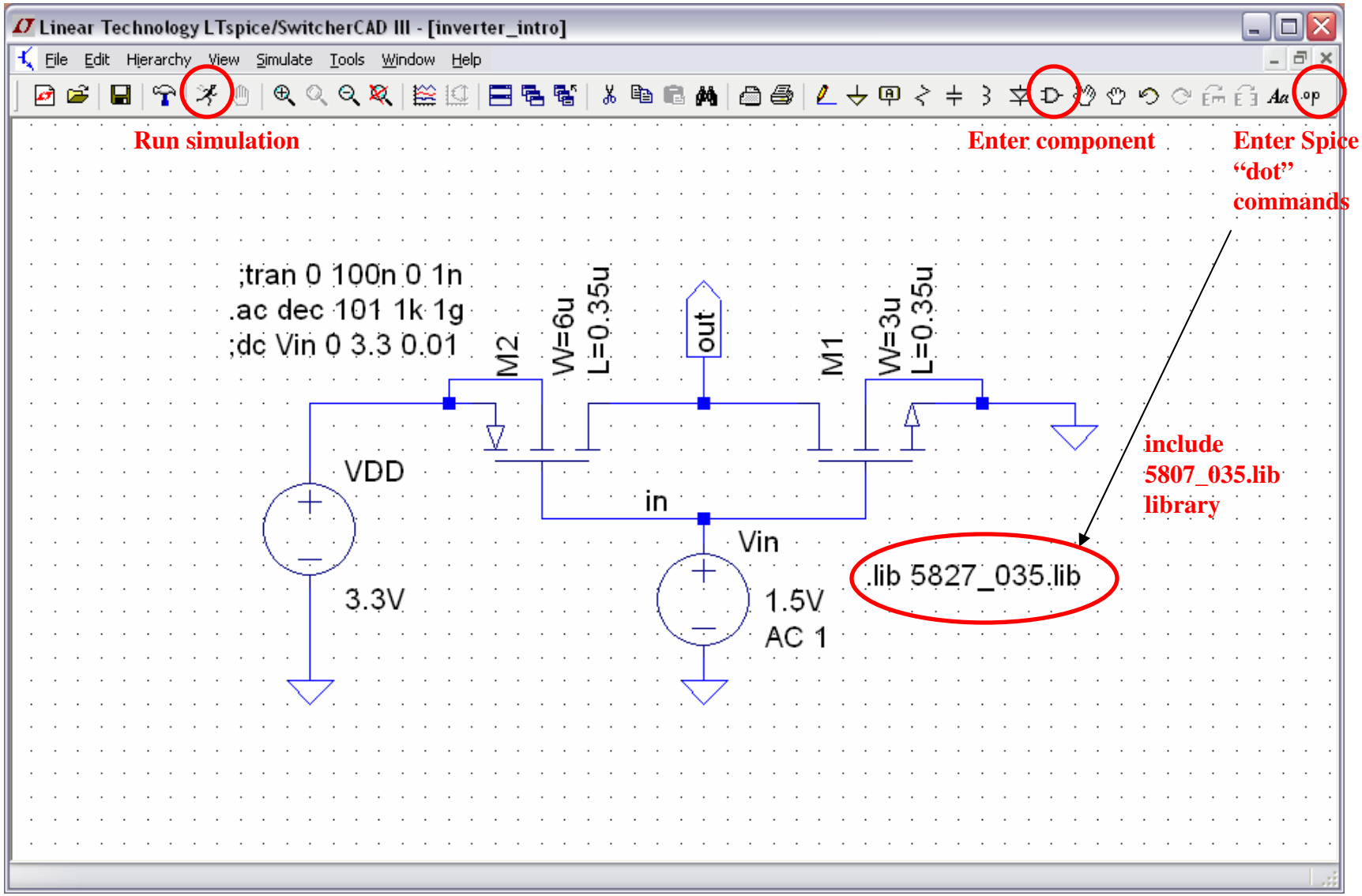
- W, L are circuit design parameters, minimum 0.35µ, minimum increment 0.1µ
- NMOS Spice model can be used as is a subcircuit, which allows automatic adjustments of AS (source area), PS (source perimeter), DS (drain area) and PD (drain perimeter) as functions of W, or as a native MOS device (user must then manually specify AS, PS, DS, PD)
- Very detailed BSIM3 model (industry standard)

# Setting up 0.35u CMOS symbols and model library for LTspice

- Option 1: local (does not require administrative privileges)
  - Place all symbol files (***.asy** files) and model library (**5827_035.lib**) in a working folder, together with schematics
- Option 2: make symbols and model library globally available
  - Place all symbols (***.asy** files) in a new folder (e.g. 5827) in **C:\Program Files\LTC\SwCADIII\lib\sym**
  - Add model library **5827_035.lib** to **C:\Program Files\LTC\SwCADIII\lib\sub**
- In all cases, an LTspice schematic must include:

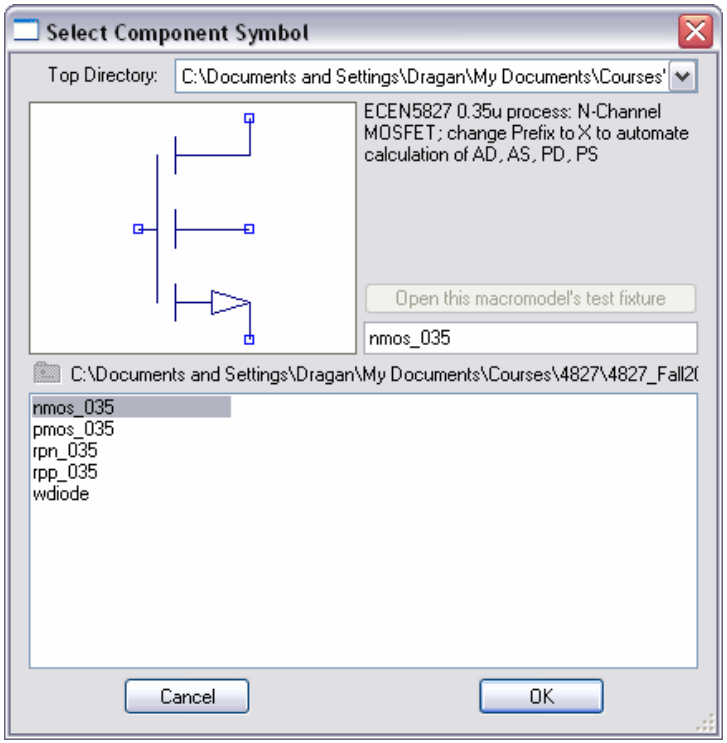
  **.lib 5827_035.lib**

# LTspice schematic entry

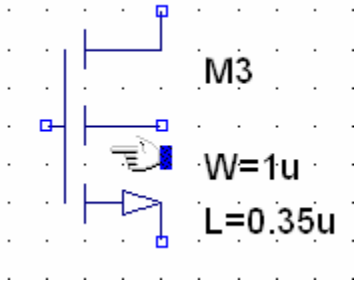


# Use of NMOS symbol in LTspice

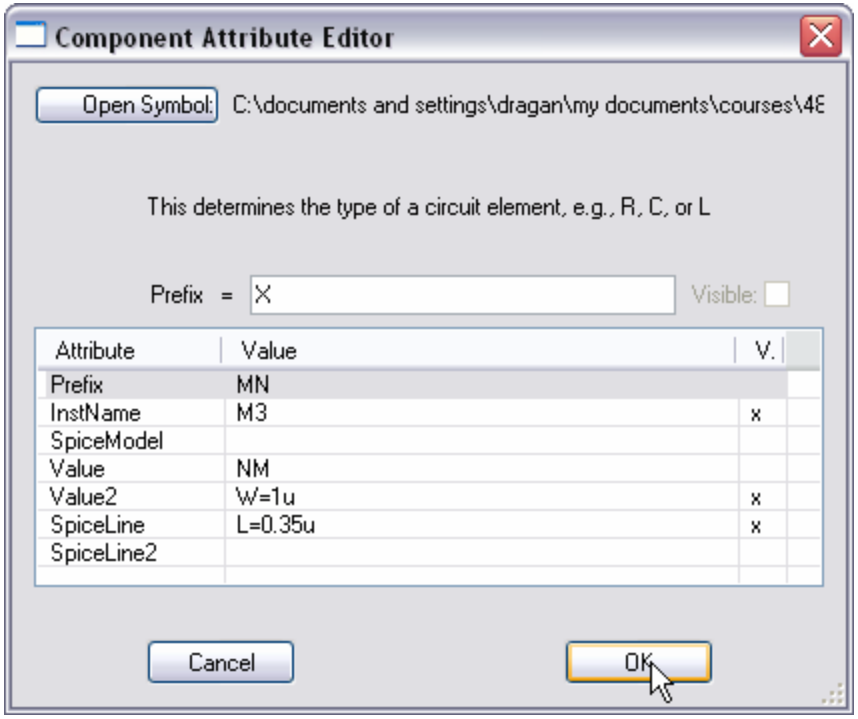
(1) place **nmos_035** symbol




(2) **CTRL-right click** to open Attribute Editor




(3) Change **Prefix to X** to use subcircuit model with automatic adjustments of AS, PS, AD, PD

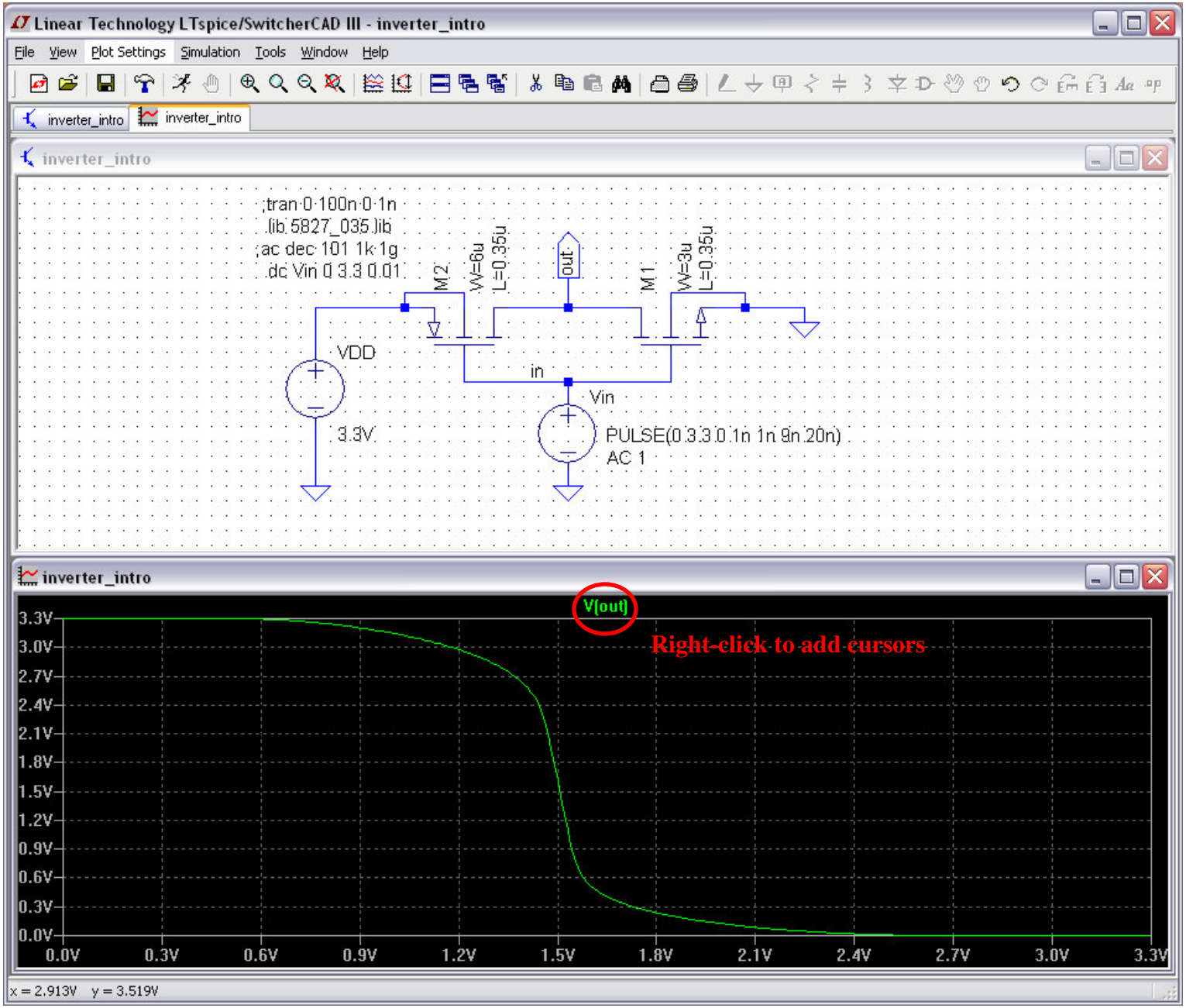



The same applies to **pmos_035**

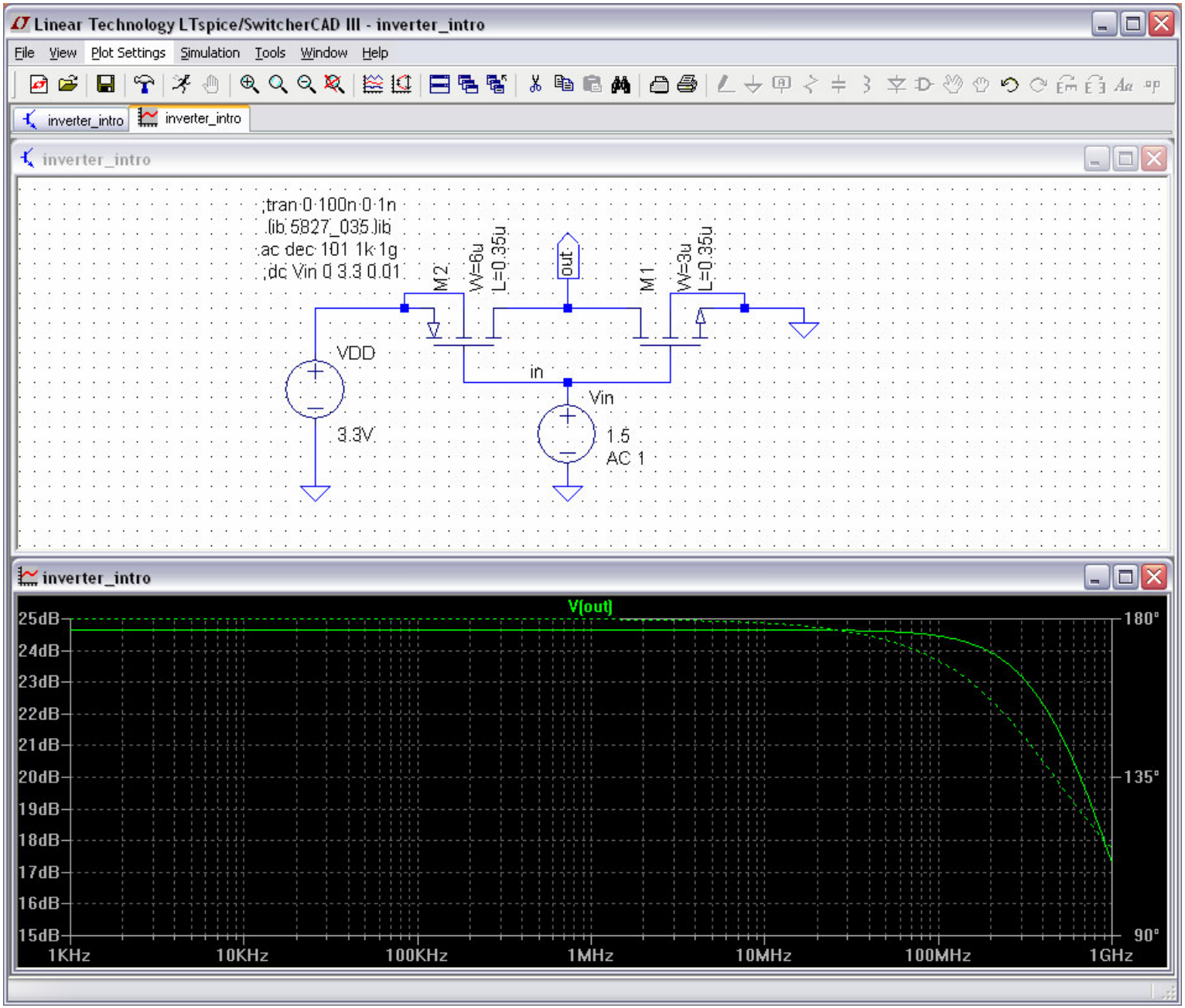
# Basic Spice simulations

- Bias Point (.op)
  - View DC operating point voltages and currents, and device small-signal model parameters in (text)
- DC Sweep (.dc)
  - Plot DC (or temperature) characteristics
- AC Sweep (.ac)
  - Plot small-signal frequency responses
- Transient (.tran)
  - Plot large-signal (total) waveforms

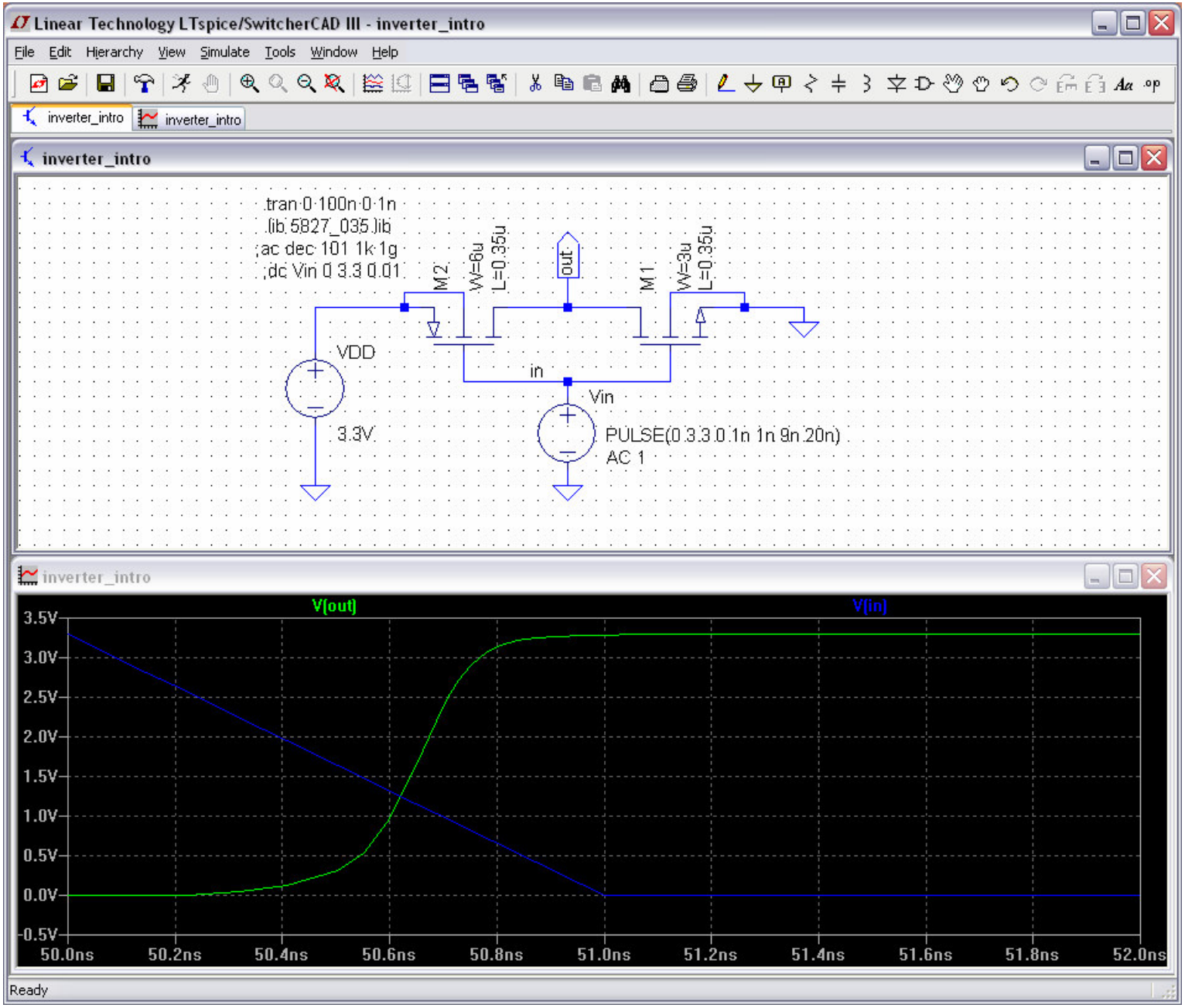
# DC sweep example: inverter $V_{OUT}$ versus $V_{IN}$



AC sweep example: inverter as an amplifier, magnitude response $\|v_{out}/v_{in}\|$ [dB]

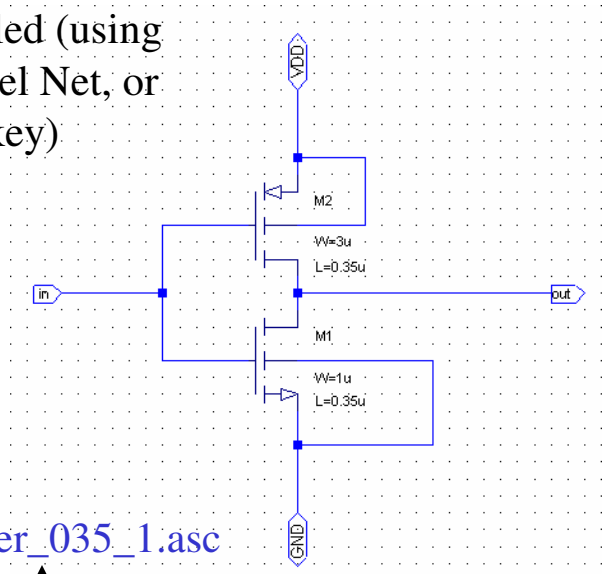


# Transient example: inverter $v_{OUT}(t)$ for pulsating $v_{IN}(t)$

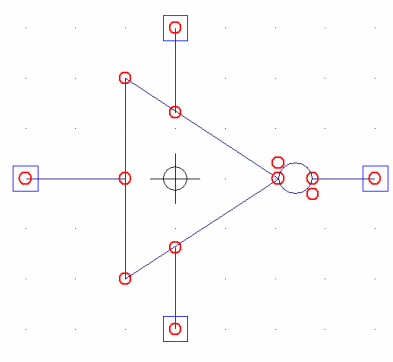


# Hierarchical schematic entry

Inverter circuit with ports labeled (using Edit, Label Net, or F4 key)




Symbol representing the inverter circuit

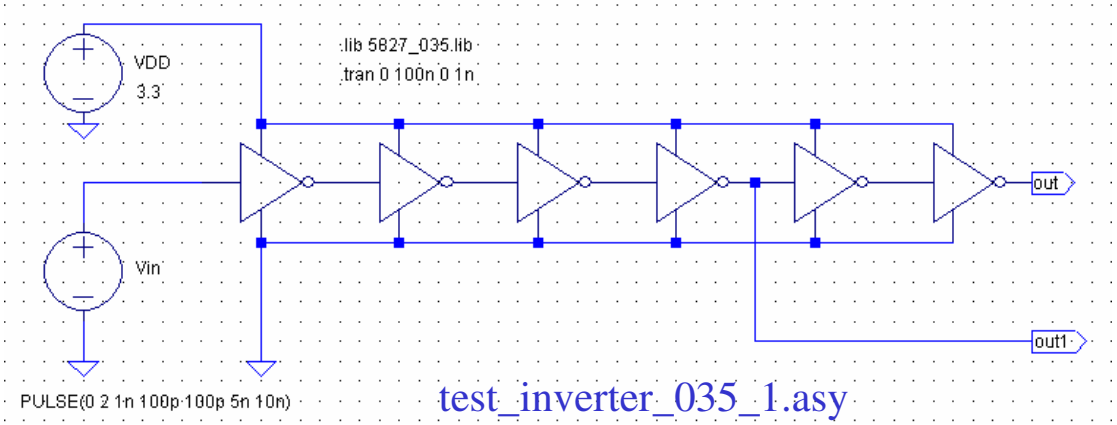


inverter_035_1.asc

inverter_035_1.asy

names must match

Symbols used to enter larger circuits




test_inverter_035_1.asy