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Low Power Schmitt Trigger in Sub-threshold Region

Sapna and Prof. B. P. Singh

Abstract **- Sub-threshold operation holds promise for ultra low energy operation in emerging applications. Sub-threshold operation is attractive for mid to high performance applications where power has become a limiting constraint. This paper proposes a low power Schmitt-Trigger using CMOS standard cell logic. Experimental results reveal that proposed design has reduced power consumption and has temperature sustainability. The paper also presents the application of Schmitt Trigger in SRAM. The simulation work has been done on Tanner EDA tool at 45nm technology.**

Keywords **– Schmitt Trigger, power consumption, sub-threshold, CMOS Technology, Tanner EDA.**

I. Introduction

Low power device design is now a vital field of research on account of increase in demand of portable devices. Environmental monitoring or emerging miniaturized energy autonomous systems e.g., for healthcare especially require circuits with extremely tight energy budgets to enable functionality at practical device sizes, motivating further research in this direction [1]. Active power reduction is a critical challenge to translate increasing levels of integration to architectural performance enhancement [2]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly [3].

The supply voltage scaling is the major focus of low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a MOS. Sub-threshold current of a MOSFET device occurs when the gate-to-source voltage (V_{GS}) of the device is lower than its threshold voltage (V_t) [4].

Sapna

FET, MITS, Lakshmangarh, Sikar (Rajasthan)

India

sapna0111@gmail.com

Prof. B. P. Singh

FET, MITS, Lakshmangarh, Sikar (Rajasthan)

India

bpsingh@ieee.org

When V_{GS} is lower than V_t, there are less minority carriers in the channel, but their presence comprises a current and the state is known as weak inversion. In standard CMOS design, this current is called sub-threshold parasitic leakage, but if the supply voltage (V_{DD}) is lowered below V_t, the circuit can be operated using the sub-threshold current with ultra low average power consumption.

The Schmitt Trigger (ST) is a comparator that incorporates positive feedback. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. ST is used to modulate the switching threshold of an inverter depending on the direction of the input transition. The output state depends upon the input level and will change only as the input crosses a predefined circuit threshold. Therefore Schmitt Triggers are bistable networks that are widely used to enhance immunity of circuits to noise and disturbances [5]. The ST circuit has a dc transfer characteristic like an inverter, but with different switching thresholds depending on whether input signal is increasing or decreasing. ST can be used as a CMOS logic inverter. It has a number of applications in sub-threshold SRAM [3], frequency doublers [6], image sensors [7].

II. Existing Schmitt Trigger

The existing Schmitt Trigger circuit consists of three pMOS devices P1, P2, P3 and three nMOS devices N1, N2, N3 as shown in Figure 1 [8]. ST circuit has two different high-to-low (V_H) and low-to-high (V_L) transition threshold voltages which make the circuit to have better noise immunity than the inverter. When the threshold voltage of the existing ST circuit is high, input signal goes up to V_{DD} from ground. In other words, output signal is pulled low as input signal exceeds V_H. Similarly, when the threshold voltage of the existing ST circuit is low, input signal goes down to ground from V_{DD}. In other words, output signal is pulled up as input signal is lower than V_L. Hence, the noise immunity of the existing ST circuit is better than that of inverter [9].

Initially input voltage (V_{IN}) in Fig. 1 is equal to 0V, to turn on the two stacked pMOS transistors P1 and P2. Hence output voltage (V_{OUT}) will be equal to V_{DD}.

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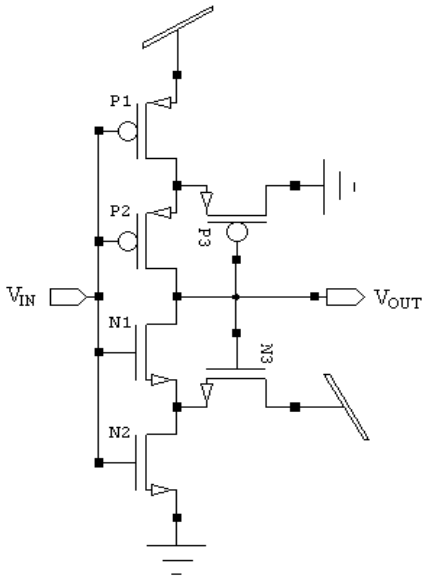

Figure 1. Existing Schmitt Trigger.

When V_{IN} rises to threshold voltage of nMOS (V_{tn}), N2 will turn on but N1 remains off since N3 is on and hence source voltage of N1 becomes V_{DD}-V_{tn}. Now N2 and N3 are forming an inverting nMOS amplifier. Thus the source voltage of N1 is falling with increasing V_{IN}. When source voltage of N1 drops to V_{tn}, N1 becomes on. Here both N1 and N2 are on, causing V_{OUT} to be driven to 0V rapidly so that N3 becomes off. When V_{IN} falls below the threshold voltage of pMOS ($|V_{tp}|$), P1 will turn on but P2 remains off since P3 is on, forcing the source voltage of P2 to 0V. Now P1 and P3 are forming an inverting pMOS amplifier. Thus source voltage of P2 is rising with decreasing V_{IN}. When source voltage of P2 rises to $|V_{tp}|$, P2 becomes on. V_{OUT} approaches to V_{DD} rapidly as P1 and P2 are on to drive P3 off.

The major drawback of this circuit is the high power consumption. This is due to the leakage current flowing through N2 when V_{IN} is low that is N1, N2 are in off state along with P1, P2 and N3 in on state. As transistors are of small size, leakage current will also flow through N1 due to drain induced barrier lowering (DIBL) effect.

III. Proposed Schmitt Trigger

The existing ST is modified by removing two nMOS transistors N2 and N3. The proposed ST circuit uses four transistors P1, P2, P3, and N1 as compared to the existing ST which uses six transistors as shown in Fig. 2.

Thus the area requirement for the circuit is reduced along with the reduction in the leakage current as the transistors N2 and N3 are removed. So if V_{IN} is low, P1 and P2 become on and N1 becomes off. Therefore no leakage current will flow through N1 during its off state and no DIBL effect will occur in N1. Hence power consumption is reduced. The proposed ST gives the full output swing operating at smaller input voltages.

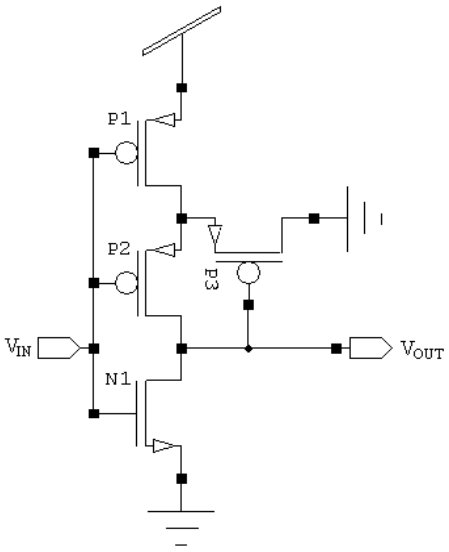

Figure 2. Proposed Schmitt Trigger.

IV. Simulation and Analysis

A. *Simulation Environment*

In low power applications area, average power consumption and delay introduced by the device are the main technological aspects to prefer a design over its counterparts. The proposed ST is an area efficient design as it is producing better results with less number of transistors.

The existing and the proposed circuits have been simulated using Tanner EDA Tools version 13.0. Average power consumption and delay produced are measured at various temperatures. While working in sub-threshold region the voltage value is taken below the threshold value that is 0.40V at all temperatures. For fair comparison, the aspect ratio of all transistors is taken to be 1. The circuits are compared at 45nm technology. The transient response of the proposed ST is shown in Fig. 3.

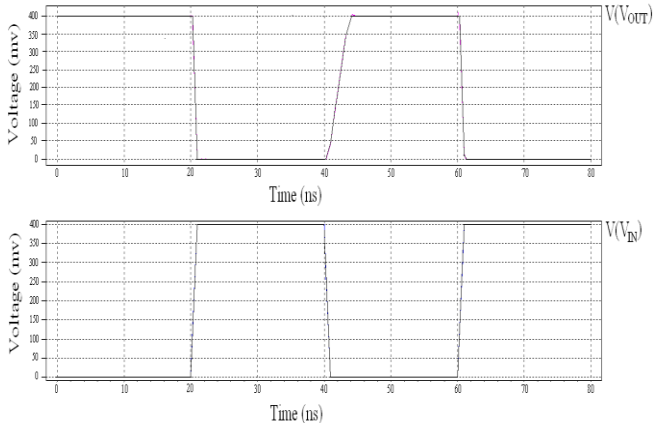

Figure 3. Input Output waveforms of the proposed circuit.

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B. *Simulation Comparison*

Proposed ST consumes less power and has high performance as compared to the existing ST in terms of power, delay and power-delay product at various temperatures. Following bar graphs represent the variation of the average power consumption and delay as shown in Fig. 4 and Fig. 5 respectively. From bar graphs, it can be seen that power consumption and delay of the proposed Schmitt Trigger are less than existing Schmitt Trigger. Also power consumption and delay both, for the proposed and the existing circuits, increases with the temperature.

The quantitative approach showing the variations of the Power-Delay Product (PDP) at different temperatures is presented in Table I. It clearly depicts that PDP for proposed Schmitt Trigger is much lower than existing Schmitt Trigger.

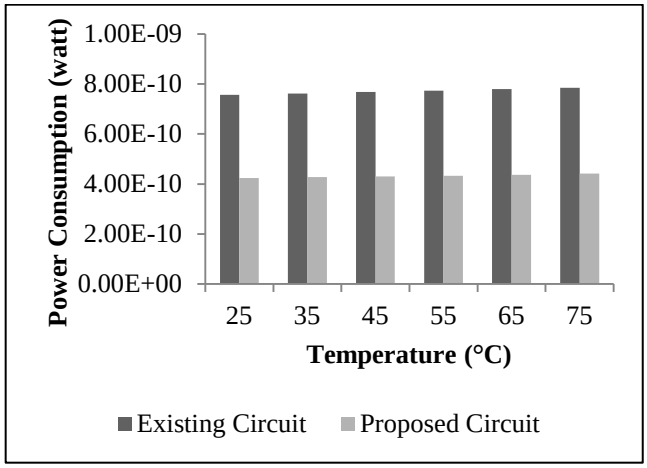

Figure 4. Power Consumption at various temperatures.

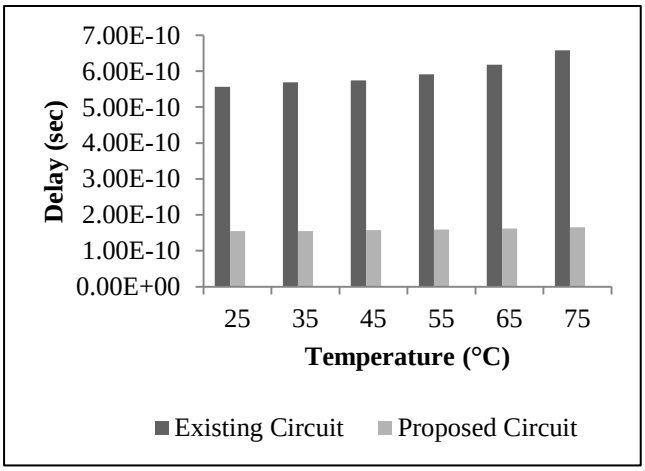

Figure 5. Delay at various temperatures.

TABLE I. POWER-DELAY PRODUCT AT DIFFERENT TEMPERATURES.

Temperature (°C)	PDP (watt-sec)	
	Existing schmitt trigger	*Proposed schmitt trigger*
25	4.2092e-19	6.5572e-20
35	4.3337e-19	6.6415e-20
45	4.4148e-19	6.7534e-20
55	4.5681e-19	6.8943e-20
65	4.8159e-19	7.0630e-20
75	5.1678e-19	7.2543e-20

v. Application of Schmitt Trigger

The ongoing demand for reduction in energy consumption has motivated the design of low voltage, low power digital circuits; which are reliable even for complex systems and memories [1]. The amount of memory required in a particular system depends on the type of the application. SRAM utilizes a flip flop mechanism, which uses static latches and these operate in a manner similar to the way in which memory cells work. One of the most important applications of ST is in SRAMs. To reduce the power consumption of SRAMs operating at low voltages, a Schmitt Trigger based SRAM cell has been proposed.

A. *Proposed SRAM Cell using Schmitt Trigger*

The proposed SRAM cell requires no architectural change compared to the 6T cell architecture except that the cross coupled inverter pair is replaced by the proposed Schmitt Trigger pair as shown in Fig. 6. It can be used as a drop-in replacement for 6T cell. The proposed Schmitt Trigger based SRAM cell gives reduced power consumption.

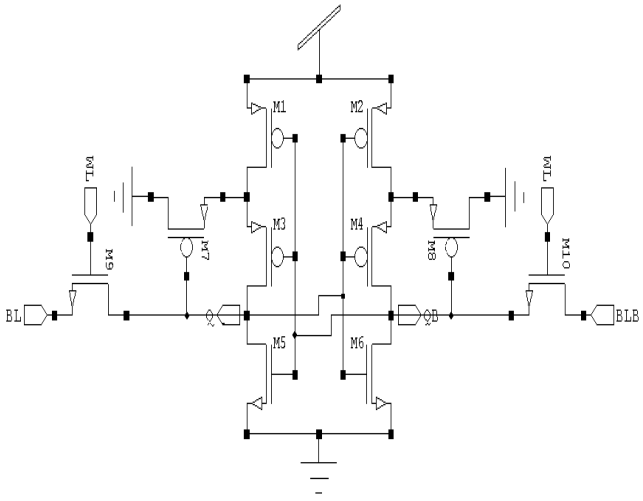

Figure 6. Proposed SRAM cell.

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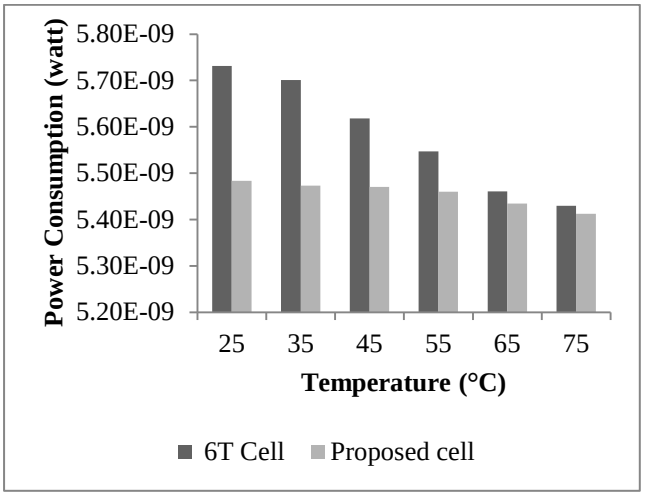

Figure 7. Power Consumption at various temperatures.

Fig. 7 shows the comparison between existing SRAM 6T and proposed SRAM cell in terms of power consumption at different temperatures. It can be seen from the bar graph that the modified cell i.e. the proposed cell consumes less power as compared to the existing cell.

VI. Conclusion

The need of low power consumption and improvement in efficiency in the digital systems is increasing day by day. The reason for a growing importance of sub-threshold conduction is that the supply voltage has continually scaled down, to reduce average power consumption. The proposed Schmitt Trigger is compared with existing Schmitt Trigger in sub-threshold region. The proposed Schmitt Trigger is an area efficient circuit and found better than the existing Schmitt Trigger circuit in terms of power consumption, delay and power-delay product at various temperatures. Application of ST also demonstrates that Schmitt Trigger based SRAM cell consumes less power as compared to the existing SRAM cell.

Power and delay comparisons reflect that the proposed Schmitt Trigger is better viable option for low power and high performance VLSI designs.

References

[1] N. Lotze and Y. Manoli, "A 62 mV 0.13 µm CMOS standard cell-based design technique using Schmitt-trigger logic," IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 47-60, Jan. 2012.

[2] P. Kolar, E. Karl, U. Bhattacharya, F. Hamzaoglu, H. Nho, Y. G. Ng, Y. Wang, and K. Zheng, "A 32nm high-k metal gate SRAM with adaptive dynamic stability enhancement for low-voltage operation," IEEE J. Solid State Circuits, vol. 46, no. 1, pp. 76-84, Jan. 2011.

[3] J. P. Kulkarni and K. Roy, "Ultralow-voltage process- variation-tolerant Schmitt-trigger-based SRAM design," IEEE Trans. Very Large Scale Integration Syst., vol. 20, no. 2, pp. 319-332, Feb. 2012.

[4] H. Soeleman, K. Roy, and B. Paul, "Robust sub-threshold logic for ultra-low power operation," IEEE Trans. Very Large Scale Integration (VLSI) Syst., vol. 9, no. 1, pp. 90-99, Feb. 2001.

[5] F. Yuan, "Current regenerative schmitt triggers with tunable hysteresis," IEEE 52nd International Midwest Symposium on circuits and systems, pp. 110-113, Aug. 2009.

[6] S. Seo, Y. Jeong, and J. Kenney, "A modified CMOS frequency doubler considering delay time matching condition," Proc. Int 'I Symp. Info. Tech. Converg., pp. 392-395, 2007.

[7] Park, 1. Rhee, and Y. Joo, "Wide dynamic range and high SNR self reset CMOS image sensor using a Schmitt trigger," Proc. IEEE Sensor Conf., pp. 294-296, Oct. 2008.

[8] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV robust Schmitt trigger based subthreshold SRAM," IEEE J. Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[9] S. L. Chen and M. D. Ker, "A new Schmitt trigger circuit in a 0.13 µm 1/2.5-V CMOS process to receive 3.3-V input signals," IEEE Trans. Circuits Syst. II: Express Brief, vol. 52, no. 7, pp. 361-365, Jul. 2005.

About Author (s):

Sapna received the B. Tech. degree in electronics and communication engineering in 2011 and now pursuing her M. Tech. degree in VLSI Design from Mody Institute of Technology and Science, Lakshmangarh, Sikar, India.

B. P. Singh received the B.Sc. degree from Bihar Institute of Technology, Sindri, Dhanbad, India, in 1967 and M.Sc. degree from B.I.T Mesra, Ranchi, India, in 1970. He completed his Ph.D. from Ranchi University, Ranchi, India, in 1980.
Dr. B. P. Singh served B.I.T Mesra, Ranchi from 1970 to 1981, Indian School of Mines, Dhanbad from 1981 to 1987 and Madan Mohan Malaviya Engineering College from 1987 to 2009.
Since 2009 he has been the H.O.D. of E&CE and E&EE, Mody Institute of Technology and Science, Lakshmangarh, Sikar, India. He has over 100 papers to his credits in International and National Journals.