

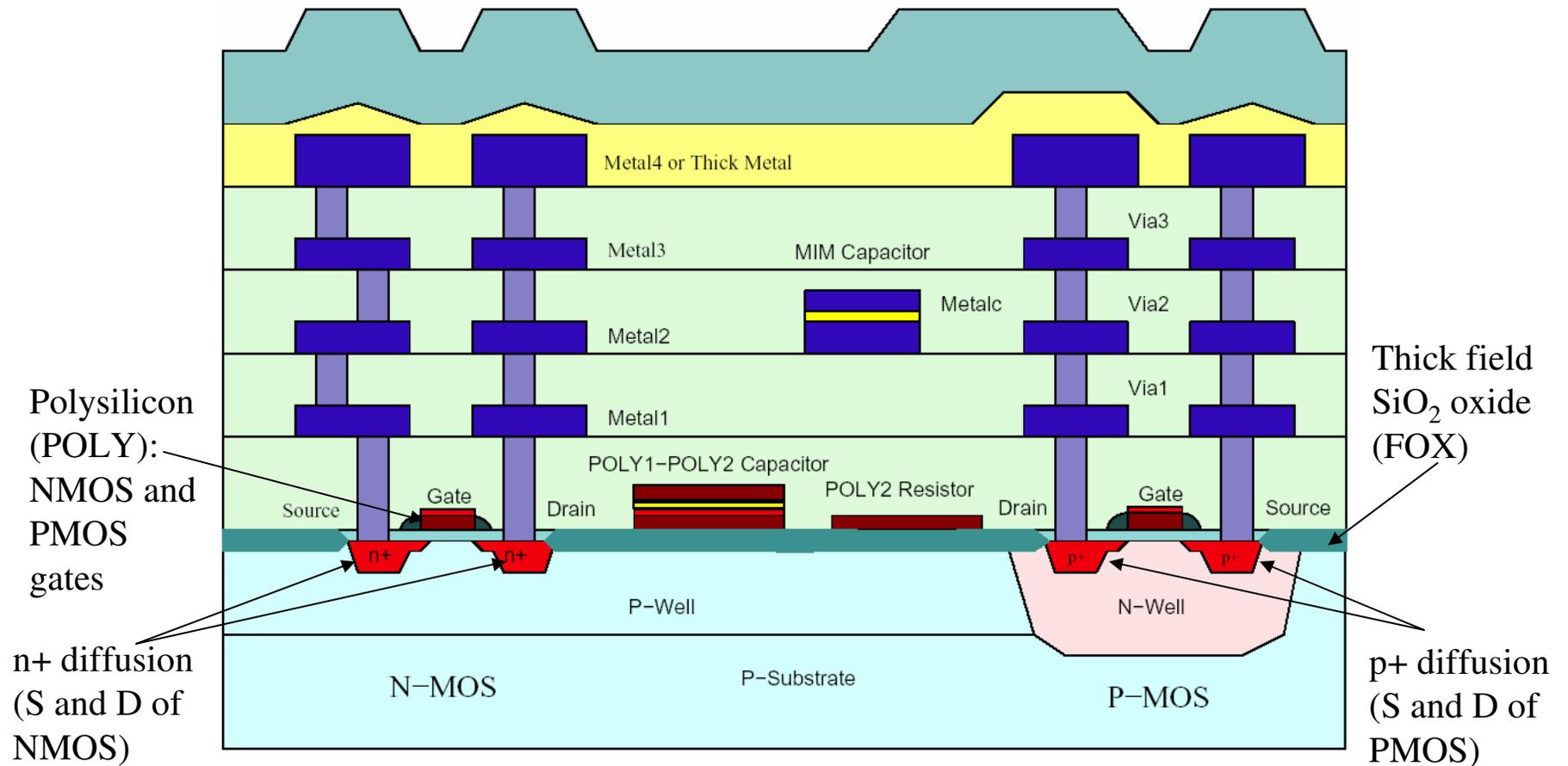
ECEN4827/5827

Process example: 0.35u CMOS  
Spice models

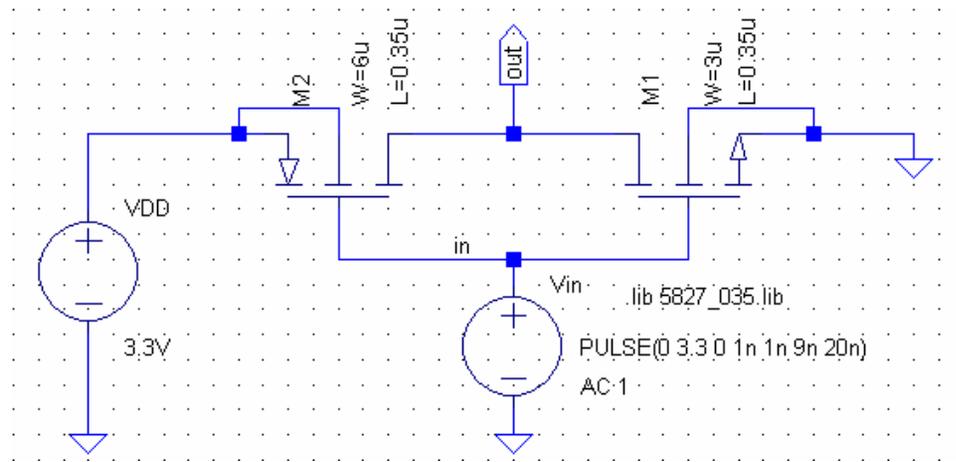
Introduction to schematic capture and Spice simulations  
using LTspice

8/22/2008

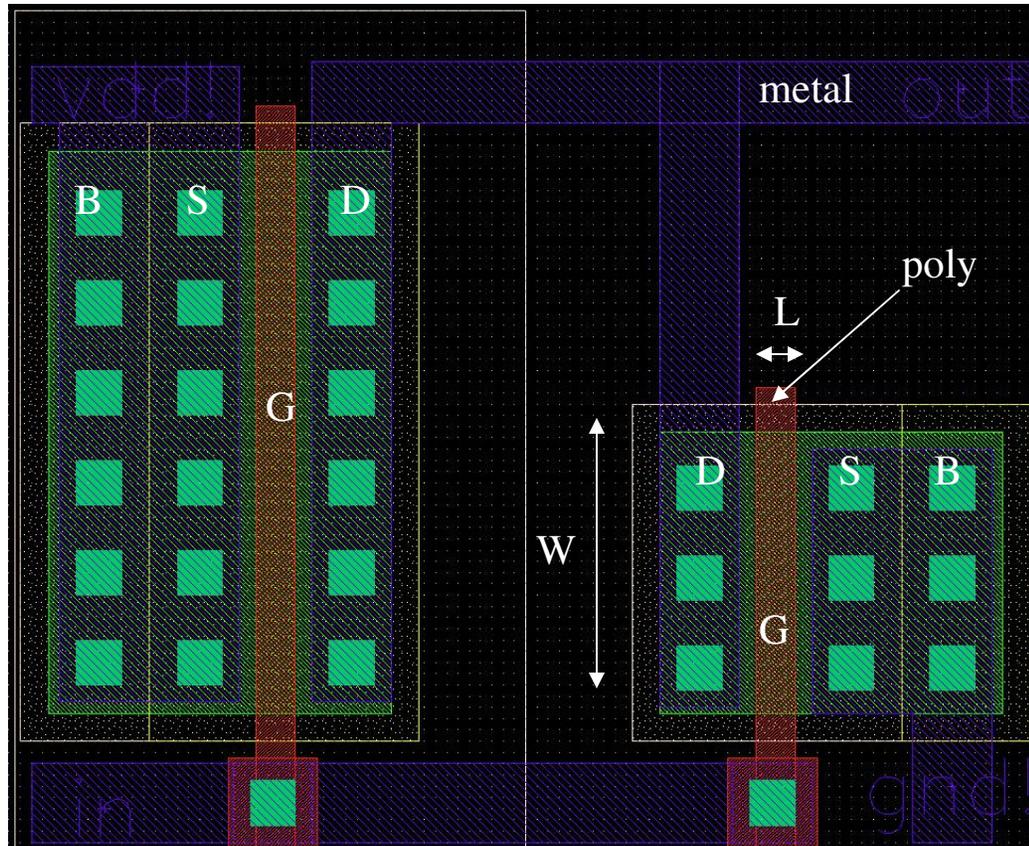
## Typical CMOS process (minimum channel length: $0.35\mu\text{m}$ )



- *p* substrate
- *p* well (body) for NMOS transistors, *n* well (body) for PMOS transistors
- *n*+ and *p*+ source/drain diffusions
- 1 or more polysilicon layers (2 POLY layers in this example)
- 2 or more metal layers (4 metal layers in this example)

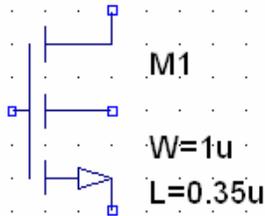


inverter\_intro.asc



# Spice model library: 5827\_035.lib

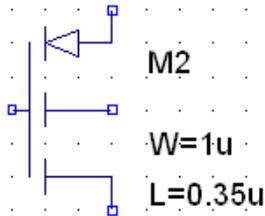
NMOS  
[nmos\\_035.asy](#)



NMOS transistor

B (*p* substrate) must be tied to most negative supply rail

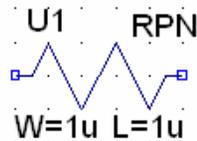
PMOS  
[pmos\\_035.asy](#)



PMOS transistor

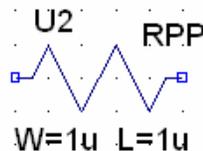
B is *n*-well, usually most positive supply rail

RPN  
[rpn\\_035.asy](#)



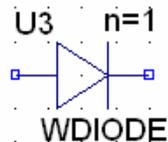
$R_{sheet} = 1.2 \text{ k}\Omega/\text{square}$ ,  $TC = -400 \text{ ppm}/^\circ\text{C}$   
“square” =  $L/W$

RPP  
[rpp\\_035.asy](#)



$R_{sheet} = 50 \text{ }\Omega/\text{square}$ ,  $TC = +830 \text{ ppm}/^\circ\text{C}$   
“square” =  $L/W$

WDIODE  
[wdiode.asy](#)



Unit-area ( $5\mu * 5\mu$ ) *p*+ diffusion to *n*-well diode  
 $n = \text{area multiple}$ . Cathode must be tied to the most negative supply rail

# Example: NMOS model

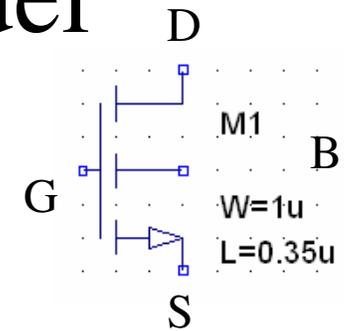
```

-----
*
.subckt NM D G S B
+params: W=10u L=1u
M1 D G S B NM L={L} W={W} AS={2u*W} PS={2*(2u+W)} AD={2u*W} PD={2*(2u+W)}
.ends

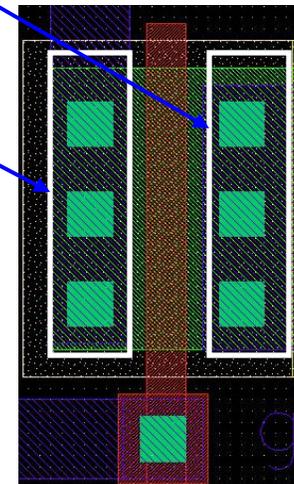
*
* NMOS transistor model
*
.MODEL NM NMOS LEVEL=8
*
***** SIMULATION PARAMETERS *****
*
* format      : LTspice
* model       : MOS BSIM3v3
*
*
* TYPICAL MEAN CONDITION
*
*
* *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00
+NOIMOD =3.000e+00
*
* *** Threshold voltage related model parameters ***
+K1      =5.0296e-01
+K2      =3.3985e-02 K3      =-1.136e+00 K3B     =-4.399e-01
+NCH     =2.611e+17 UTH0    =4.979e-01
+UOFF    =-8.925e-02 DUT0    =5.000e+01 DUT1     =1.039e+00
+DUT2    =-8.375e-03 KETA    =2.032e-02
+PSCRF1  =3.518e+08 PSCRF2  =7.491e-05

```

... more (BSIM3 model is very detailed and complicated)...



nmos\_035.asy



- W, L are circuit design parameters, minimum  $0.35\mu$ , minimum increment  $0.1\mu$
- NMOS Spice model can be used as is a subcircuit, which allows automatic adjustments of AS (source area), PS (source perimeter), DS (drain area) and PD (drain perimeter) as functions of W, or as a native MOS device (user must then manually specify AS, PS, DS, PD)
- Very detailed BSIM3 model (industry standard)

# Setting up 0.35u CMOS symbols and model library for LTspice

- Option 1: local (does not require administrative privileges)
  - Place all symbol files (\*.asy files) and model library (**5827\_035.lib**) in a working folder, together with schematics
- Option 2: make symbols and model library globally available
  - Place all symbols (\*.asy files) in a new folder (e.g. 5827) in **C:\Program Files\LTC\SwCADIII\lib\sym**
  - Add model library **5827\_035.lib** to **C:\Program Files\LTC\SwCADIII\lib\sub**
- In all cases, an LTspice schematic must include:  
**.lib 5827\_035.lib**

# LTspice schematic entry

The image shows a screenshot of the LTspice schematic entry window. The window title is "Linear Technology LTspice/SwitcherCAD III - [inverter\_intro]". The menu bar includes "File", "Edit", "Hierarchy", "View", "Simulate", "Tools", "Window", and "Help". The toolbar contains various icons for file operations, simulation, and editing. Three icons in the toolbar are circled in red: the "Run simulation" icon (a lightning bolt), the "Enter component" icon (a component symbol), and the "Enter Spice commands" icon (a text box).

The schematic diagram shows a CMOS inverter circuit. It consists of a PMOS transistor (M2) and an NMOS transistor (M1) connected in series between a 3.3V DC source (VDD) and ground. The input of the inverter is labeled "in" and is connected to a 1.5V AC source (Vin). The output of the inverter is labeled "out". The PMOS transistor (M2) has a width (W) of 6u and a length (L) of 0.35u. The NMOS transistor (M1) has a width (W) of 3u and a length (L) of 0.35u.

Spice commands are entered in the top-left corner of the schematic area:

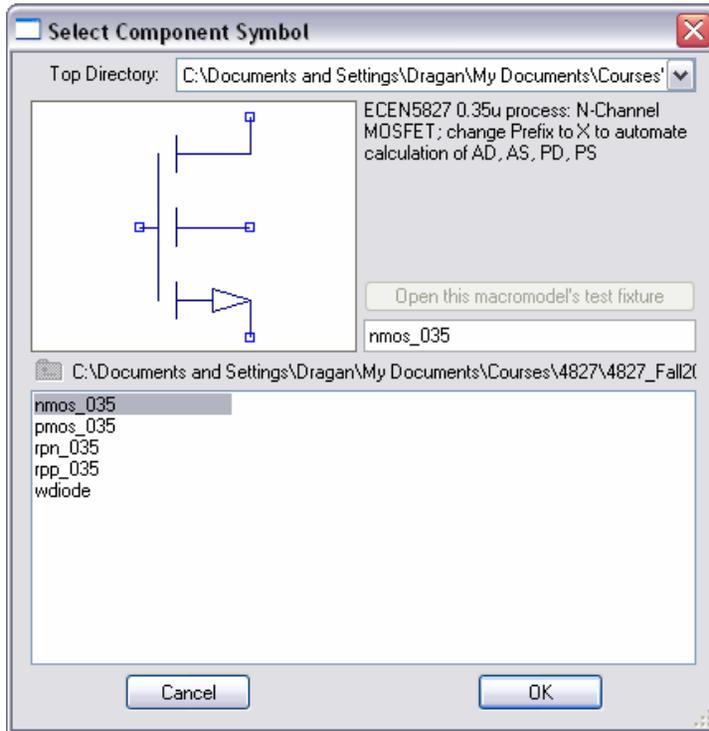
```
;tran 0 100n 0 1n  
.ac dec 101 1k 1g  
;dc Vin 0 3.3 0.01
```

Annotations in red text provide instructions:

- "Run simulation" points to the lightning bolt icon in the toolbar.
- "Enter component" points to the component symbol icon in the toolbar.
- "Enter Spice 'dot' commands" points to the text box icon in the toolbar.
- "include 5807\_035.lib library" points to the ".lib 5827\_035.lib" command in the schematic area.

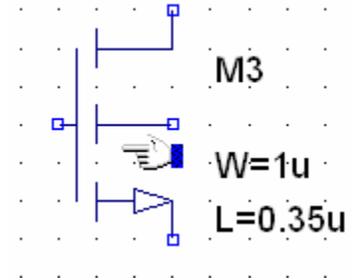
# Use of NMOS symbol in LTspice

(1) place **nmos\_035** symbol

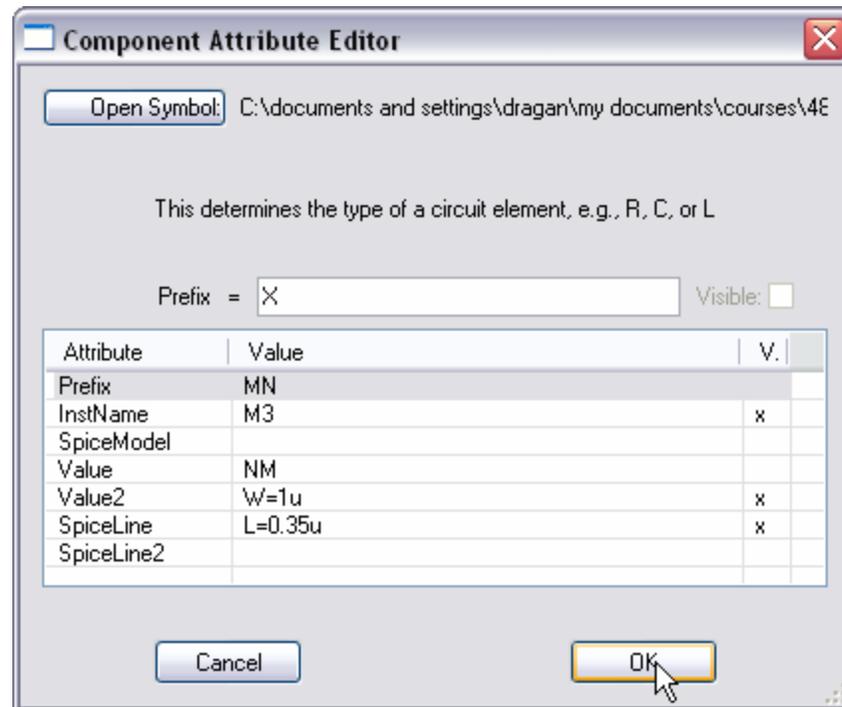


The same applies to **pmos\_035**

(2) **CTRL-right click** to open Attribute Editor



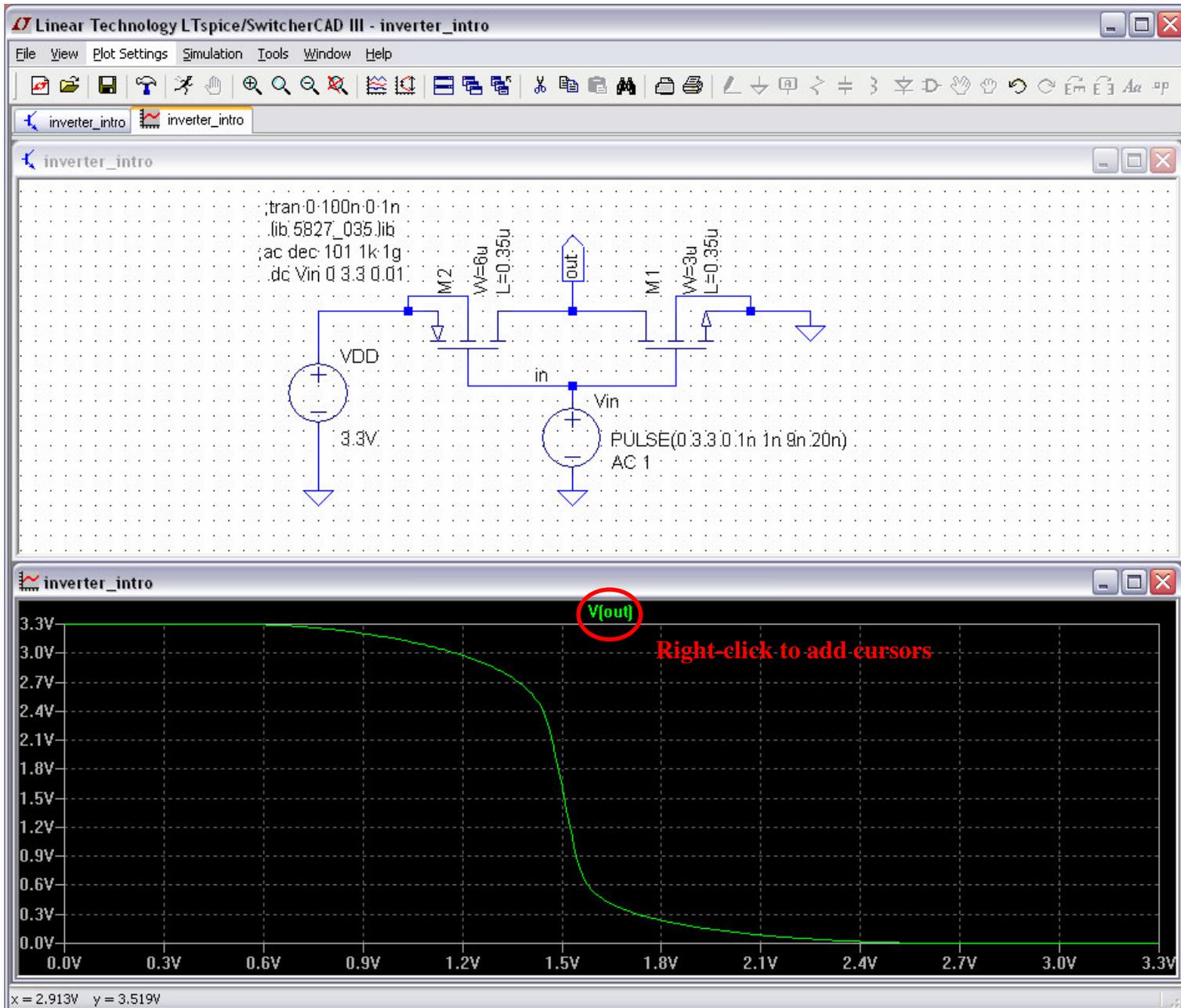
(3) Change **Prefix to X** to use subcircuit model with automatic adjustments of AS, PS, AD, PD



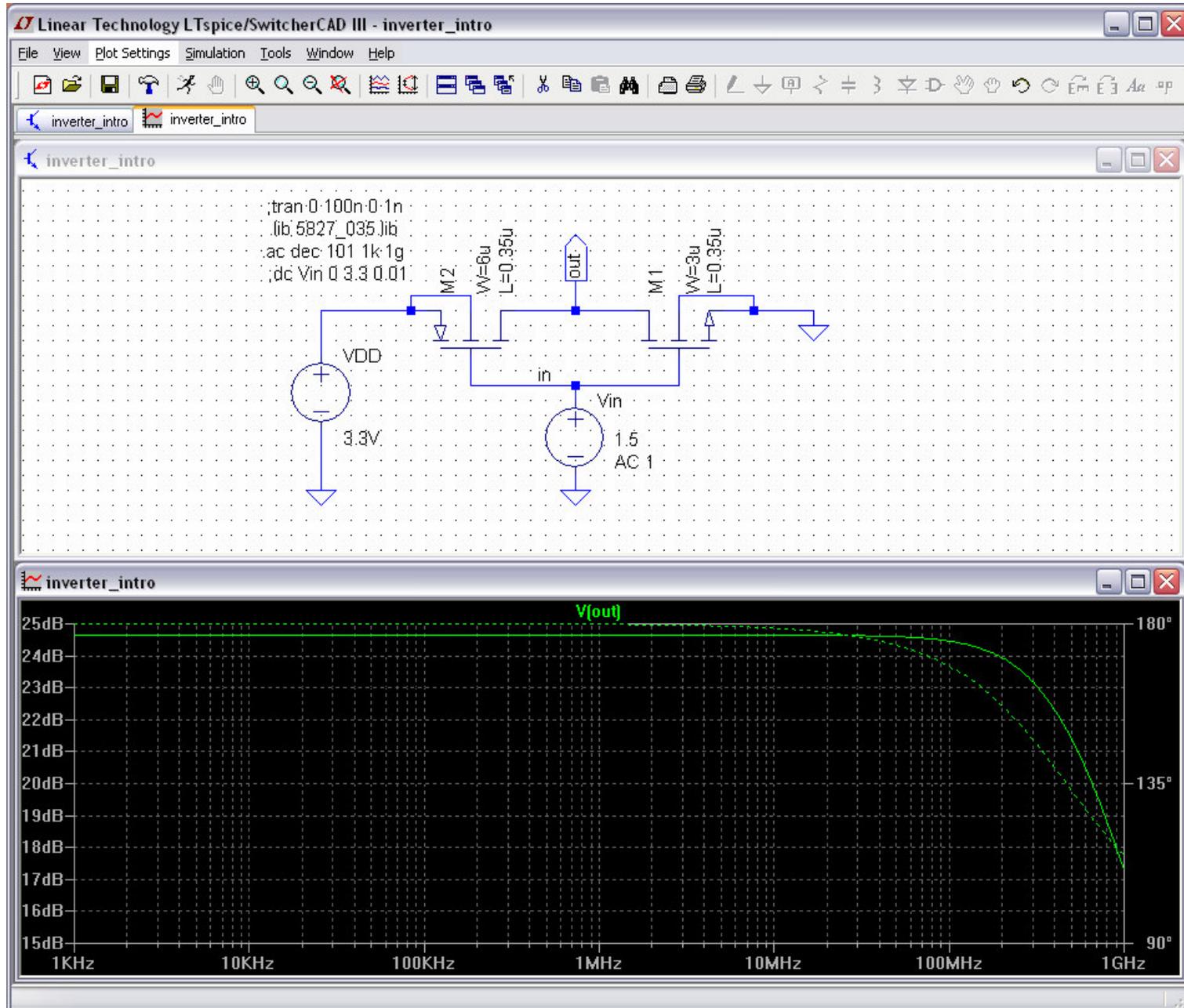
# Basic Spice simulations

- Bias Point (.op)
  - View DC operating point voltages and currents, and device small-signal model parameters in (text)
- DC Sweep (.dc)
  - Plot DC (or temperature) characteristics
- AC Sweep (.ac)
  - Plot small-signal frequency responses
- Transient (.tran)
  - Plot large-signal (total) waveforms

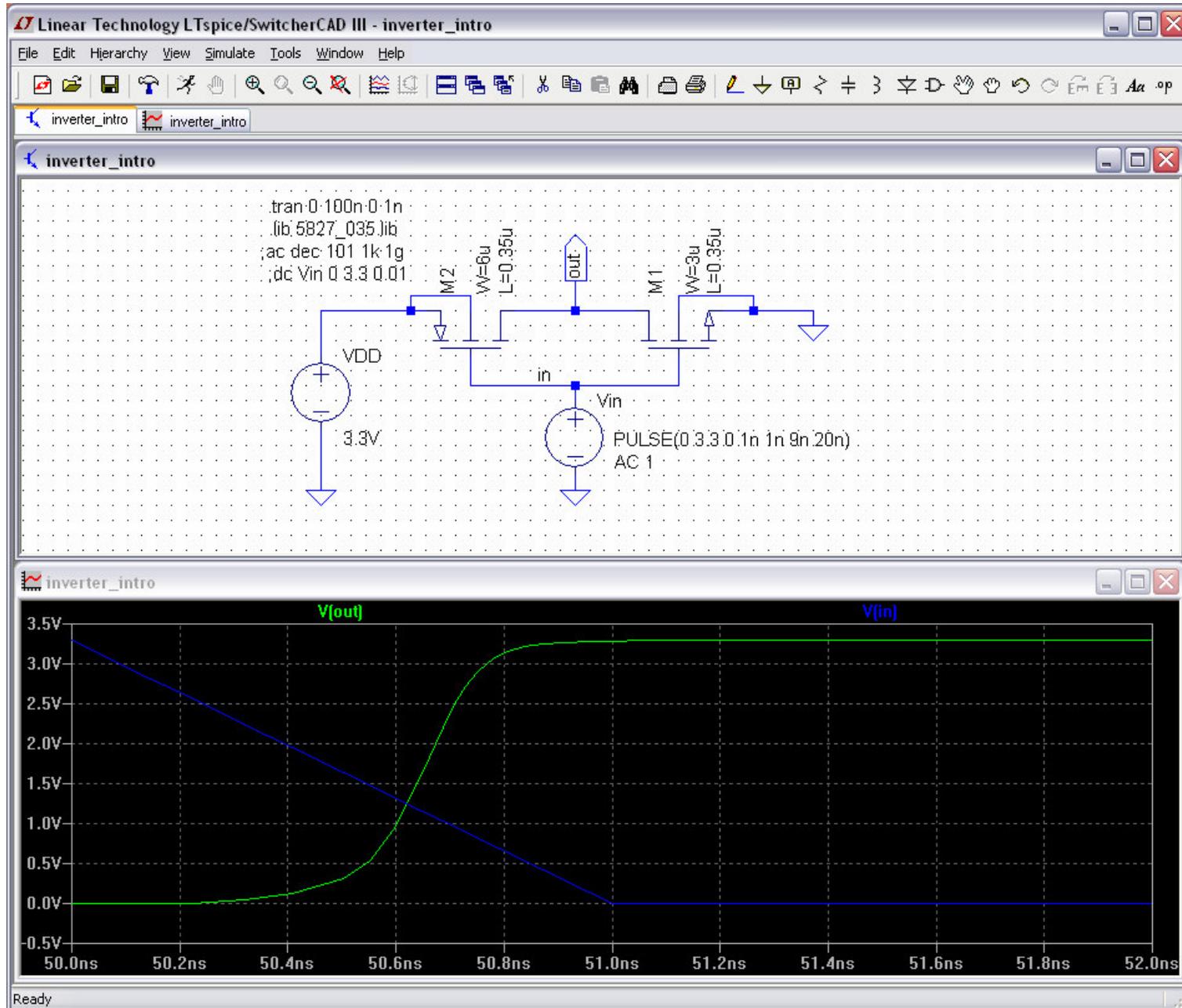
# DC sweep example: inverter $V_{OUT}$ versus $V_{IN}$



AC sweep example: inverter as an amplifier, magnitude response  $\|v_{out}/v_{in}\|$  [dB]

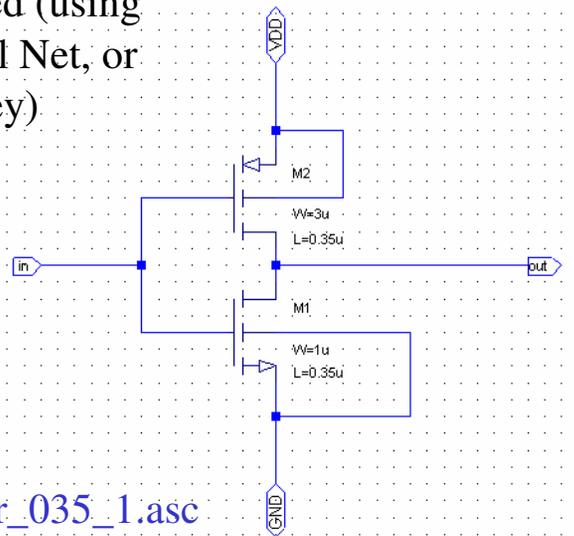


# Transient example: inverter $v_{OUT}(t)$ for pulsating $v_{IN}(t)$



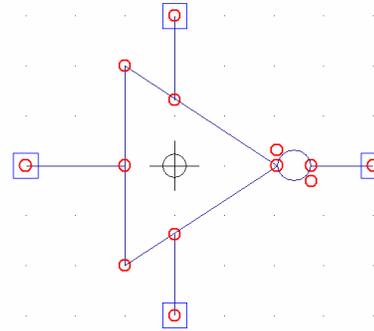
# Hierarchical schematic entry

Inverter circuit with ports labeled (using Edit, Label Net, or F4 key)



inverter\_035\_1.asc

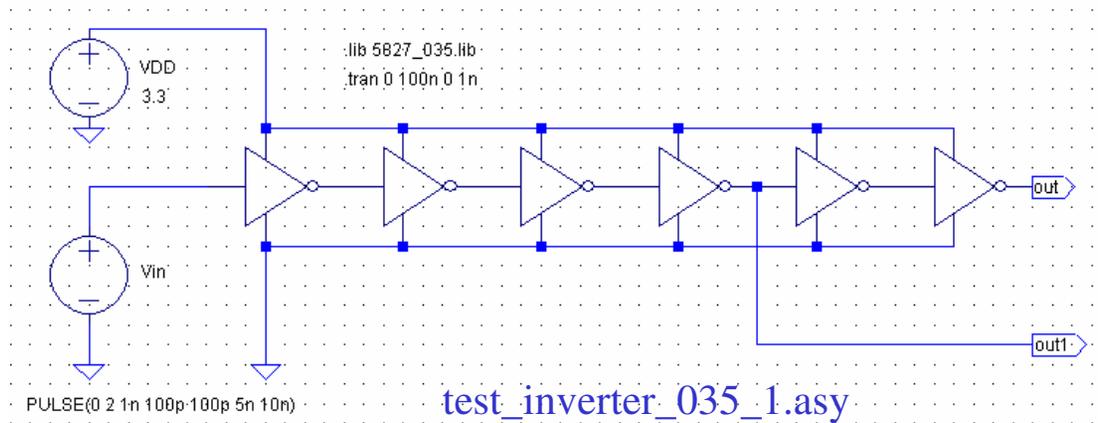
Symbol representing the inverter circuit



inverter\_035\_1.asy

names must match

Symbols used to enter larger circuits



test\_inverter\_035\_1.asy