Semiconductor Devices

THIRD EDITION

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Chapter 7
MESFET and Related Devices

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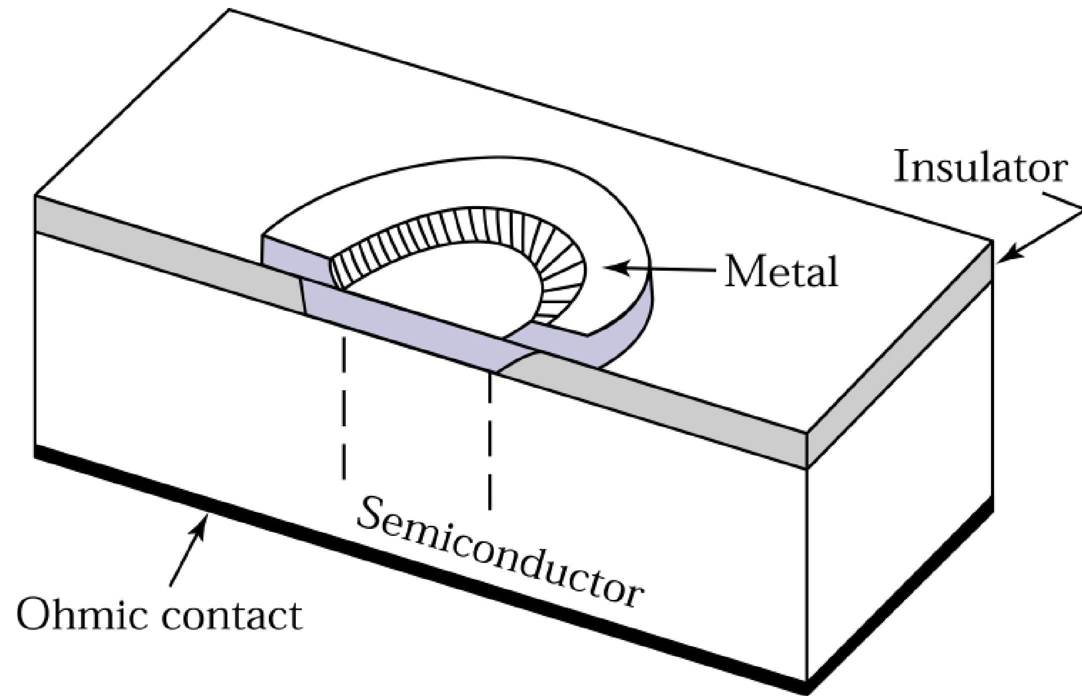
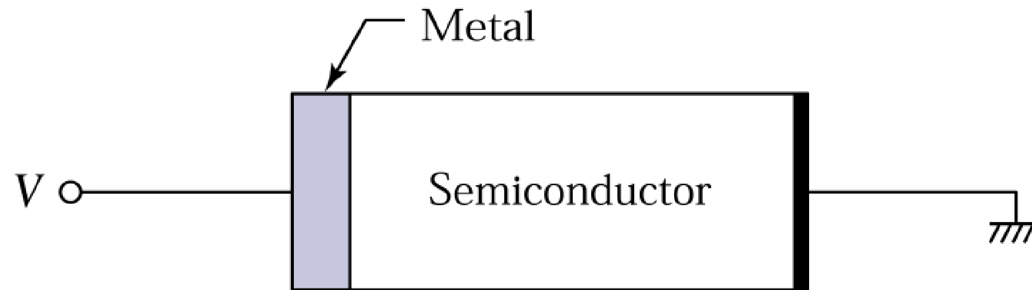
Figure 7.1.
(*a*) Perspective view of a metal-semiconductor contact fabricated by the planar process. (*b*) One-dimensional structure of a metal-semiconductor contact.



Shottky diode

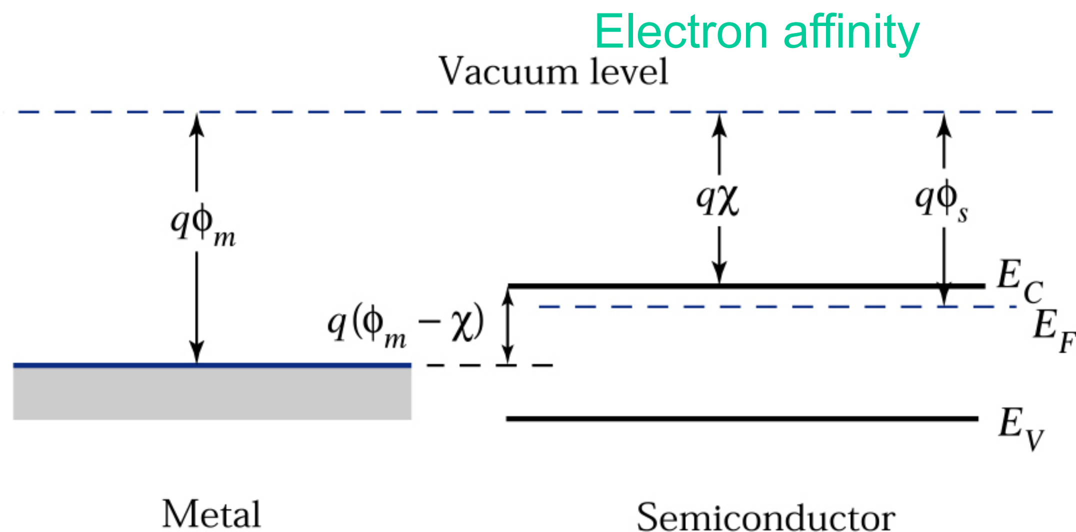
Ohmic contact



Work function Φ=vacu.- E_F

Figure 7.2. (*a*) Energy band diagram of an isolated metal adjacent to an isolated *n*-type semiconductor under thermal nonequilibrium condition. (*b*) Energy band diagram of a metal-semiconductor contact in **thermal equilibrium.**

(Ef 相等, Vacu. 連續)



e的barrier $q\Phi_{Bn} = q(\Phi_m - X)$ (1)

h的barrier $q\Phi_{Bp} = E_g - q(\Phi_m - X)$ (2)

$q(\Phi_{Bn} + \Phi_{Bp}) = E_g$ (3)

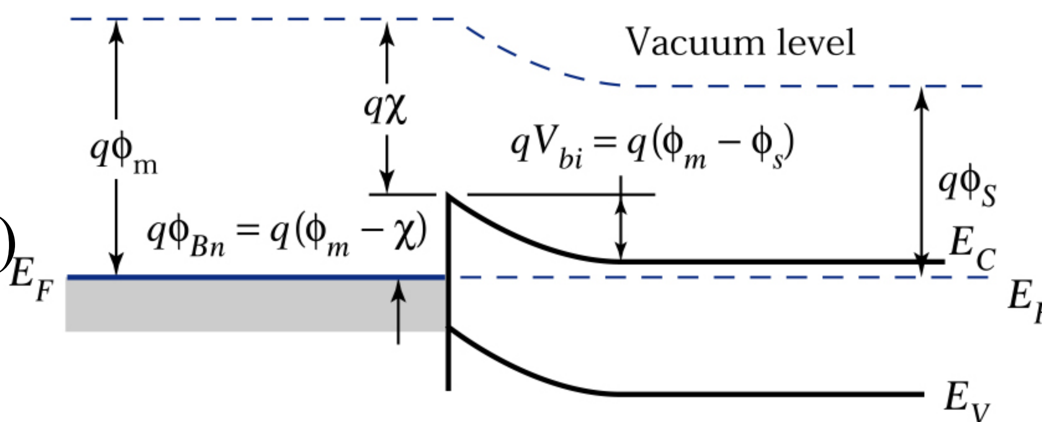
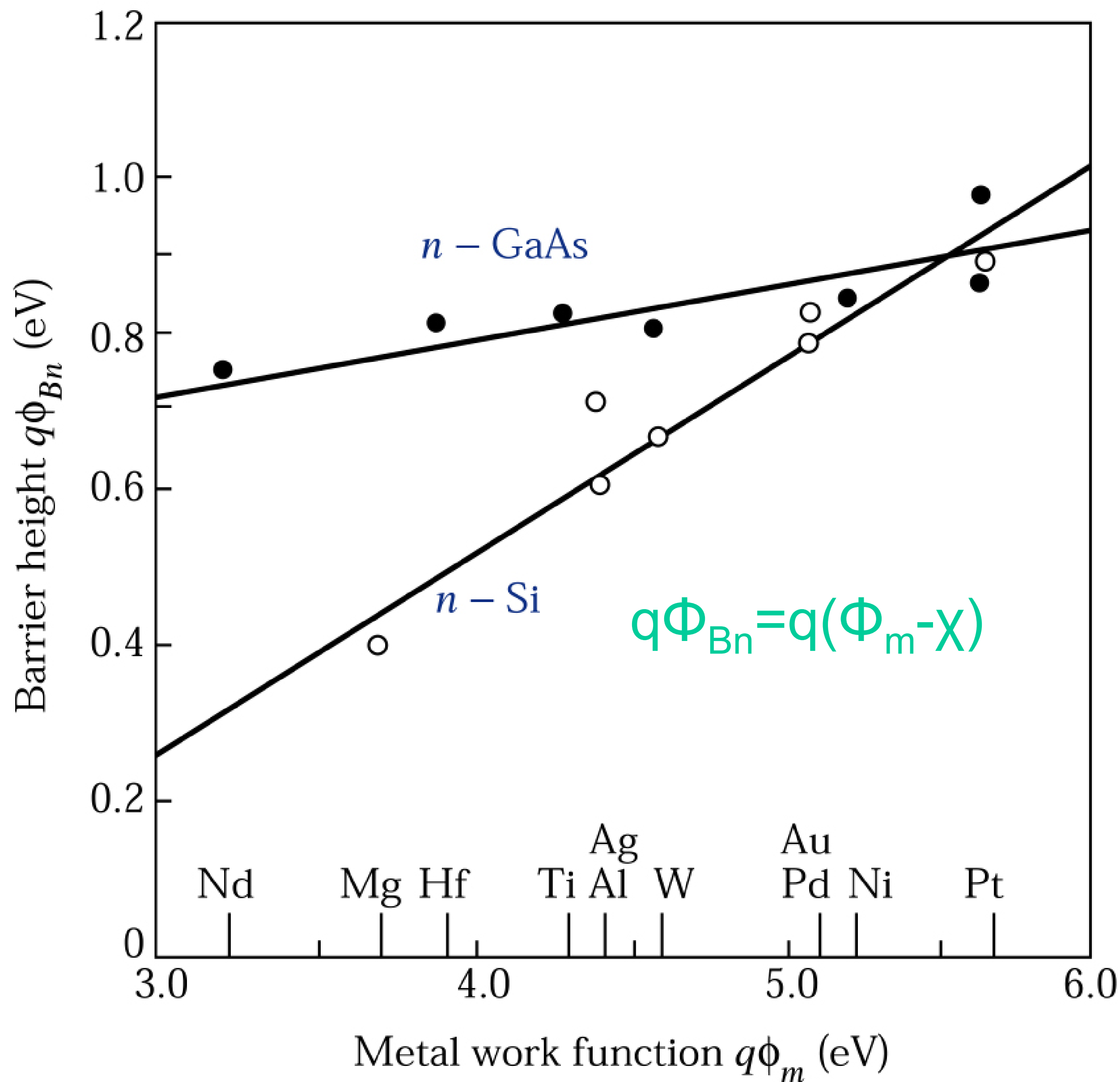


Figure 7.3.
Measured barrier height for metal-silicon and metal-gallium arsenide contacts. [2,3]

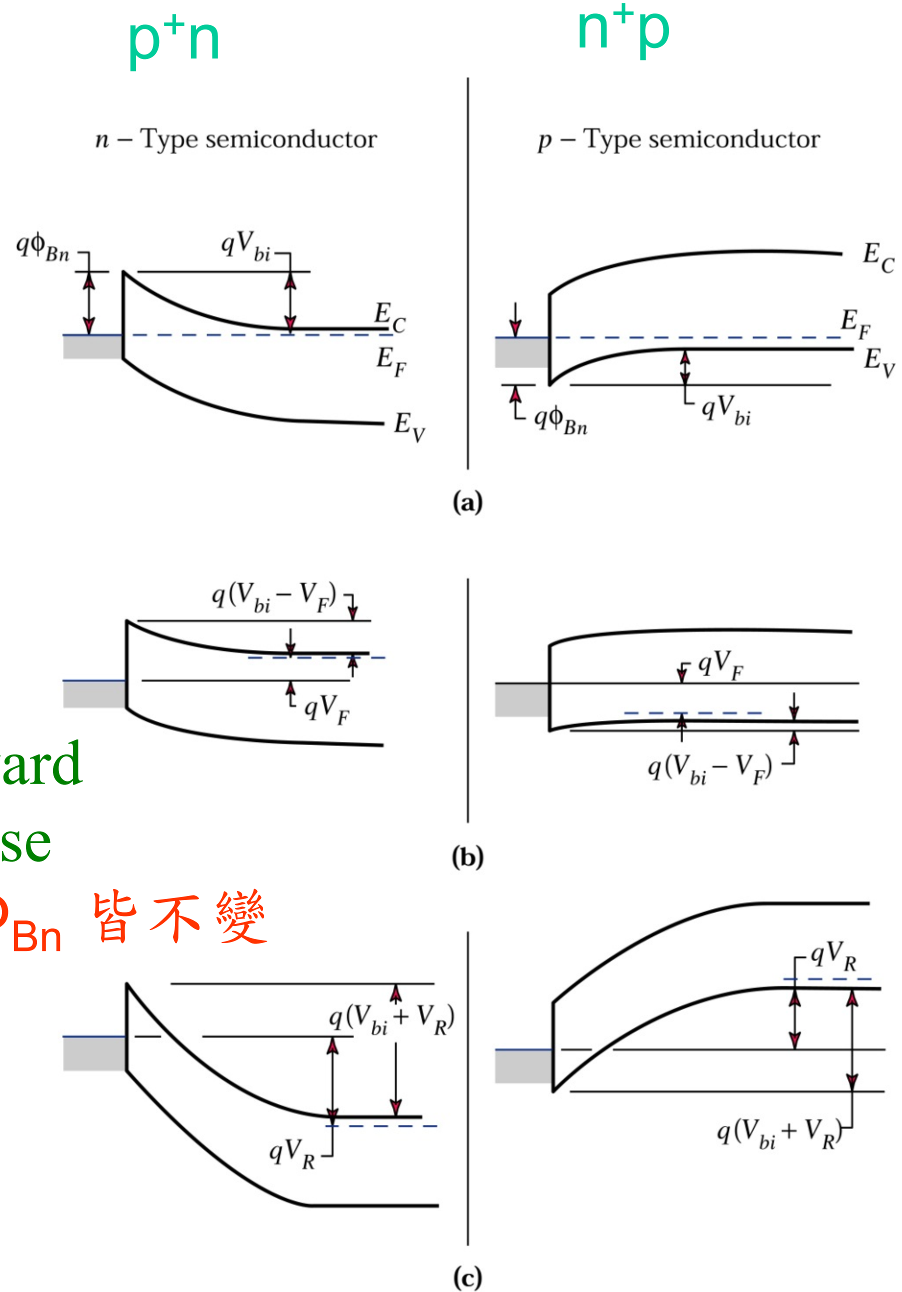


$V_{bi}=\Phi_{Bn}-V_n$

由V_{bi}得知，
可求Φ_{Bn}

$V_n=E_c-E_F$

Figure 7.4.
Energy band diagrams of metal *n*-type and *p*-type semiconductors under different biasing conditions: (*a*) thermal equilibrium; (*b*) forward bias; and (*c*) reverse bias.



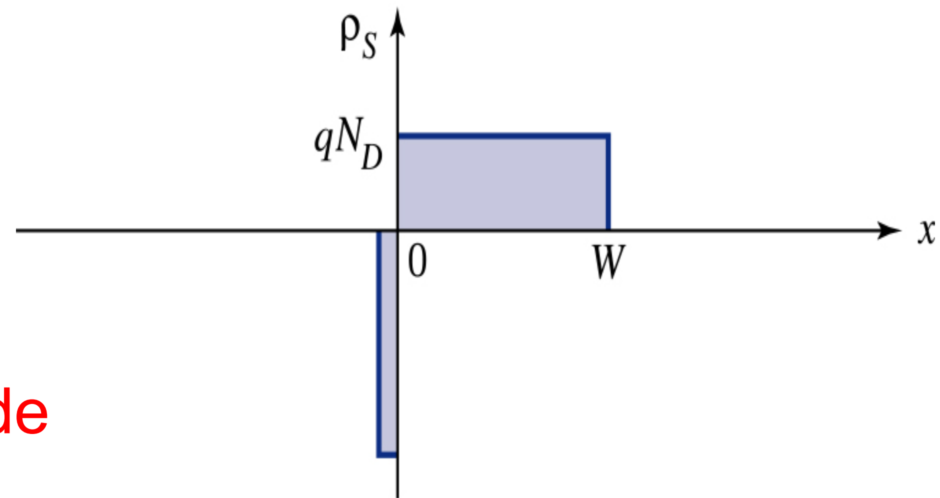
p+/n公式

$$\left|E(x)\right| = \frac{qN_D}{\varepsilon_{ss}}(W - x) = E_m - \frac{qN_D}{\varepsilon_{ss}}x \quad (6)$$

V為+,forward
-,reverse

Φ_{Bn} 皆不變

$$W = \sqrt{\frac{2\varepsilon_{ss}}{qN_D}(V_{bi} - V)} \quad (8)$$



如同p⁺n diode

Surface states 影響ΦB

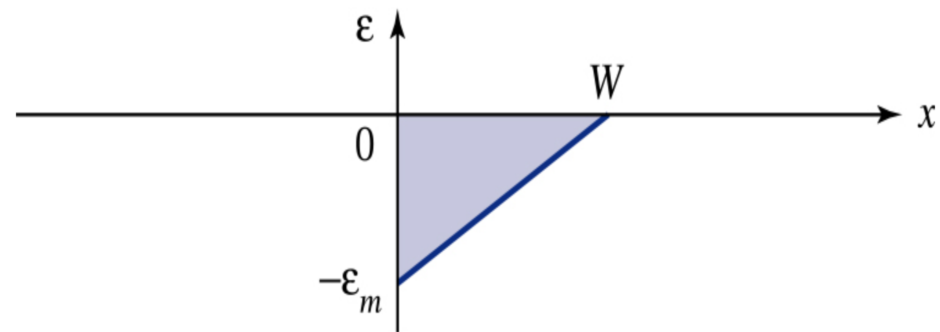


Figure 7.5. (*a*) Charge distribution and (*b*) electric-field distribution in a metal-semiconductor contact.

Figure 7.6.
$1/C^2$ versus applied voltage for W-Si and W-GaAs diodes.[4]

空間電荷

$$Q_{sc} = qN_D W = \sqrt{2q\varepsilon_s N_D (V_{bi} - V)} \quad (9)$$

$$C = \left|\frac{\partial Q_{sc}}{\partial V}\right| = \sqrt{\frac{Q\varepsilon_S N_D}{2(V_{bi} - V)}} = \frac{\varepsilon_s}{W} \quad (10)$$

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\varepsilon_s N_D} \quad (11a)$$

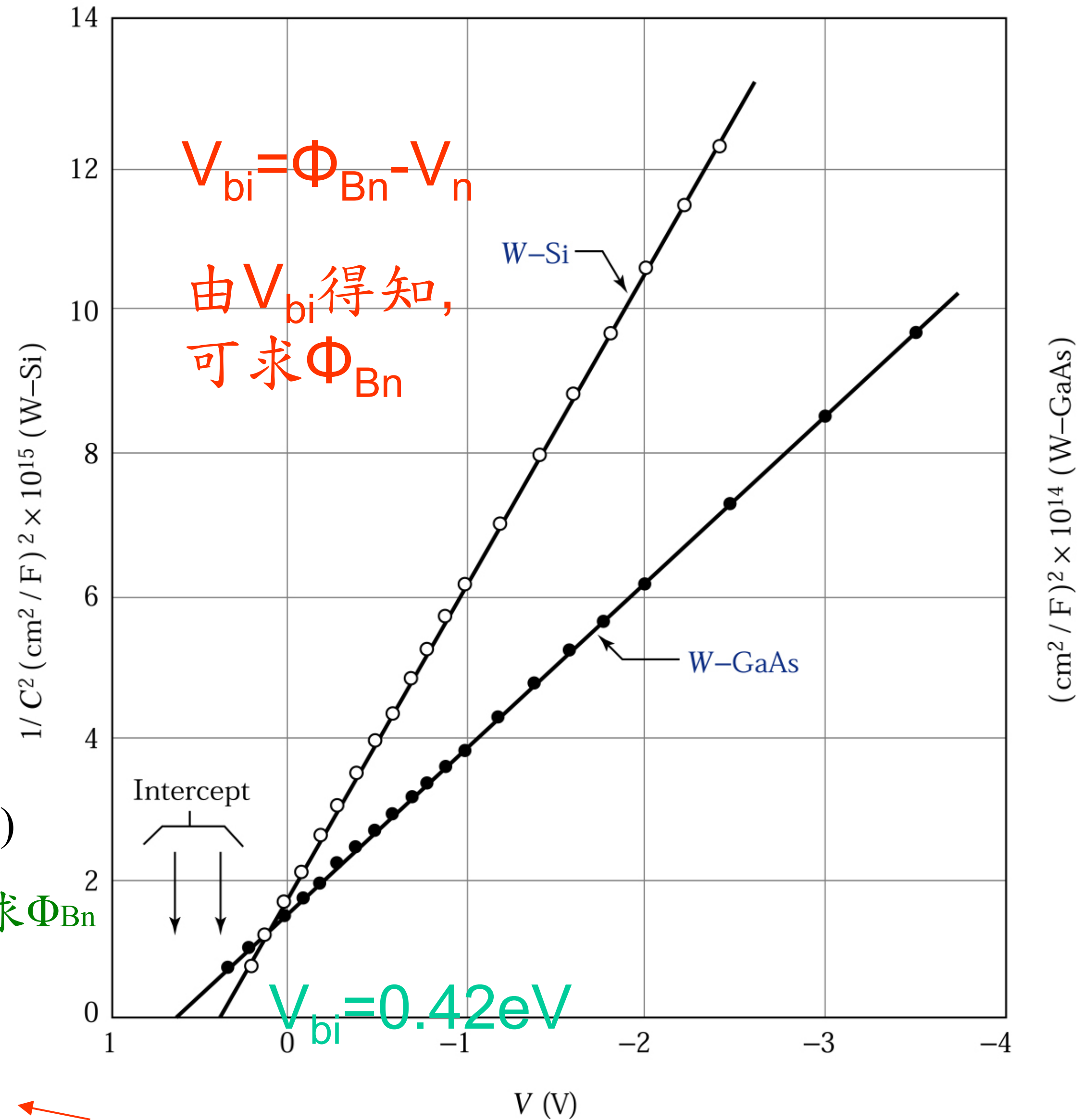
可求Vbi

$$\frac{-d(1/C^2)}{dV} = \frac{2}{q\varepsilon_S N_D}$$

$$N_D = \frac{2}{q\varepsilon_S}\left[\frac{-1}{d(1/C^2)/dV}\right] \quad (12)$$

$$\Phi_{Bn} = V_{bi} + V_n$$

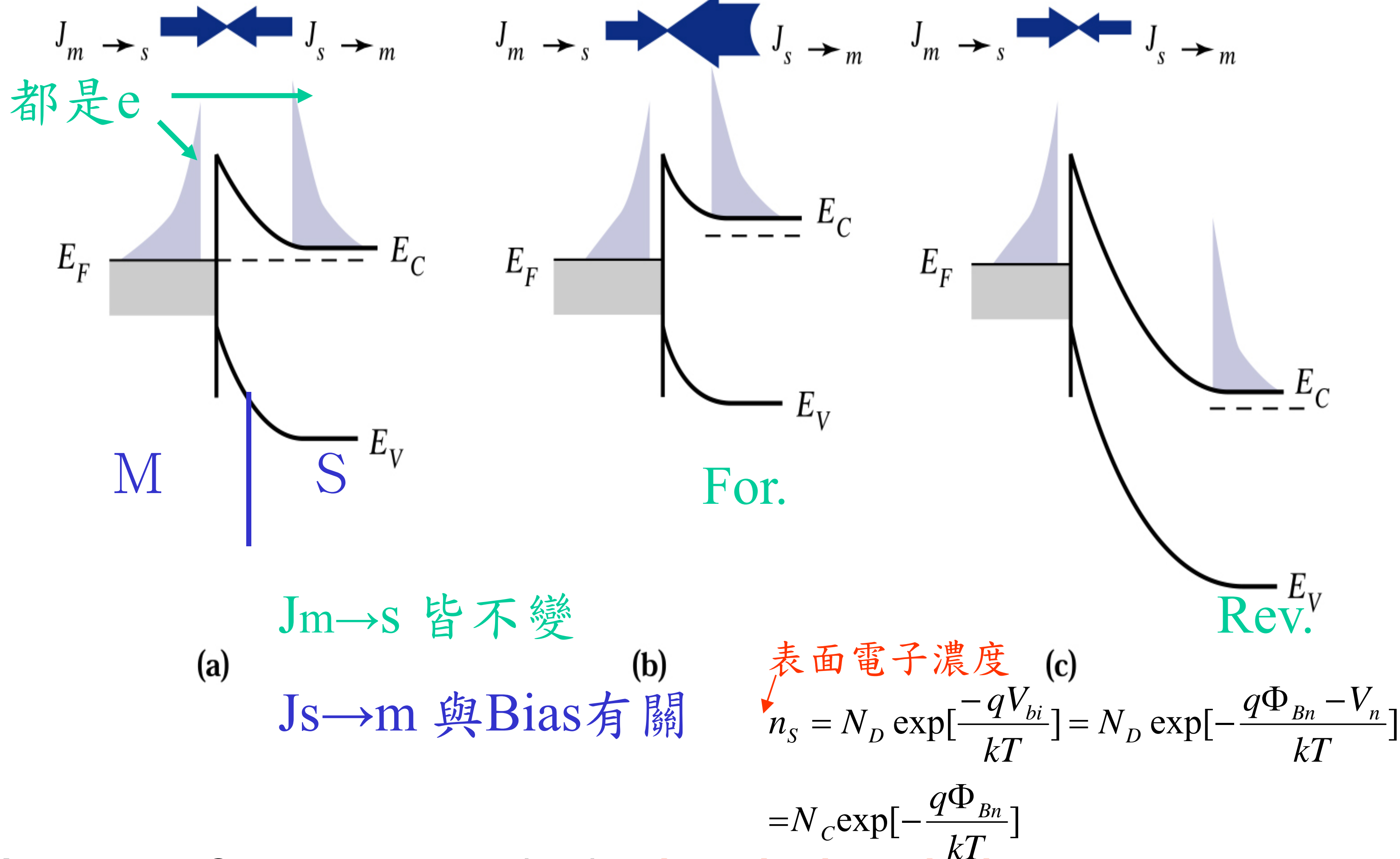
可知



可求doping profile

7.1.2 Current-Voltage Characteristics　型如diode

電流大小正比邊界電子濃度



$$n_S = N_D \exp[\frac{-qV_{bi}}{kT}] = N_D \exp[-\frac{q\Phi_{Bn} - V_n}{kT}]$$

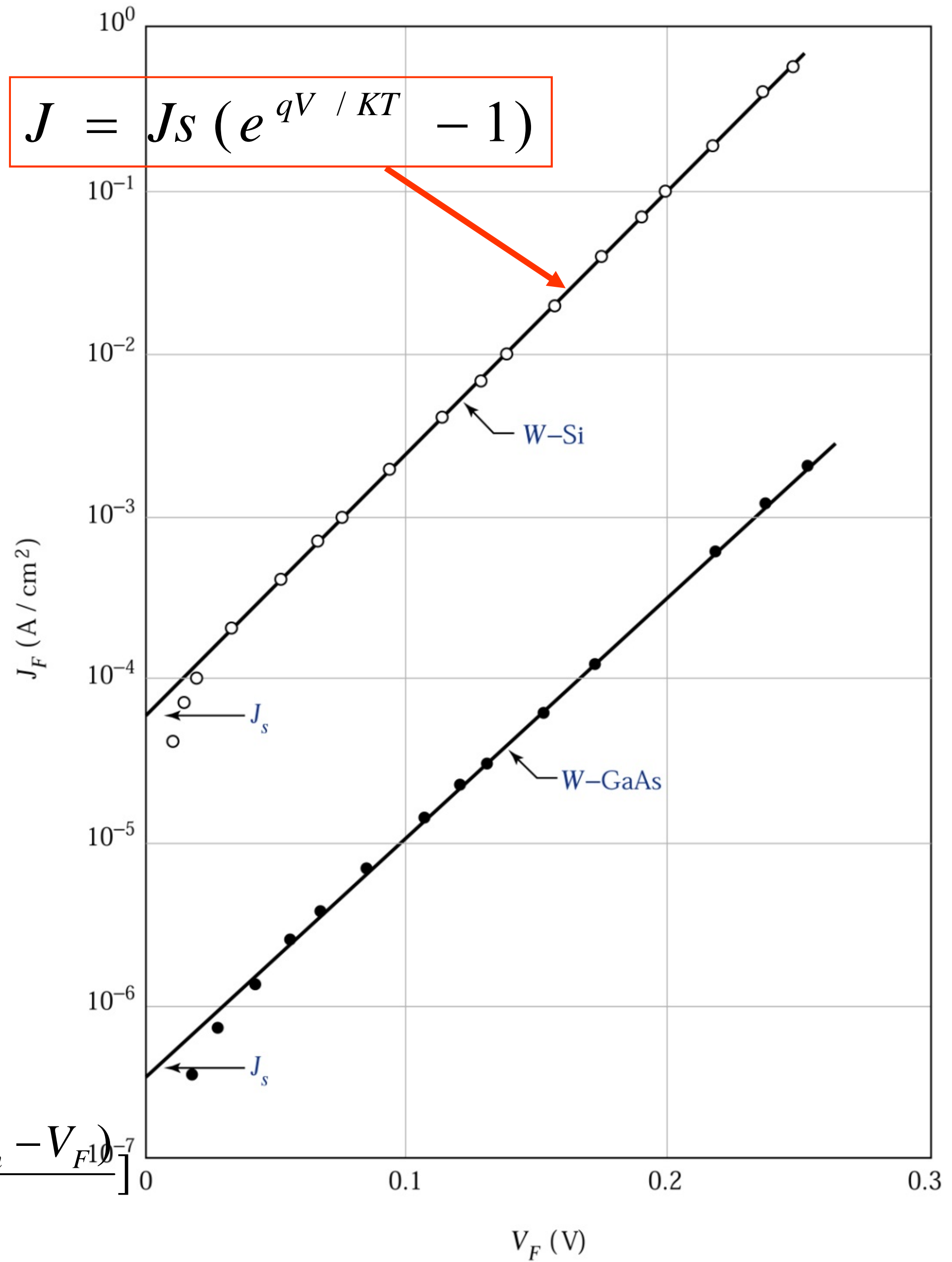
$$= N_C \exp[-\frac{q\Phi_{Bn}}{kT}]$$

Figure 7.7. Current transport by the **thermionic emission process**. (*a*) Thermal equilibrium; (*b*) forward bias; and (*c*) reverse bias.[5]

Figure 7.8. Forward current density versus applied voltage of W-Si and W-GaAs diodes.[4]

$$|J_{m\to s}| = |J_{s\to m}| \propto n_s \qquad (14)$$

$$|J_{m\to s}| = |J_{s\to m}| = C_1 N_C \exp[-\frac{q\Phi_{Bn}}{kT}] \qquad (14a)$$



$$n_S \cong N_D \exp[-\frac{q(V_{bi} - V_F)}{kT}] = N_D \exp[-\frac{q(\Phi_{Bn} - V_n - V_F)}{kT}]$$

$$= N_C \exp[-\frac{q(\Phi_{Bn} - V_F)}{kT}]$$

$$J = J_{s\to m} - J_{m\to s}$$

$$= C_1 N_C \exp[-\frac{q(\Phi_{Bn} - V_F)}{kT}] - C_1 N_C \exp[-\frac{q\Phi_{Bn}}{kT}] \quad (16)$$

$$= C_1 N_C^{-q\Phi_{Bn}/kT}(e^{qV_F/kT} - 1)$$

$$J = J_S(e^{qV/kT} - 1) \quad (17)$$

V+, for.
V- ,rev.

$$J_S \equiv A^* T^2 e^{-q\Phi_{Bn}/kT} \quad (17a)$$

$$J_P = J_{po}(e^{qV/kT} - 1) \quad (18)$$

很小

minority (→ P)

metal 之hole inj.到 Si, E向metal.

$$J_{po} \equiv \frac{qD_P n_i^2}{L_p N_D} \quad (18a)$$

Shottky diode 為 unipolar!

§ohmic Contact

Specific contact resistance

$$R_C = [\frac{\partial J}{\partial V}]^{-1}_{V=0} \qquad \Omega - cm^2 \qquad (19)$$

注意單位

$R_C \downarrow \rho_c$

$$Rc = \frac{\rho_c}{A}$$

只與材質有關!

VLSI → A↓ → R↑

只要A↑ → R → 0

由前可知

$$R_C = \frac{k}{qA^*T}\exp[\frac{q\Phi_{Bn}}{kT}] \qquad (20)$$

thermionic

$$I \sim \exp[-2W\sqrt{2m_n(q\Phi_{Bn}-qV)/h^2}] \qquad (21)$$

若ND很大,W下降,則tunneling為主

W代入,可得 →

$$I \sim \exp[\frac{-C_2(\Phi_{Bn}-V)}{\sqrt{N_D}}] \qquad (22)$$

High ND之Rc, tunneling為主

$$R_C \sim \exp[\frac{C_2\Phi_{Bn}}{\sqrt{N_D}}] \qquad (23)$$

ND≧1E19,tunneling為主

ND≦1E17,thermoionic為主

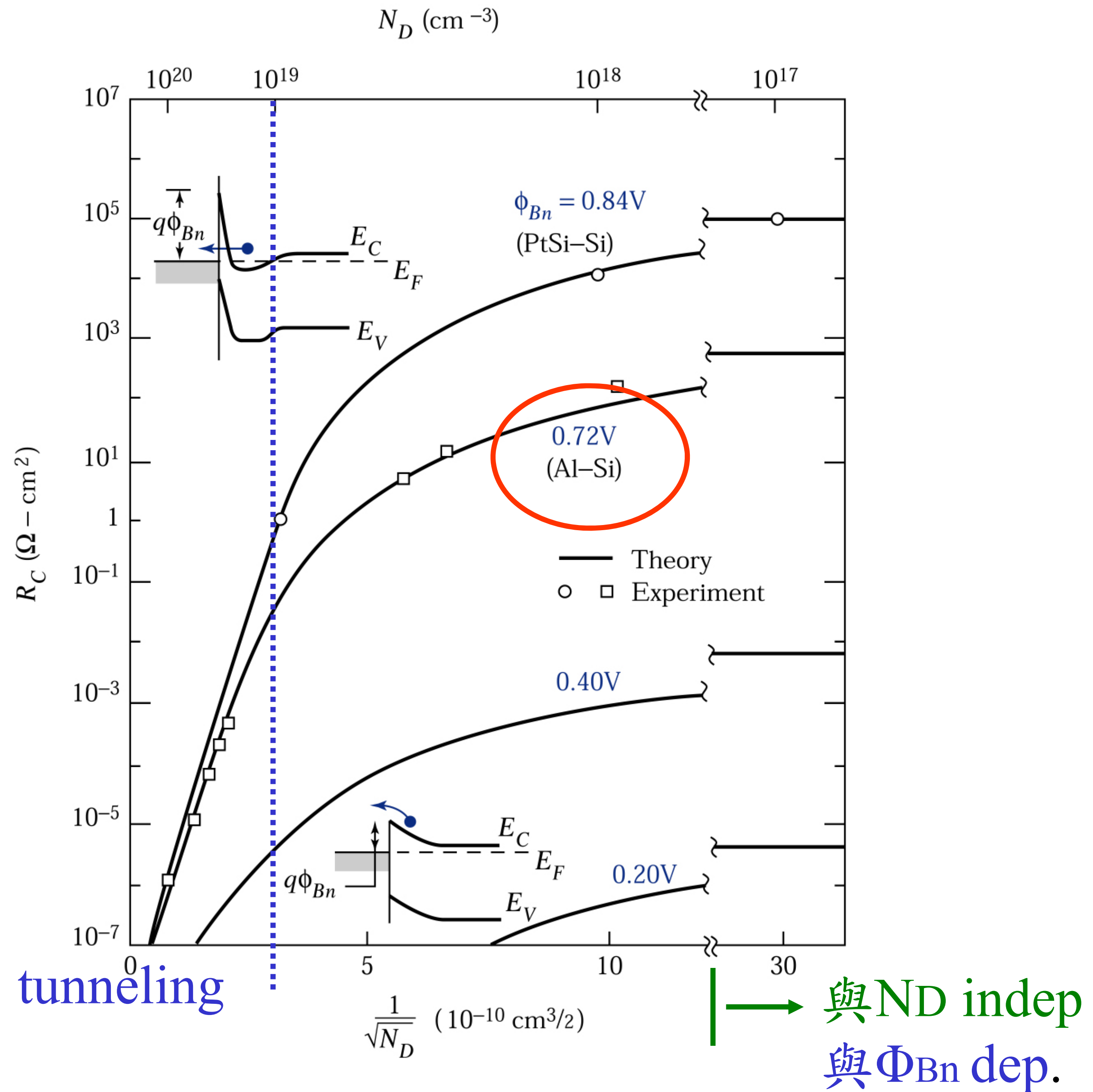


Figure 7.9. Calculated and measured values of specific contact resistance. Upper inset shows the tunneling process. Lower inset shows thermionic emission over the low barrier.[6]

欲得小 Rc

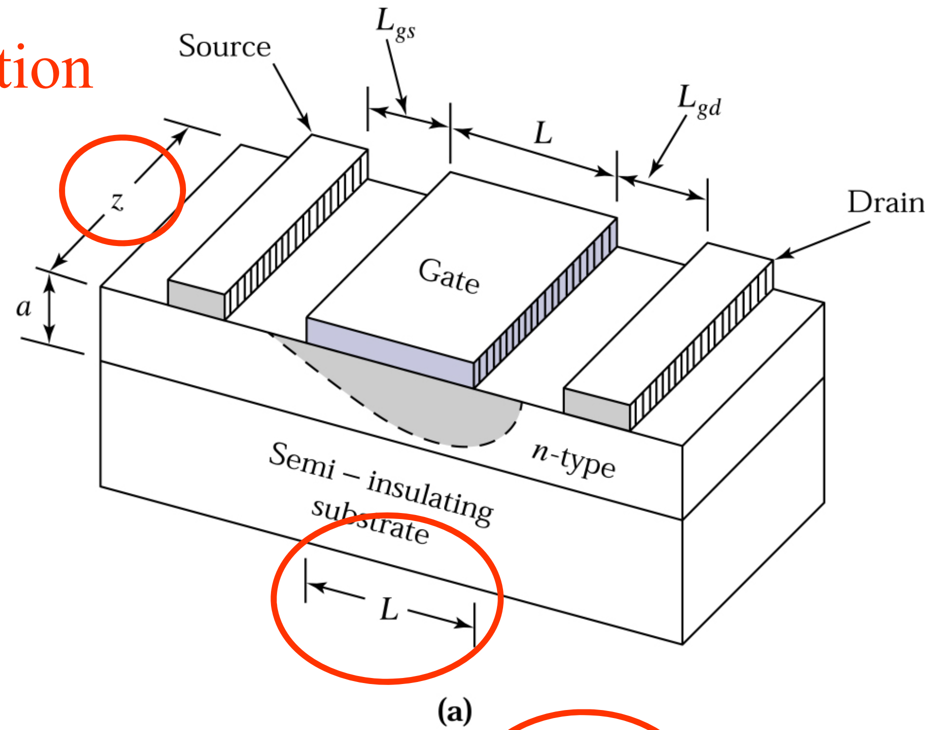
ΦBn ↓

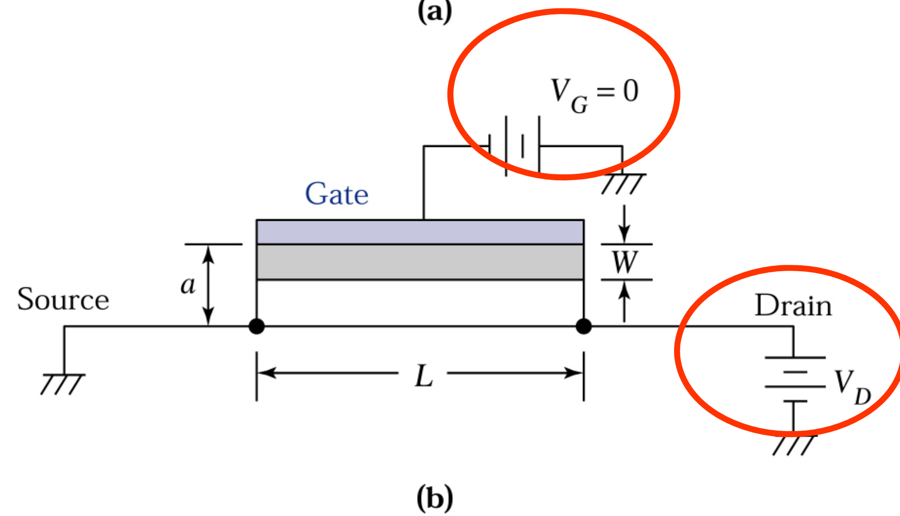
ND ↑

Metal-Semiconductor junction

Figure 7.10.
(*a*) Perspective view of a metal-semiconductor field-effect transistor (MESFET). (*b*) Cross section of the gate region of a MESFET.

n-channel
(比p-channel 之 u 高)





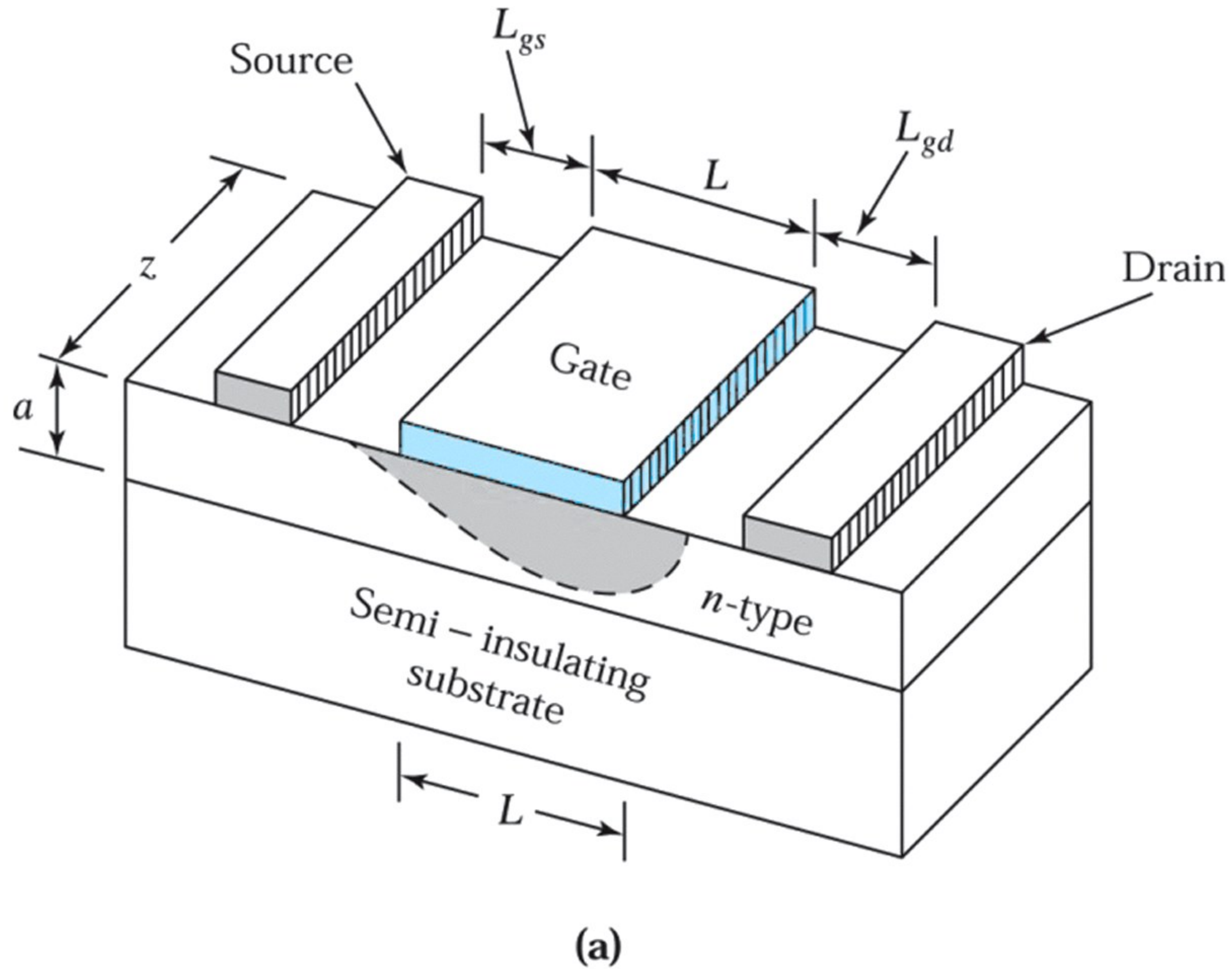


Figure 7.10a

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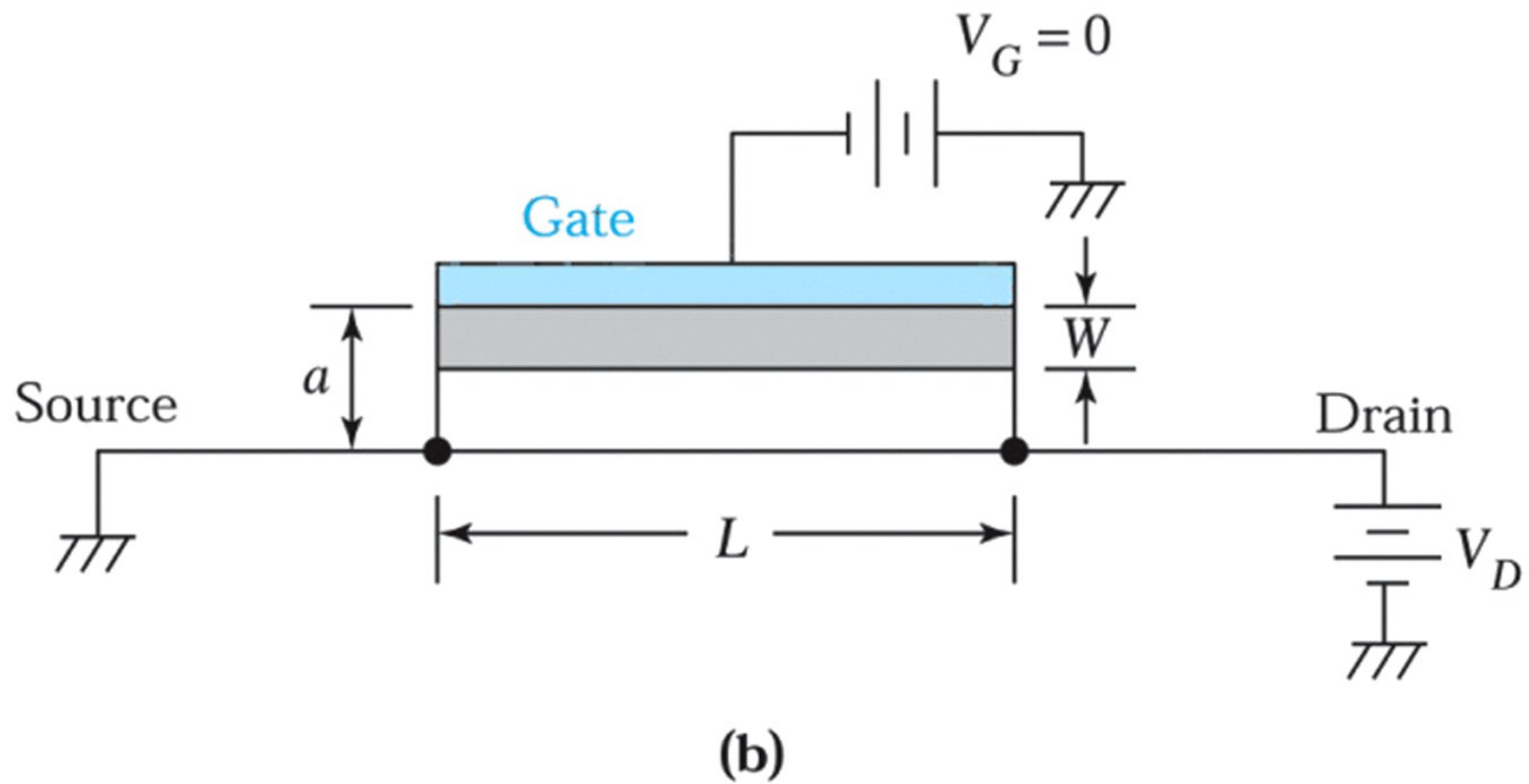

Figure 7.10b
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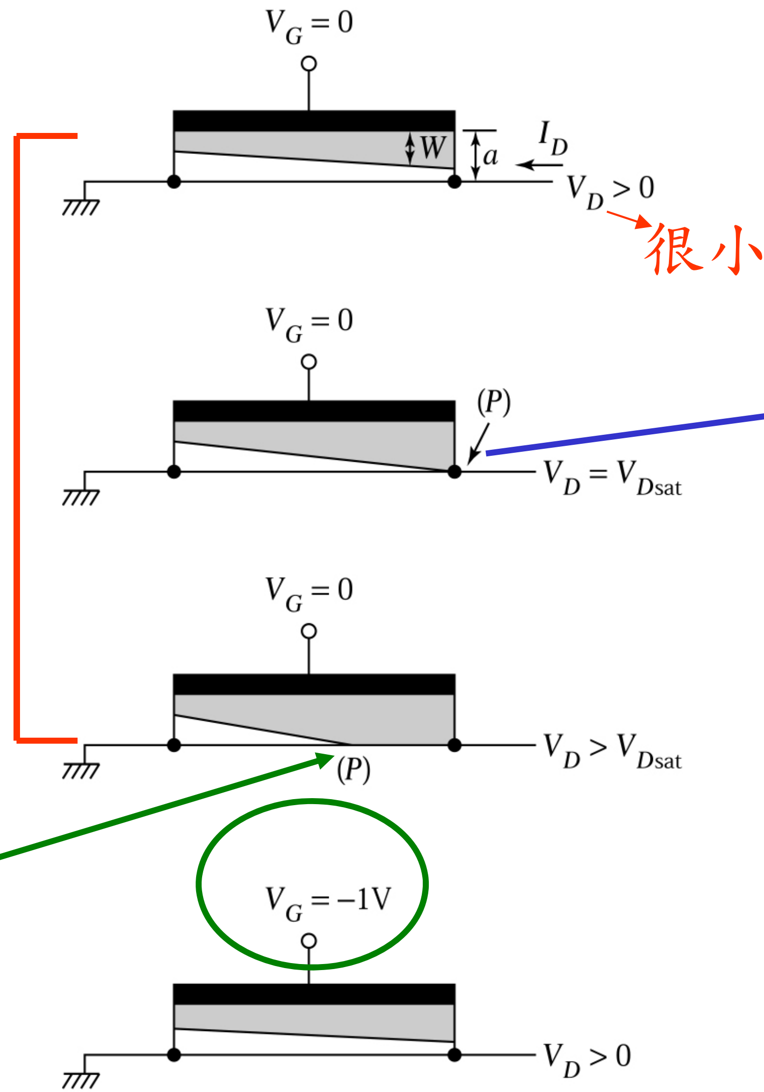
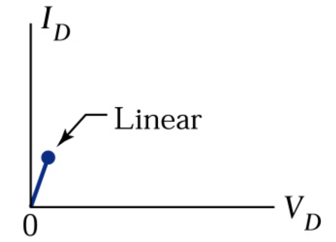
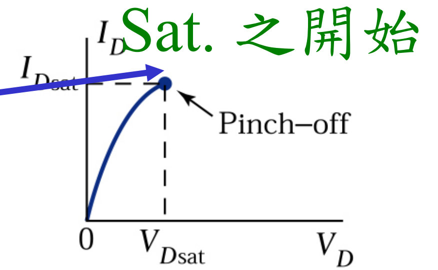
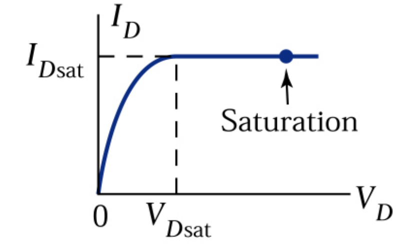
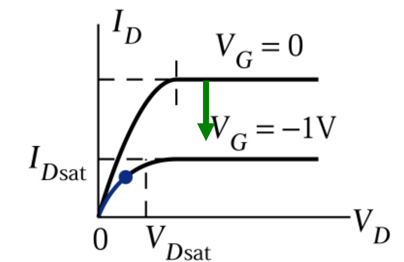
Figure 7.11.
Variation of the depletion-layer width and output characteristics of a MESFET under various biasing conditions. $V_G = 0$
(a) $V_G = 0$ and a small V_D.
(b) $V_G = 0$ and a pinch-off.
(c) $V_G = 0$ at post pinch-off ($V_D > V_{Dsat}$).
(d) $V_G = -1V$ and a small V_D.





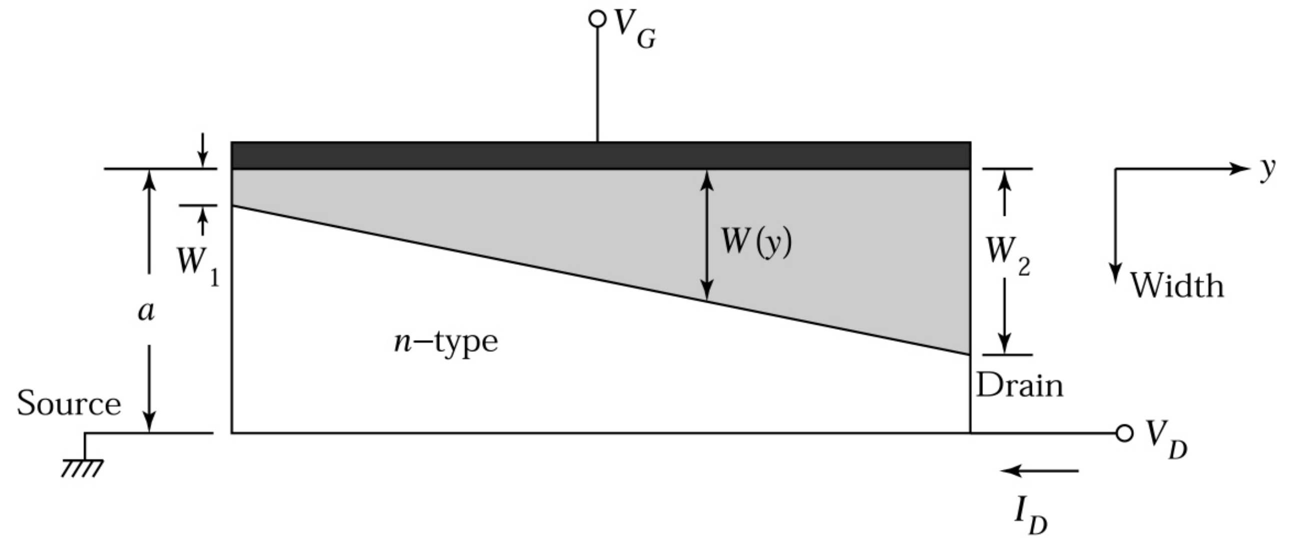


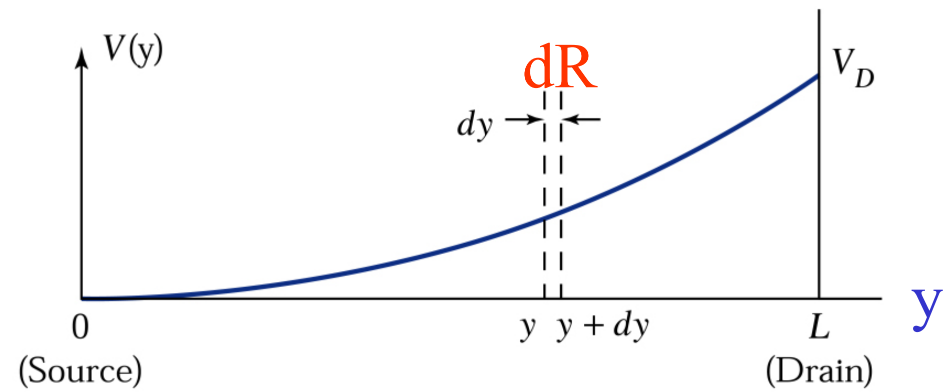


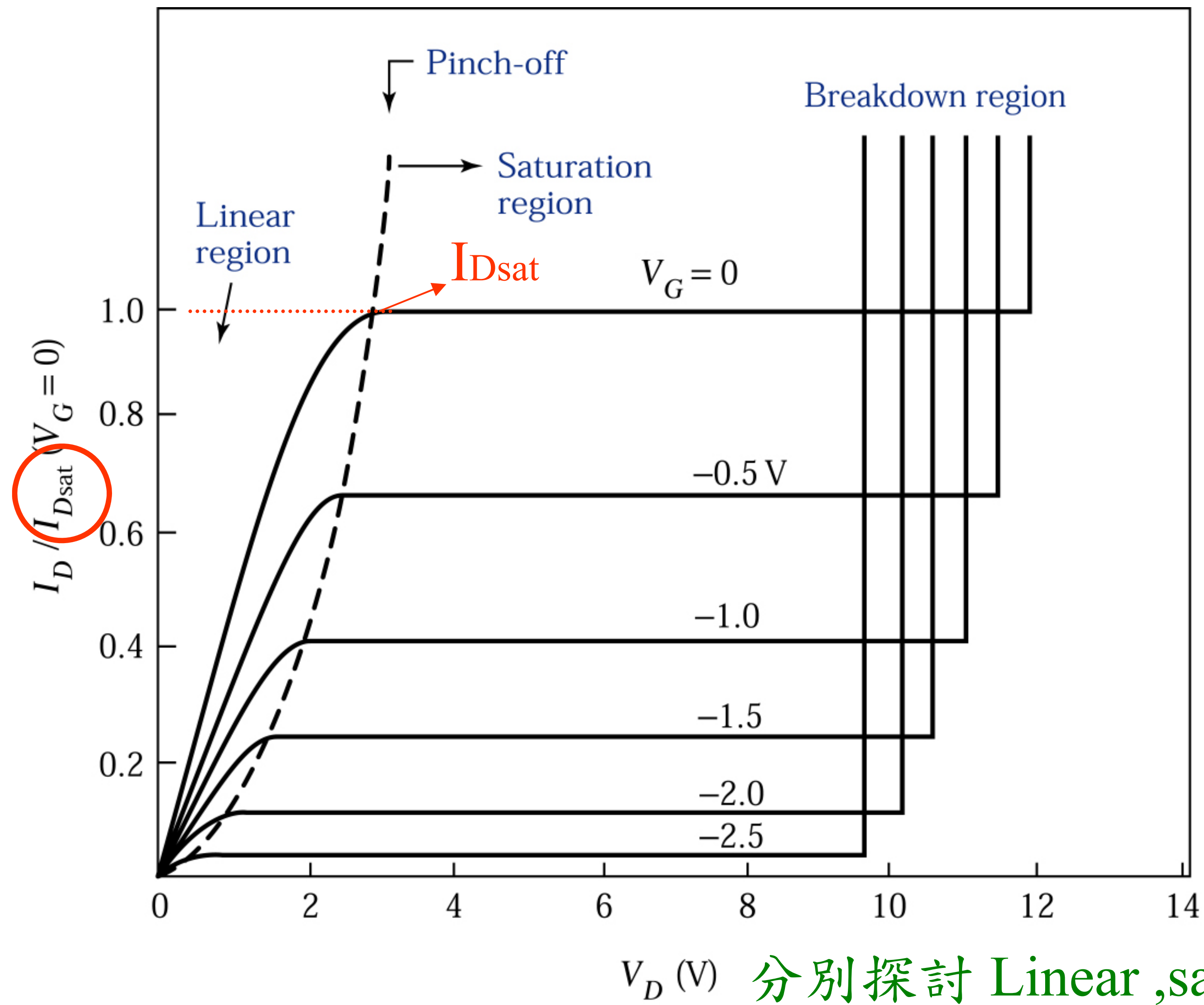


P點電壓仍為V_{Dsat}
壓降不變,I不變.

Figure 7.12.
(*a*) Expanded view of the channel region.
(*b*) Drain voltage variation along the channel.



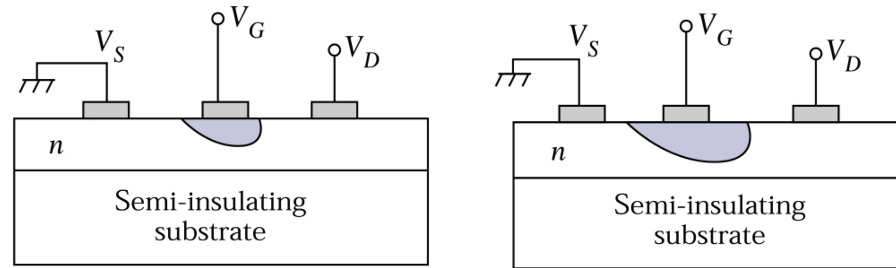


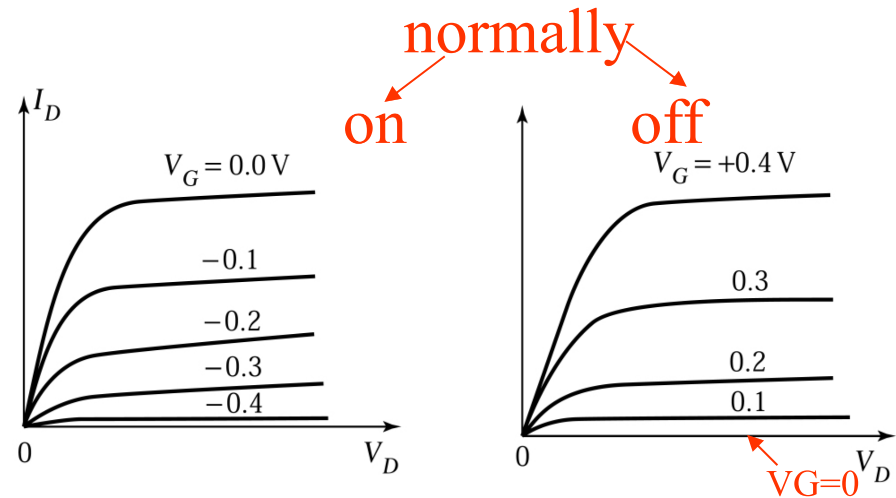


分別探討 Linear ,sat. region

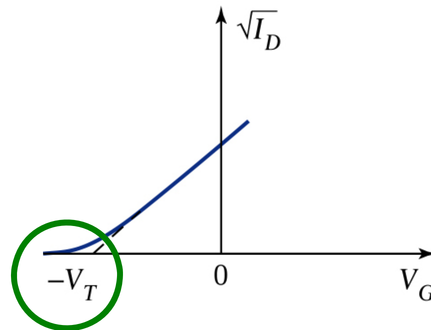
Figure 7.13. Normalized ideal current-voltage characteristics of a MESFET with $V_P = 3.2$ V.

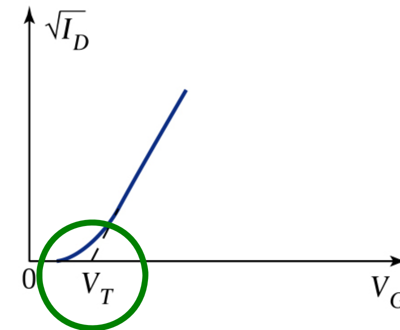
Figure 7.14.
Comparison of *I*-*V* characteristics.
(*a*) Normally on MESFET.
(*b*) Normally off MESFET.





求VT, in sat.





(a) (b)

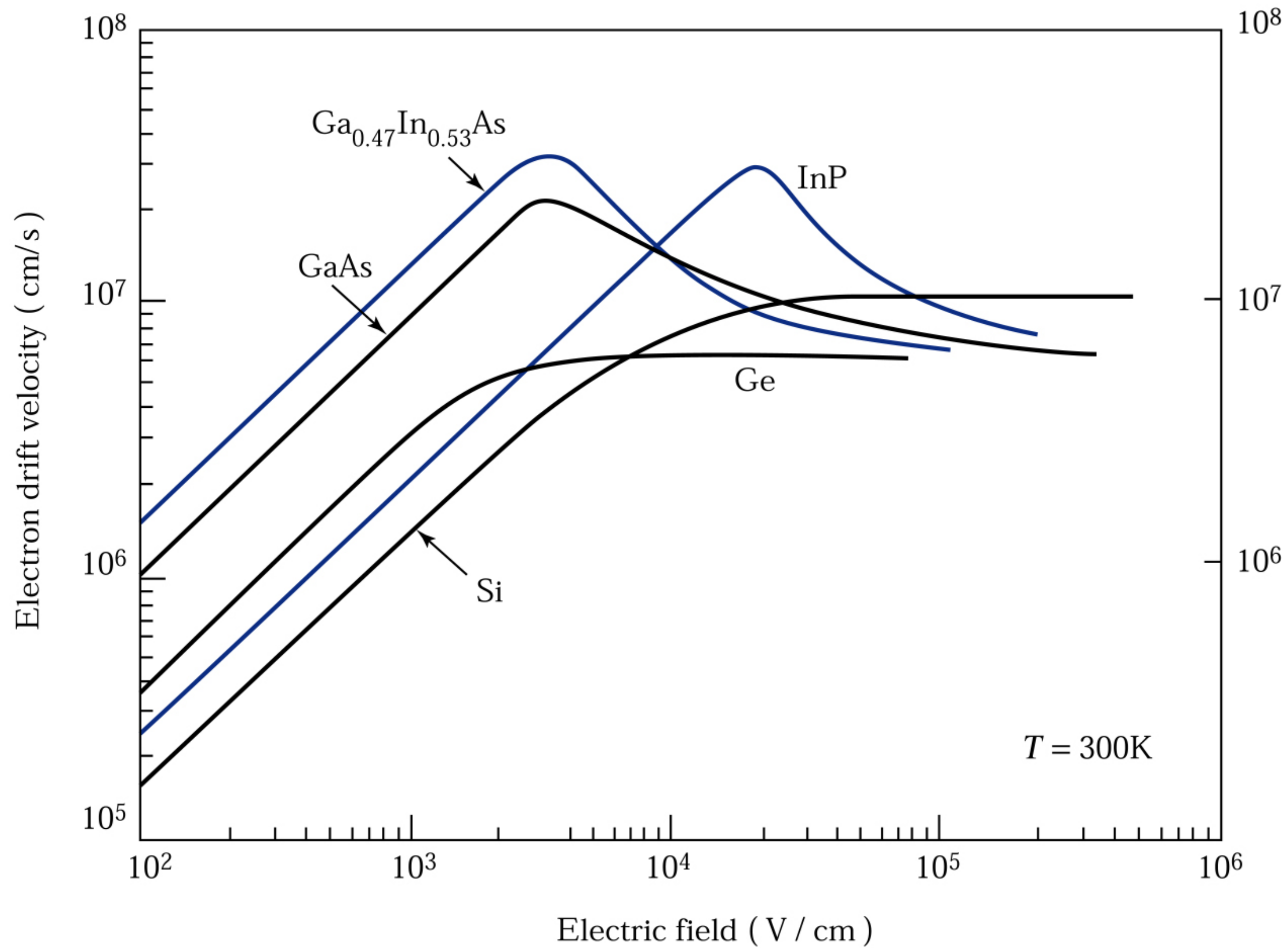


Figure 7.15. The drift velocity versus the electric field for electrons in various semiconductor materials.

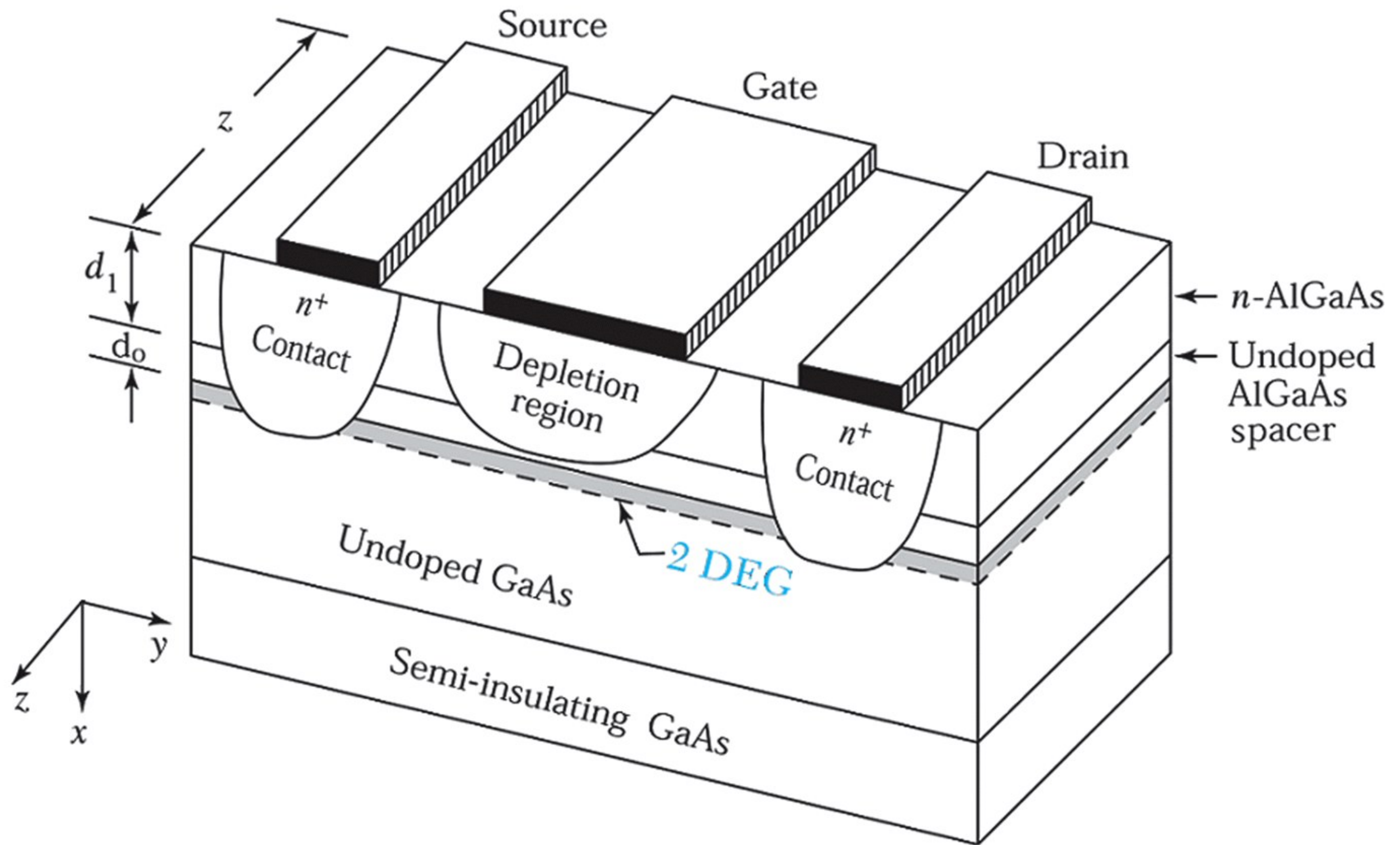


Figure 7.16
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Figure 7.16. Perspective view of a conventional modulation-doped field-effect transistor (MODFET) structure.

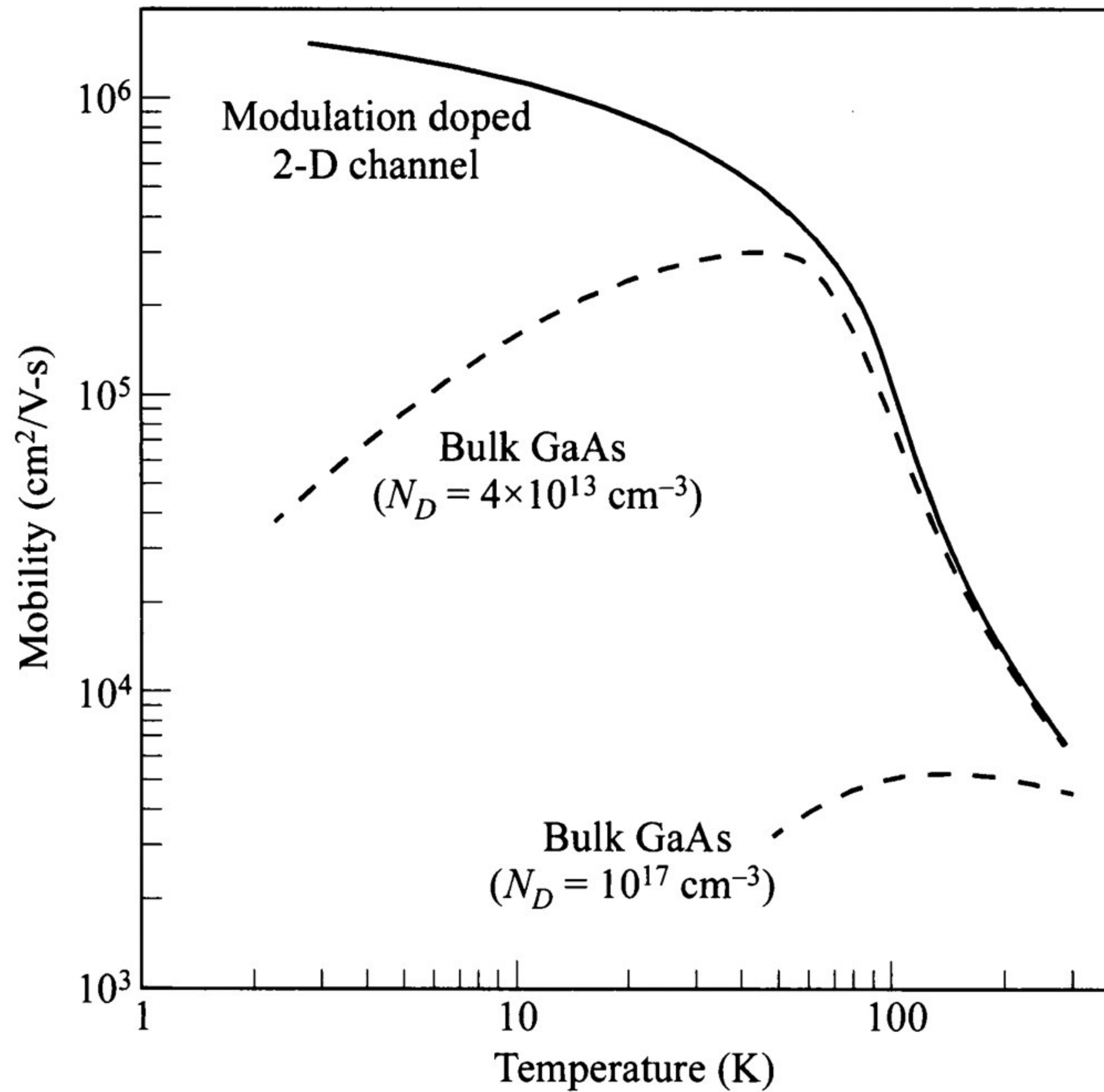

Figure 7.17

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Comparison of low-field electron mobility

Figure 7.18.
Energy band diagrams for a normally-off MODFET at (*a*) thermal equilibrium, and (*b*) the onset of threshold. ***d_1* and *d_0* are the doped and undoped regions,** respectively.

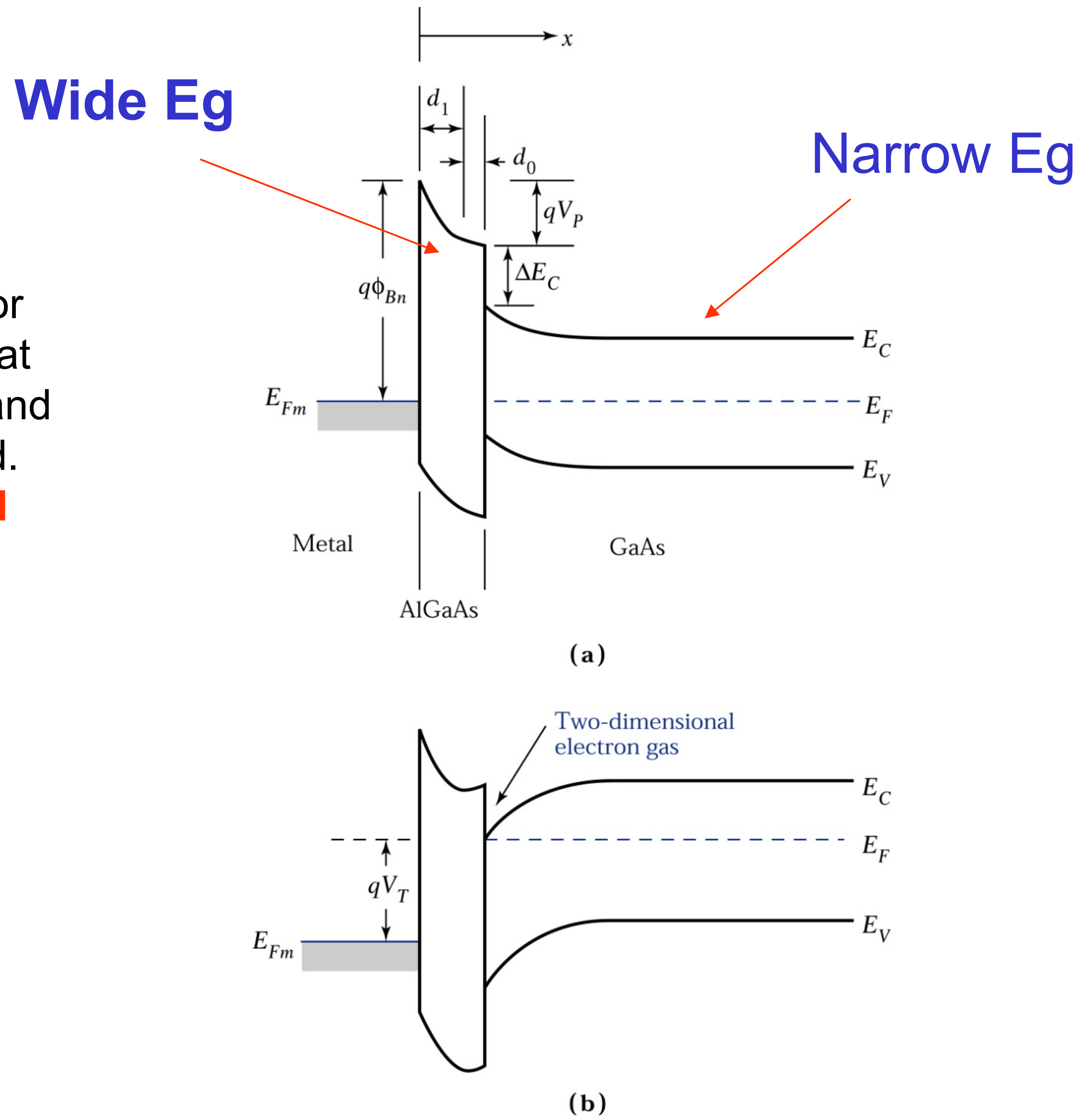

Figure 7.19. Cutoff frequency versus channel or gate length for five different field-effect transistors.[8,10]