Semiconductor Devices

THIRD EDITION

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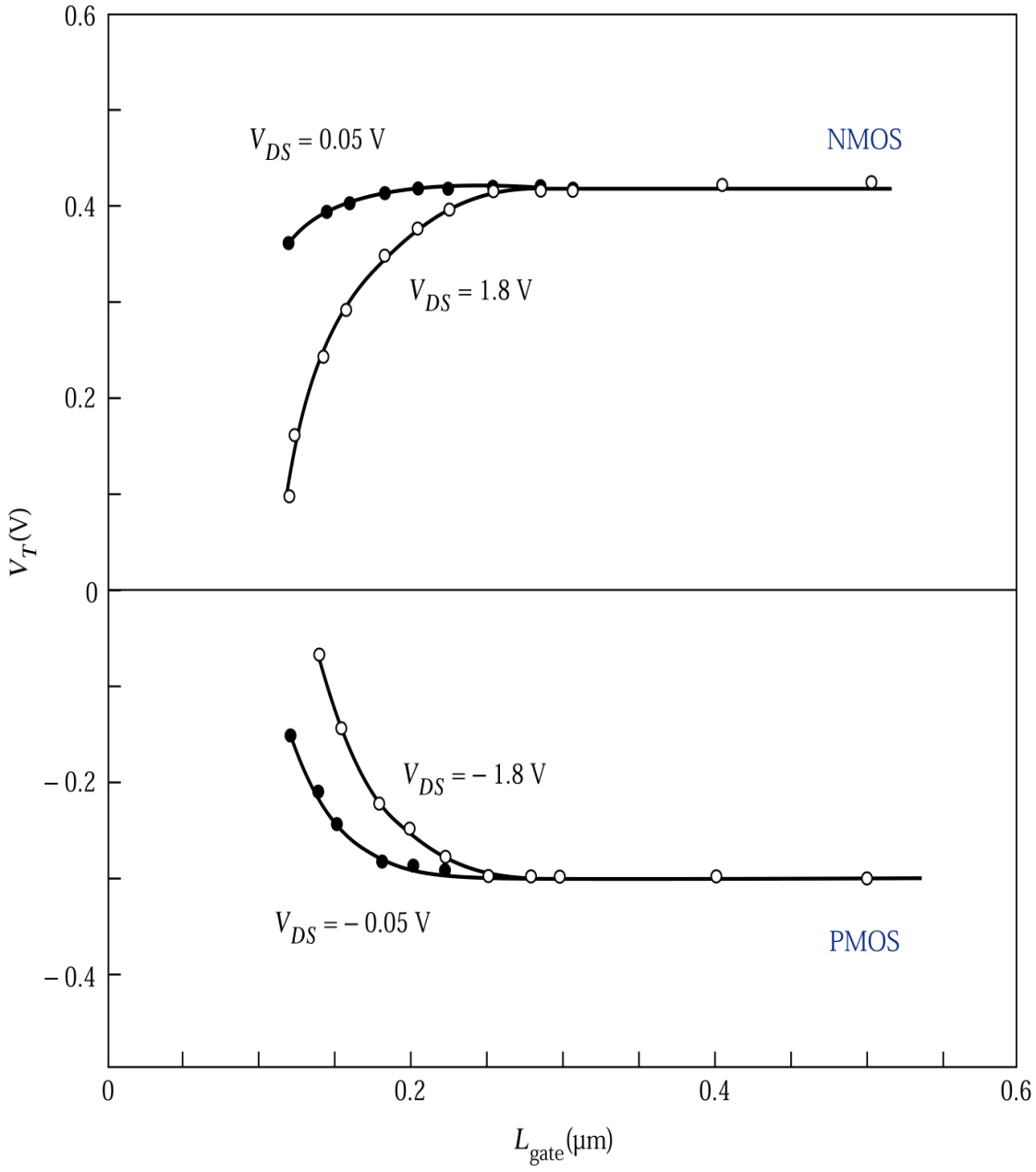
Chapter 6

Advanced MOSFET and Related Devices

Figure 6.1.
Threshold voltage **roll-off** characteristics in a 0.15 μm complementary metal-oxide-semiconductor (CMOS) field-effect transistor technology.[7]



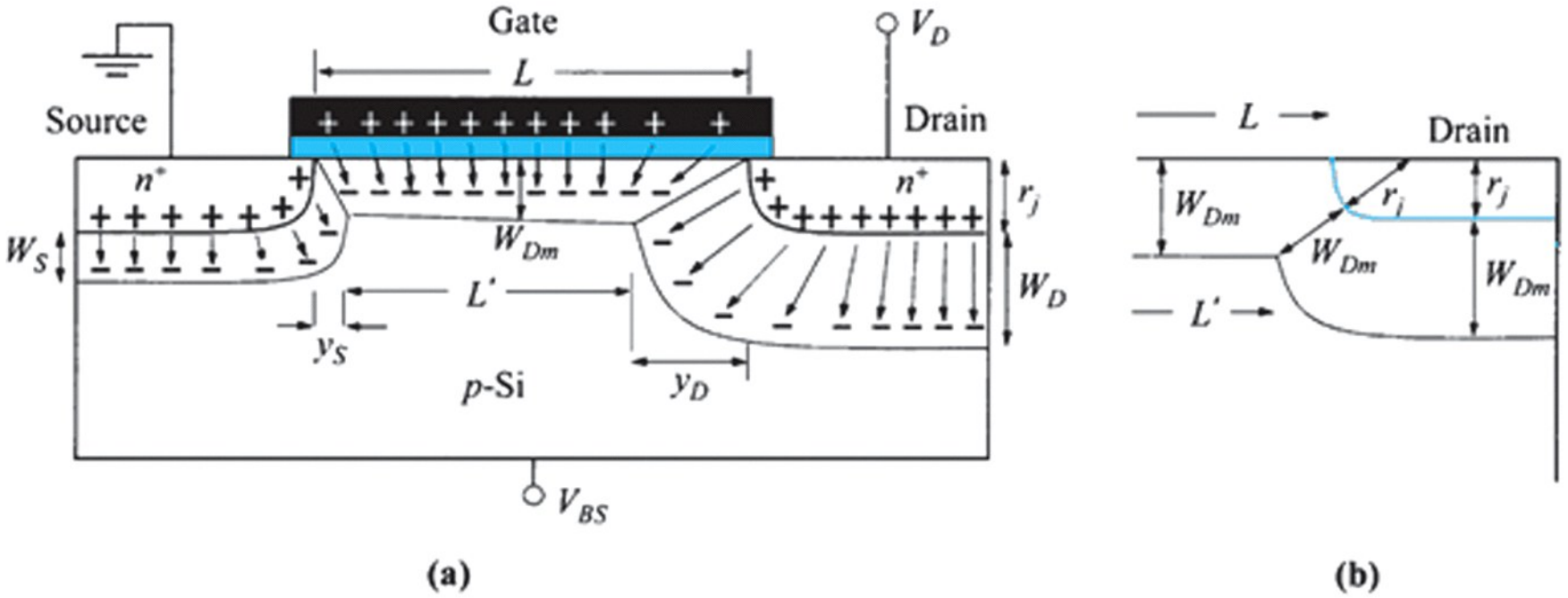


Figure 6.2ab

Charge conservation model, (a) $V_D>0$, (b) $V_D=0$

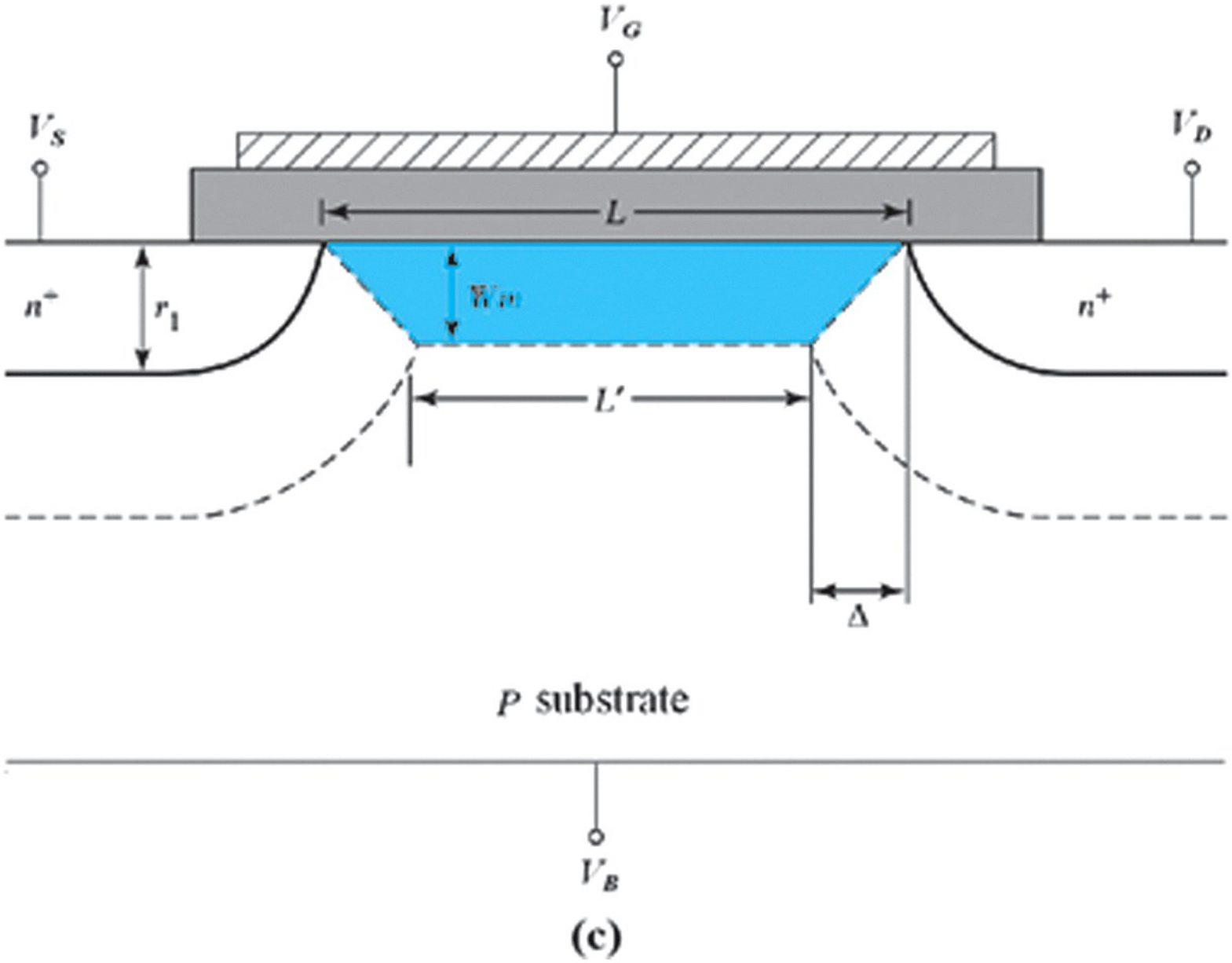
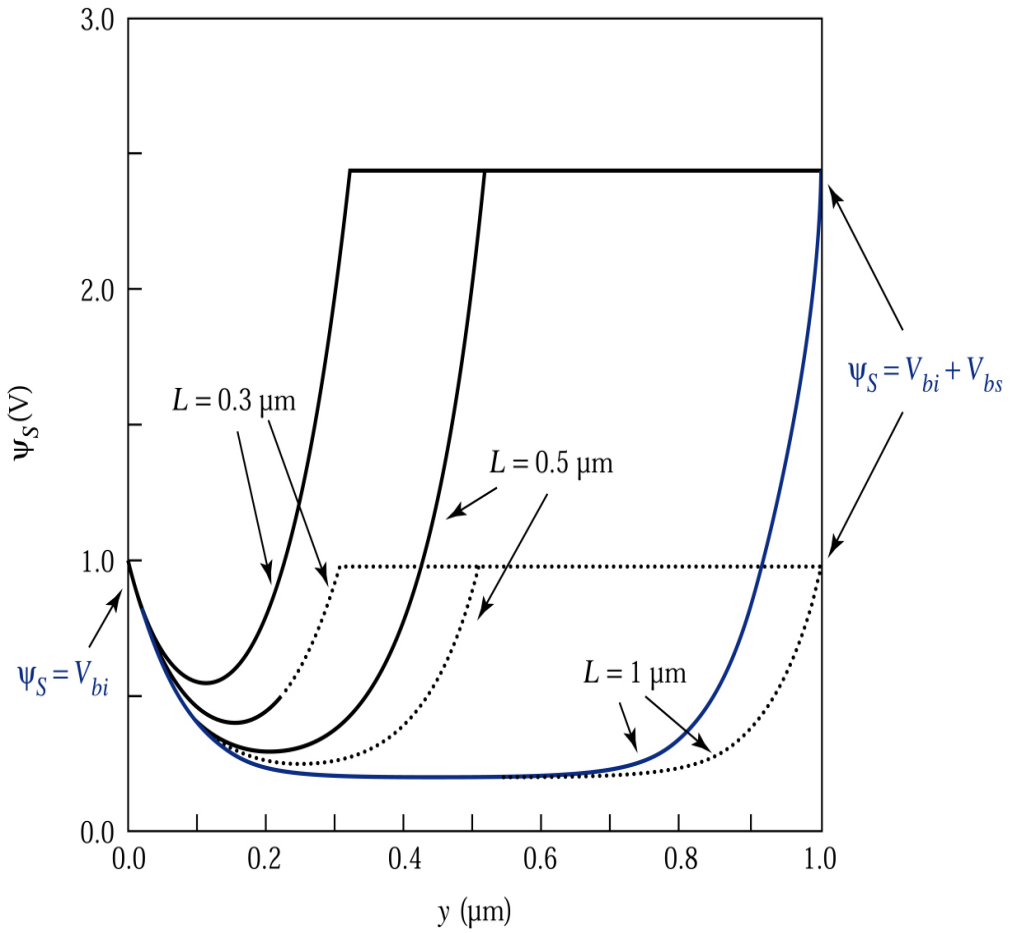


Figure 6.2c

Schematic of the charge sharing model.[8]



Calculated surface potential along the channel for *n*-channel MOSFETs with different channel lengths.[9] The source-channel boundary is at $y = 0$. A **low (0.05 V, dotted lines) and a high (1.5 V, sold lines) V_{DS}** are applied. Oxide thickness d and substrate doping N_A are 10 nm and 10^{16} cm^{-3}, respectively. The substrate bias is 0 V.

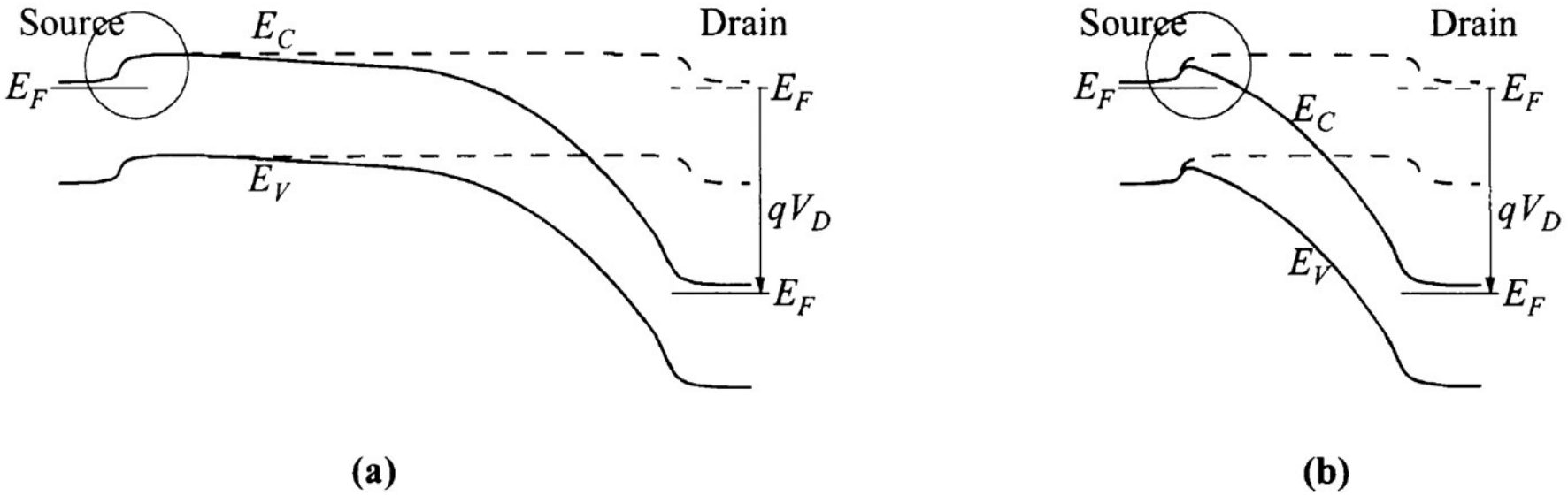


Figure 6.3

Band diagram from source to drain, (a) long L, (b) short L, dash line: V_D=0, solid line: V_D > 0

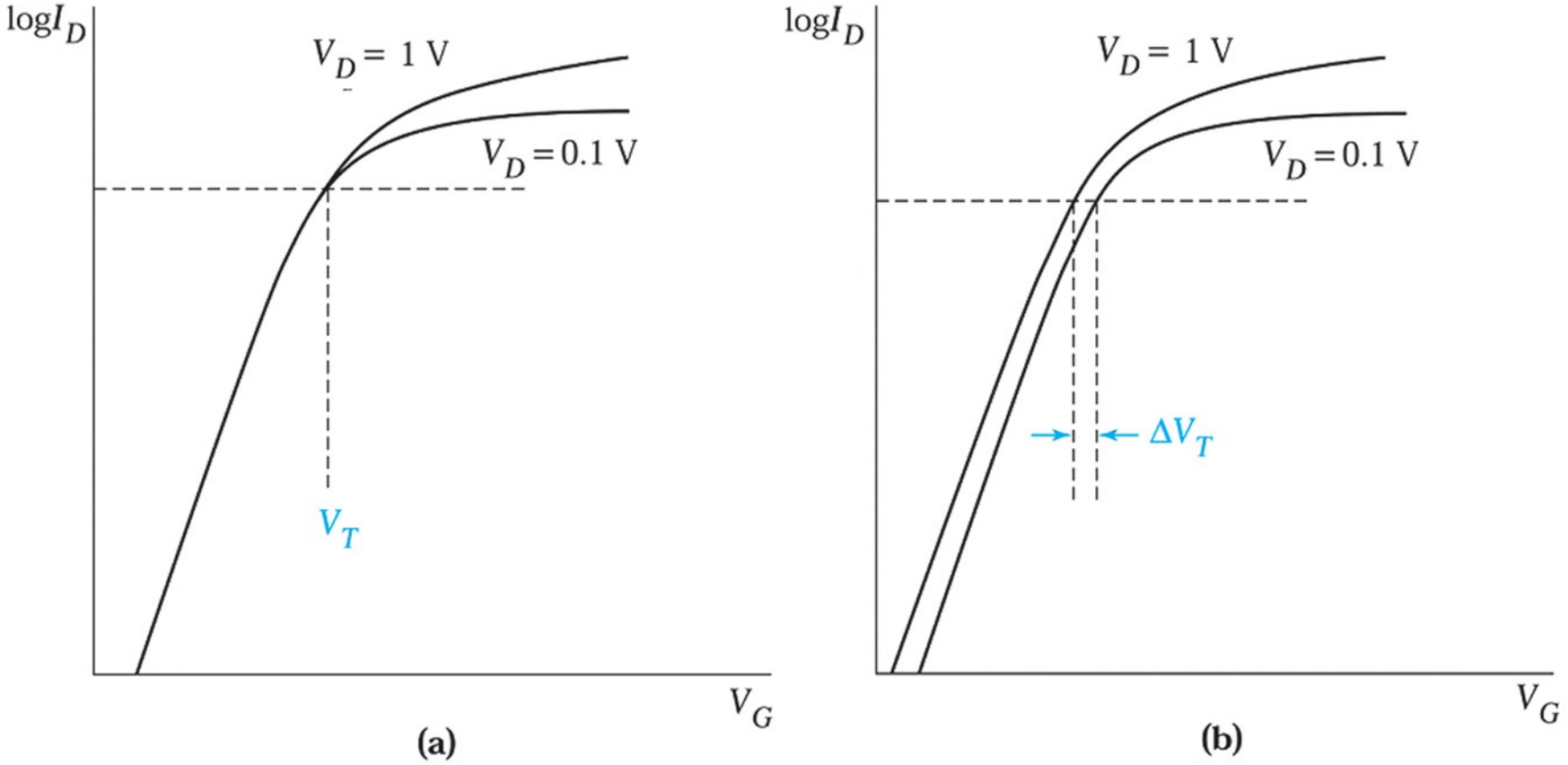


Figure 6.4

Figure 6.4.
Subthreshold characteristics of
(*a*) a long-channel and
(b) a short-channel MOSFET.

DIBL: Drain-Induced Barrier Lowering

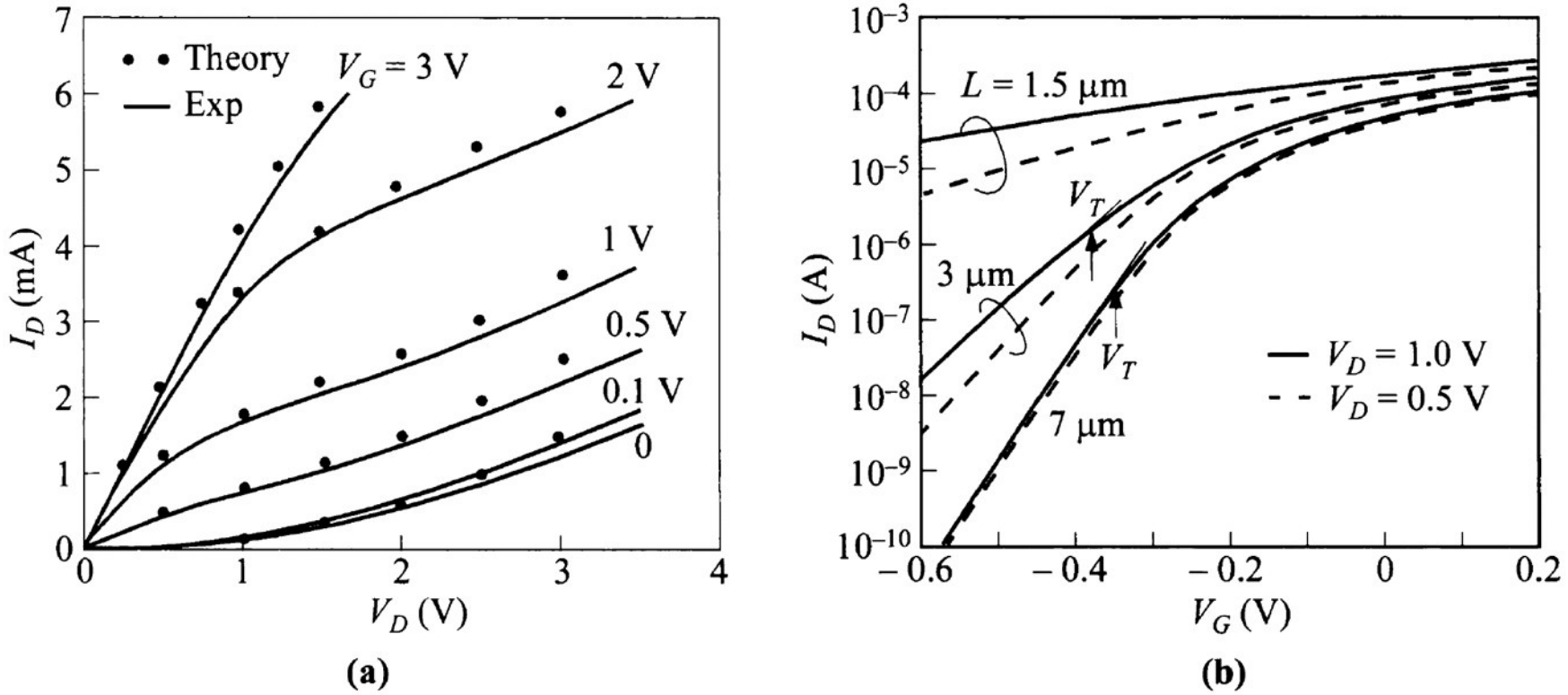


Figure 6.5

Punch-through, (a) above threshold, (b) below threshold

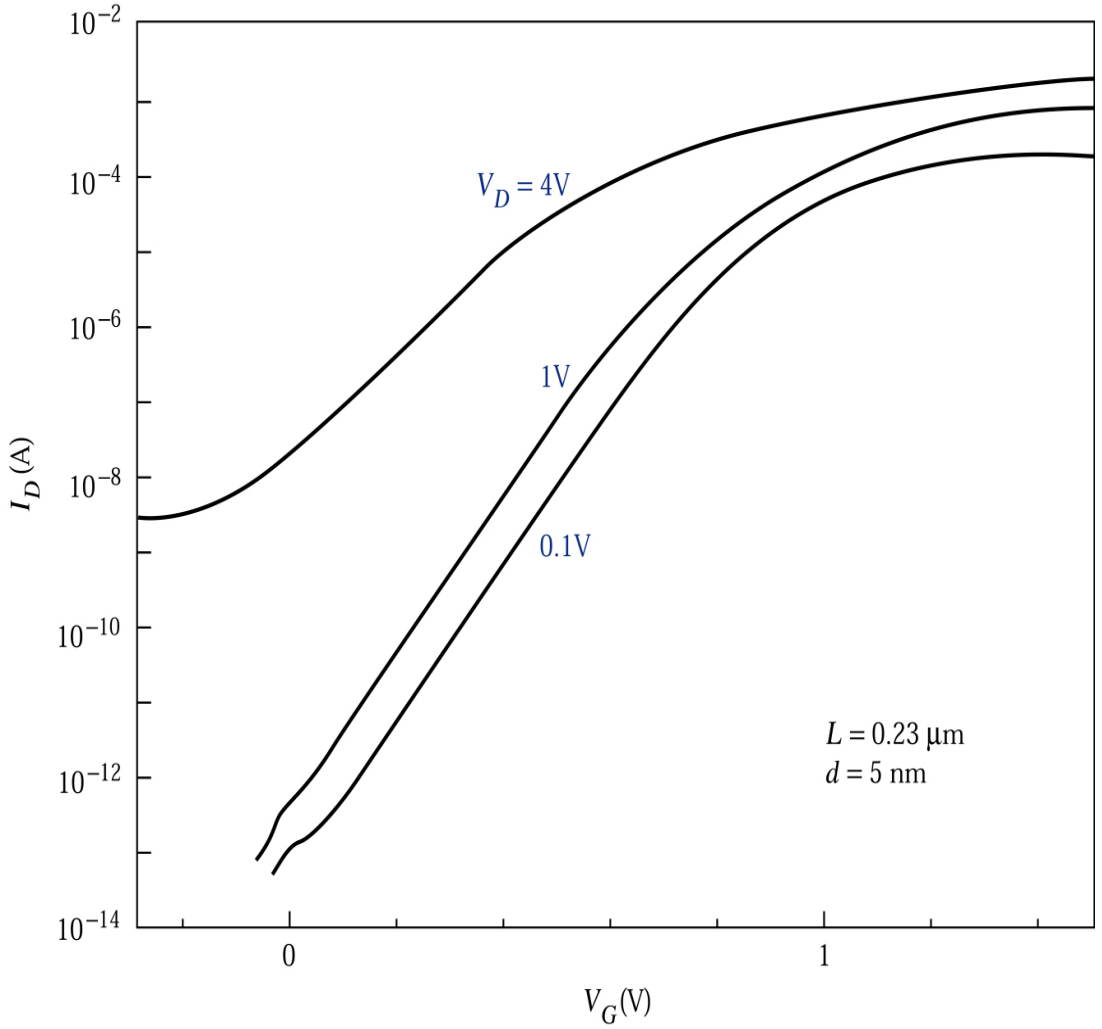


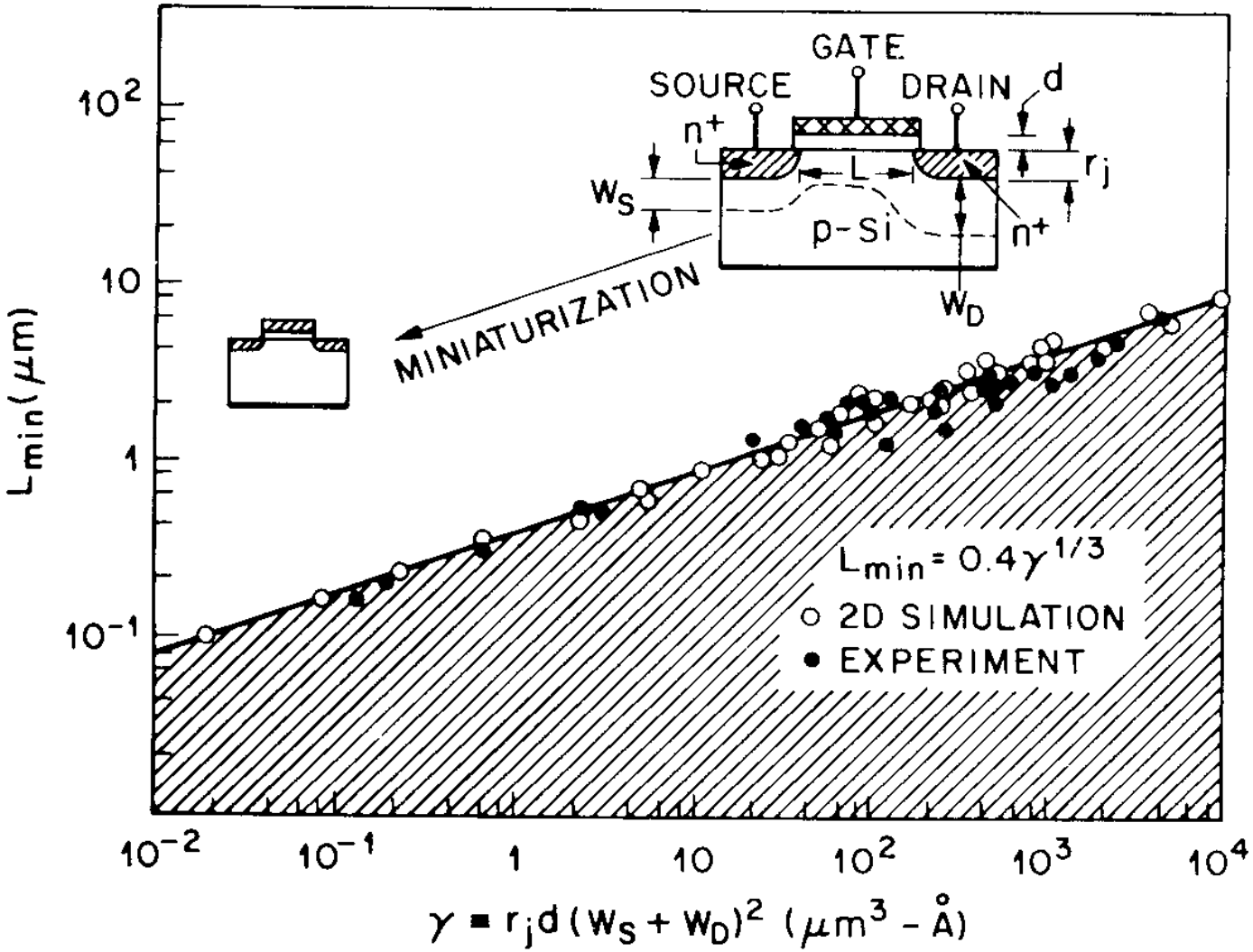
Figure 6.6. Subthreshold characteristics of an *n*-channel MOSFET with V_{DS} = 0.1, 1, and 4 V.

TABLE 1 Scaling of MOSFET Device and Circuit Parameters

Determinant	MOSFET device and circuit parameters	Multiplying factor ($\kappa > 1$)
Scaling assumptions	Device dimensions (d, L, W, r_j)	$1/\kappa$
	Doping concentration (N_A, N_D)	κ
	Voltage (V)	$1/\kappa$
Derived scaling behavior of device parameters	Electric field ($\mathscr{E}$)	1
	Carrier velocity (υ)	1
	Depletion-layer width (W)	$1/\kappa$
	Capacitance ($C = \varepsilon A/d$)	$1/\kappa$
	Inversion-layer charge density (Q_n)	1
	Current, drift (I)	$1/\kappa$
	Channel resistance (R)	1
Derived scaling behavior of circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/\kappa$
	Power dissipation per circuit ($P \sim VI$)	$1/\kappa^2$
	Power-delay product per circuit ($P\tau$)	$1/\kappa^3$
	Circuit density ($\sim 1/A$)	κ^2
	Power density (P/A)	1

Table 6.1

Scaling of MOS counts on d, rj, or Wd/Ws



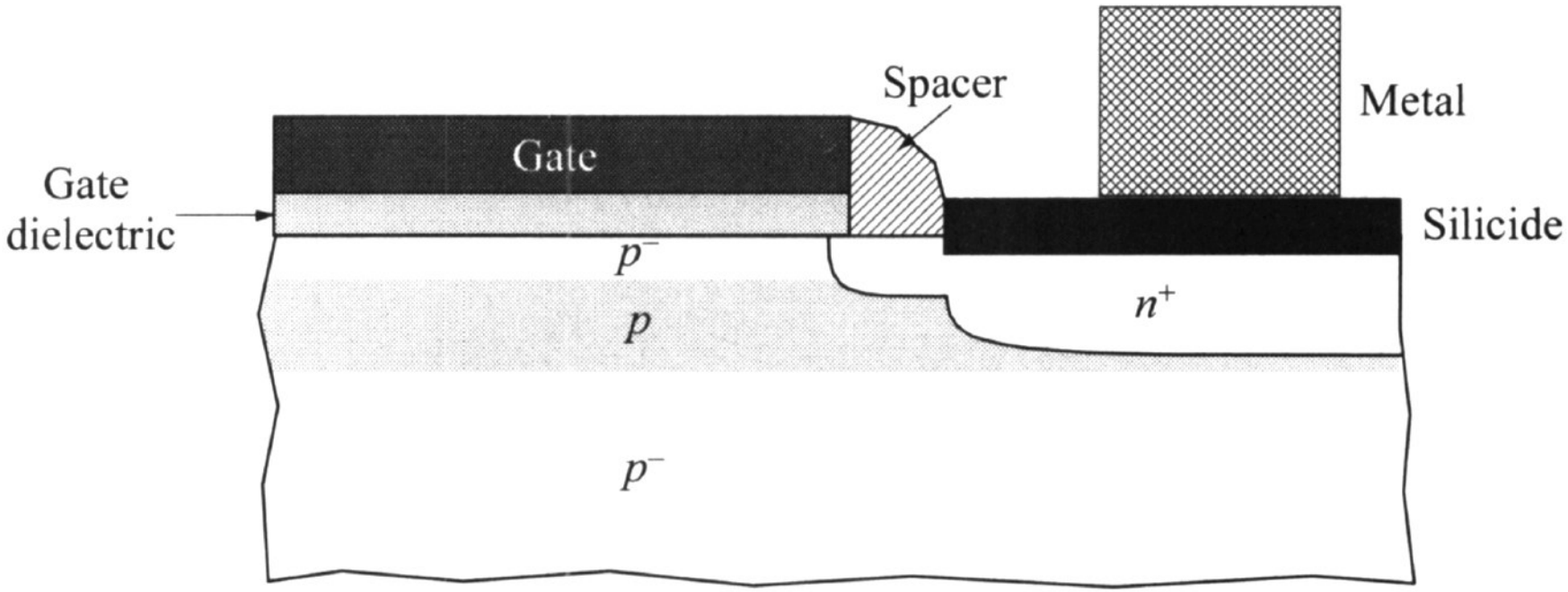


Figure 6.7

Retrograde channel doping profile
Upper P^-: mobility improvement
Middle P: control punch-through, short L effects
Bottom P^-: reduce Cj, body effect

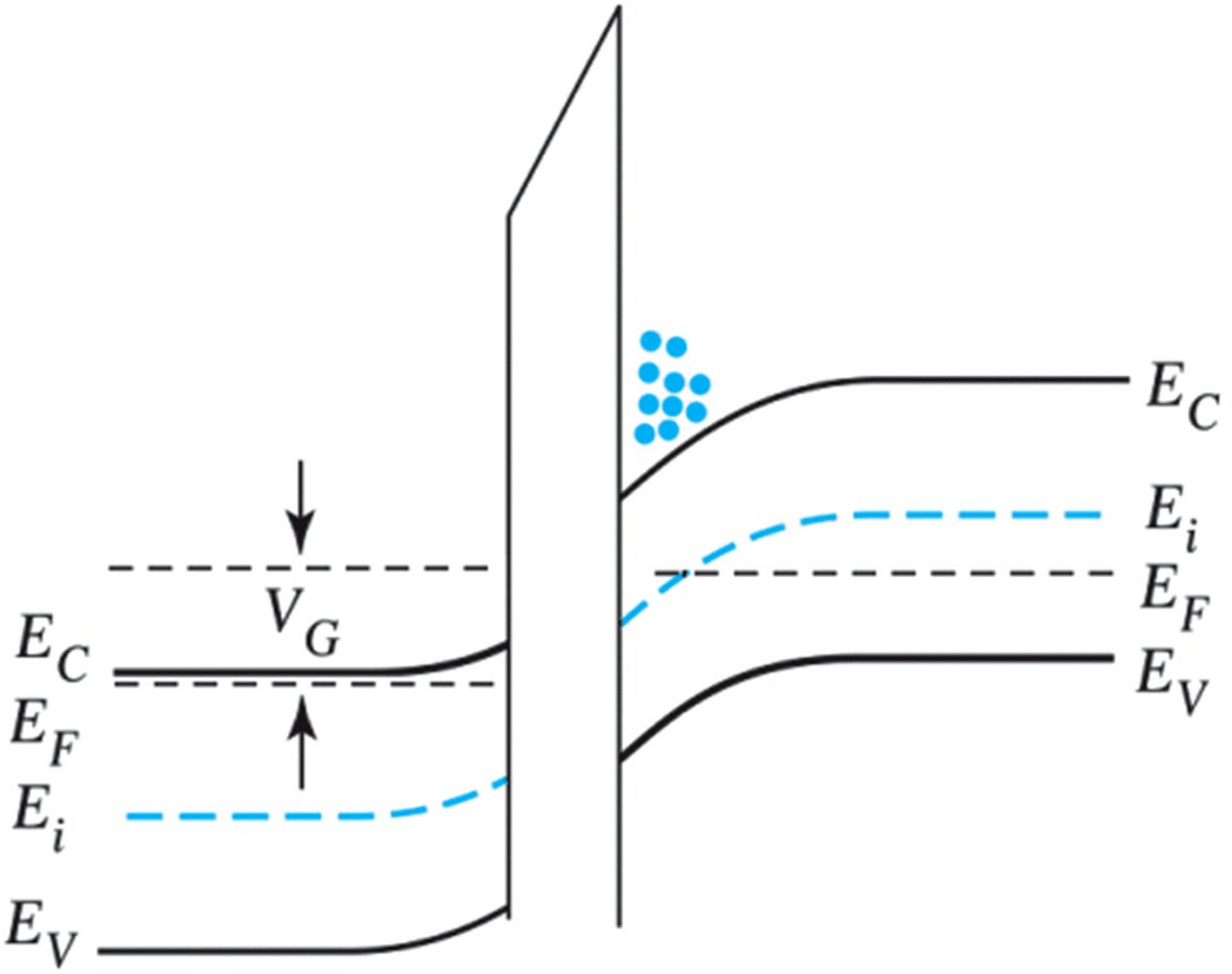


Figure 6.8a

poly-Si gate depletion effects

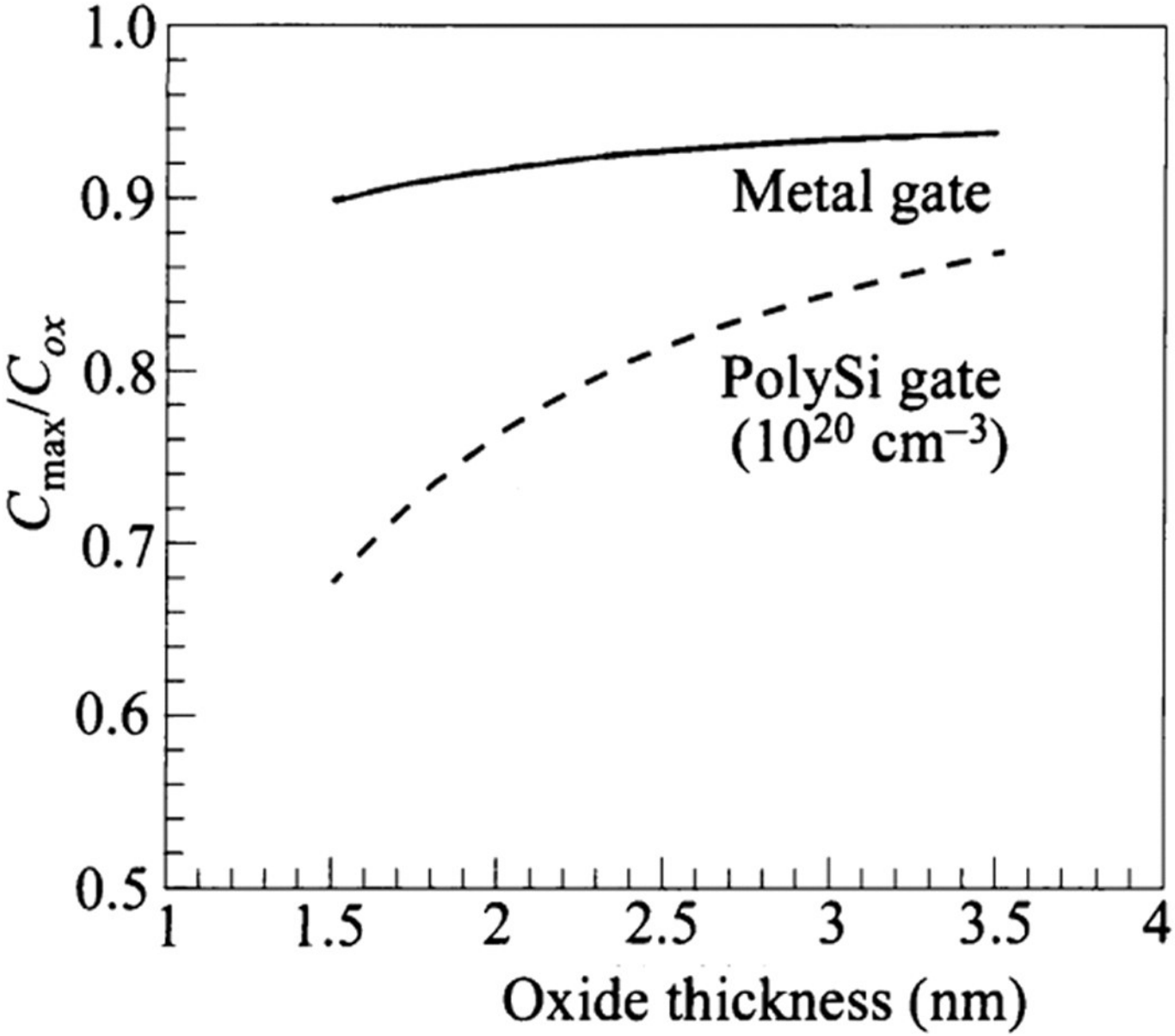


Figure 6.8b

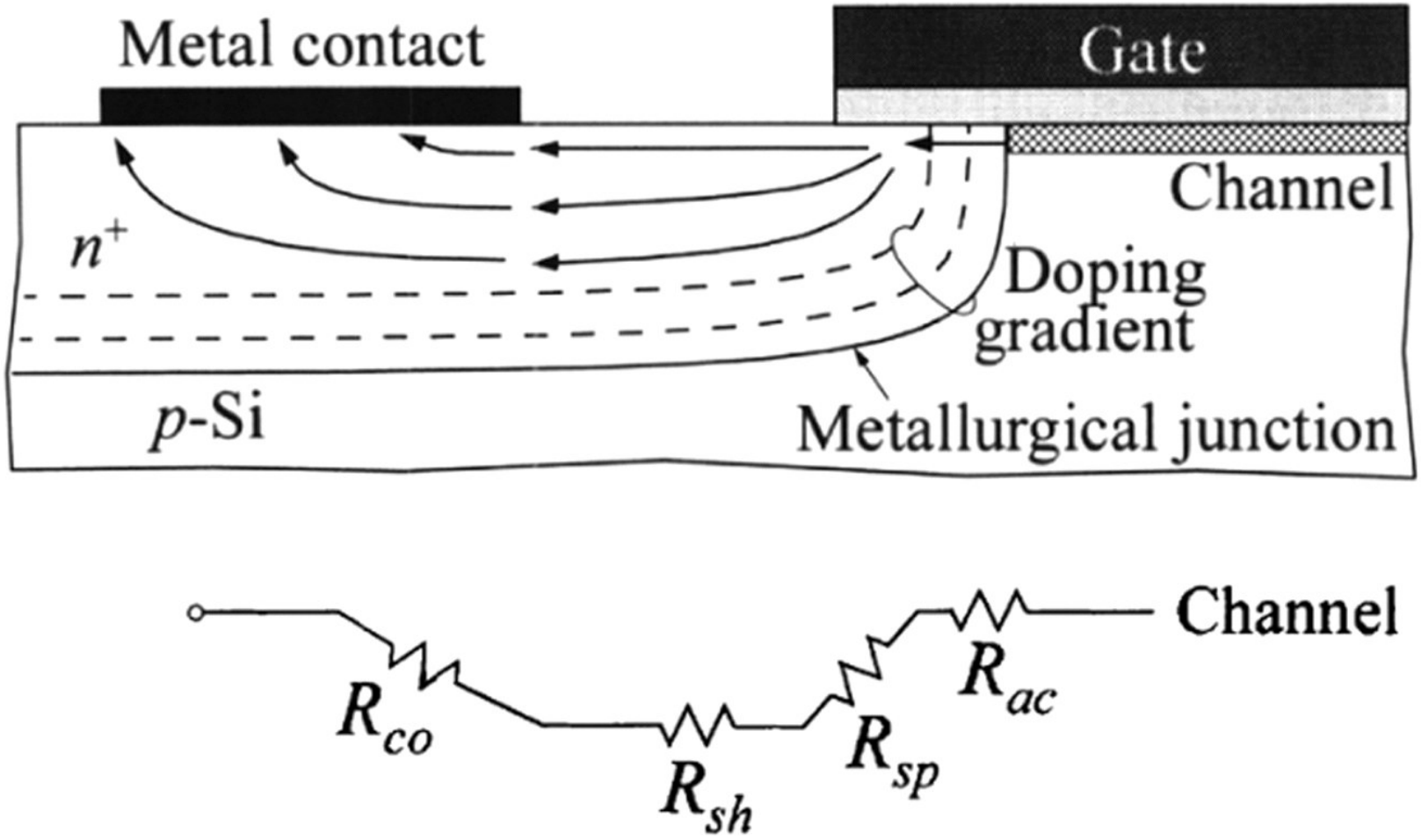


Figure 6.9

Different components of parasitic S/D series resistance

Schottky-barrier S/D

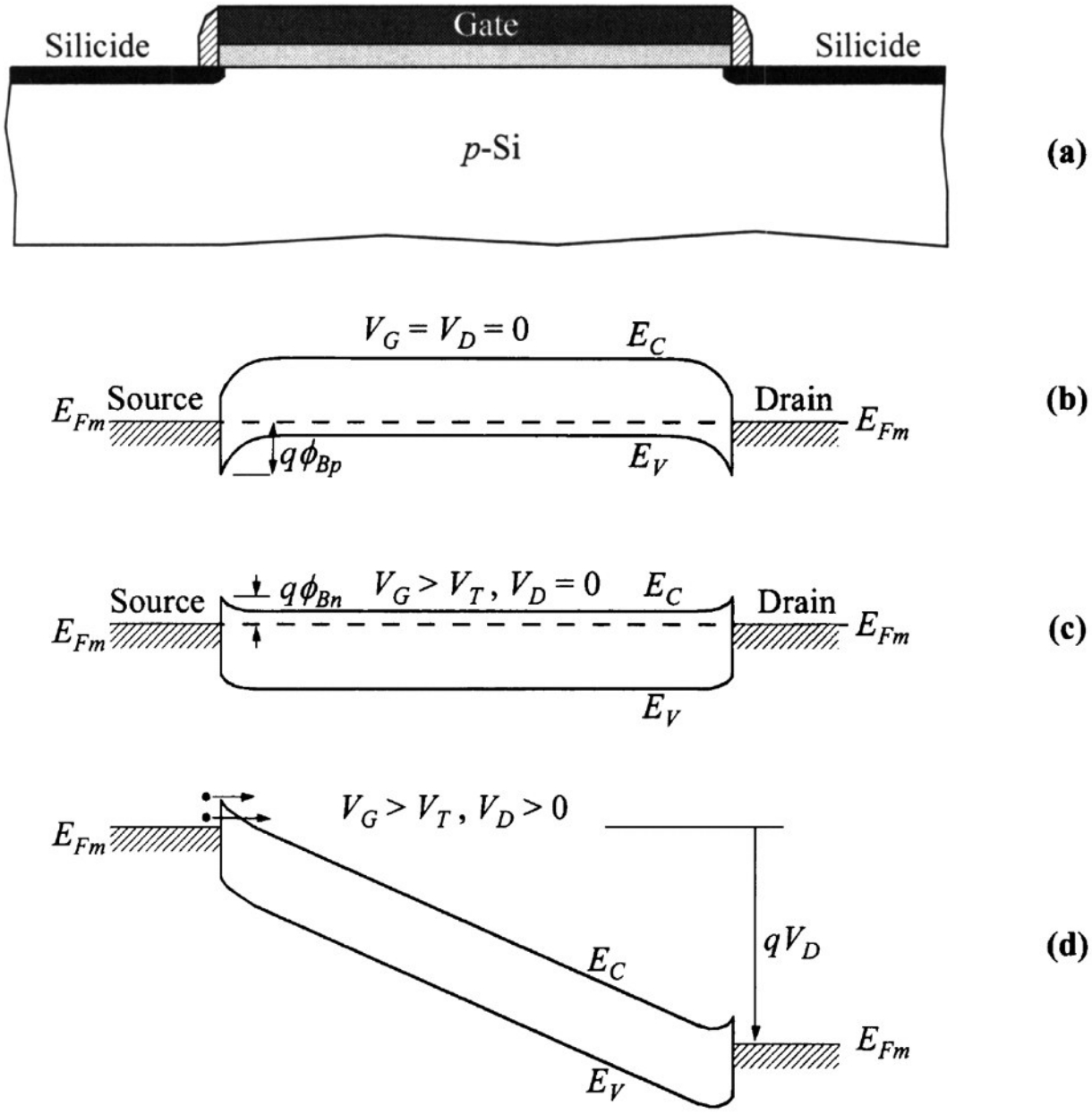


Figure 6.10

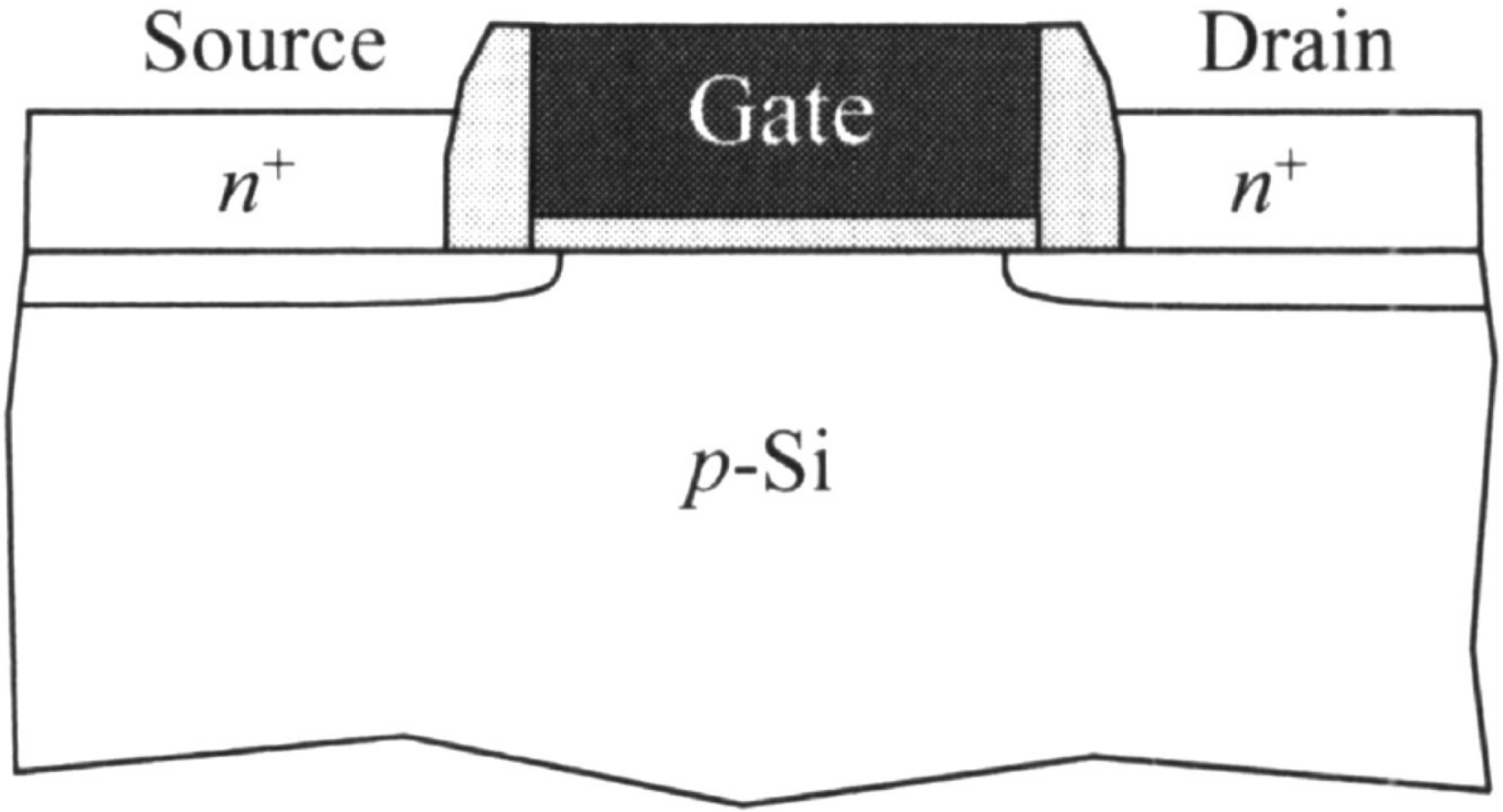
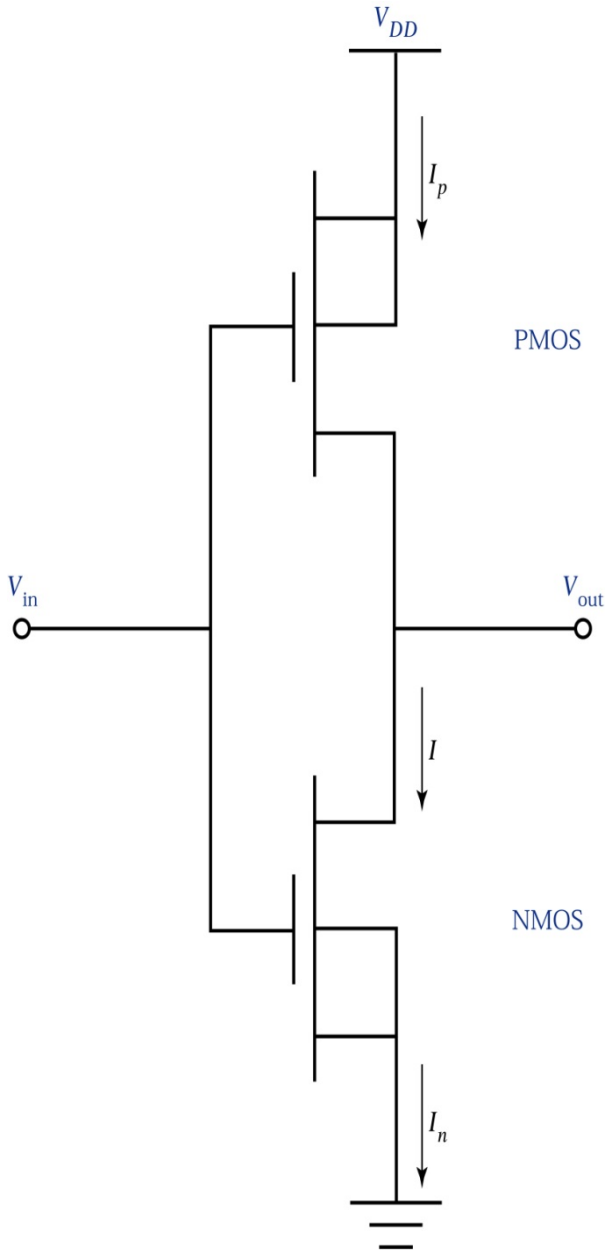


Figure 6.11

Raised S/D to reduce junction depth and series resistance

Figure 6.12. The CMOS inverter.



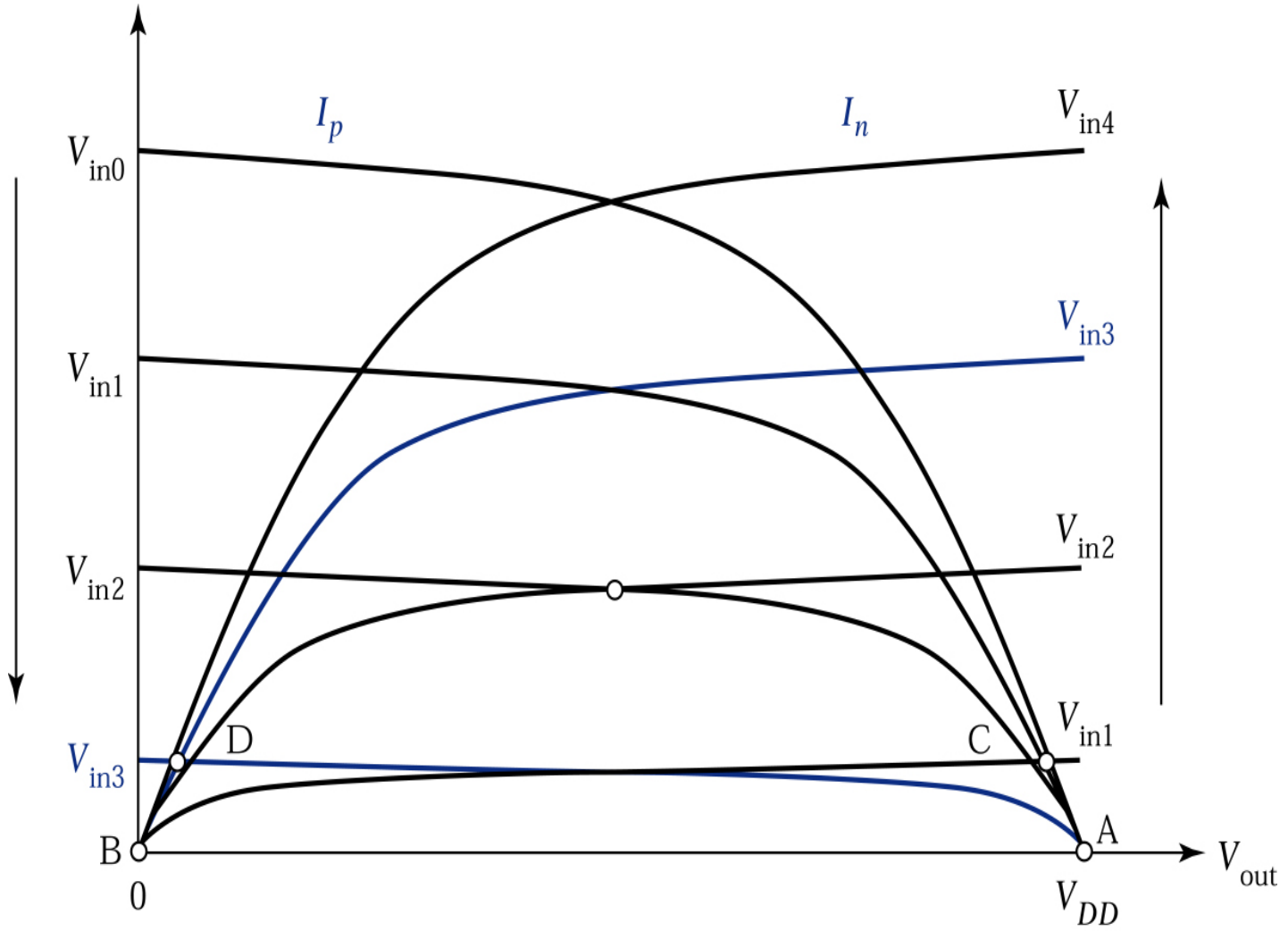
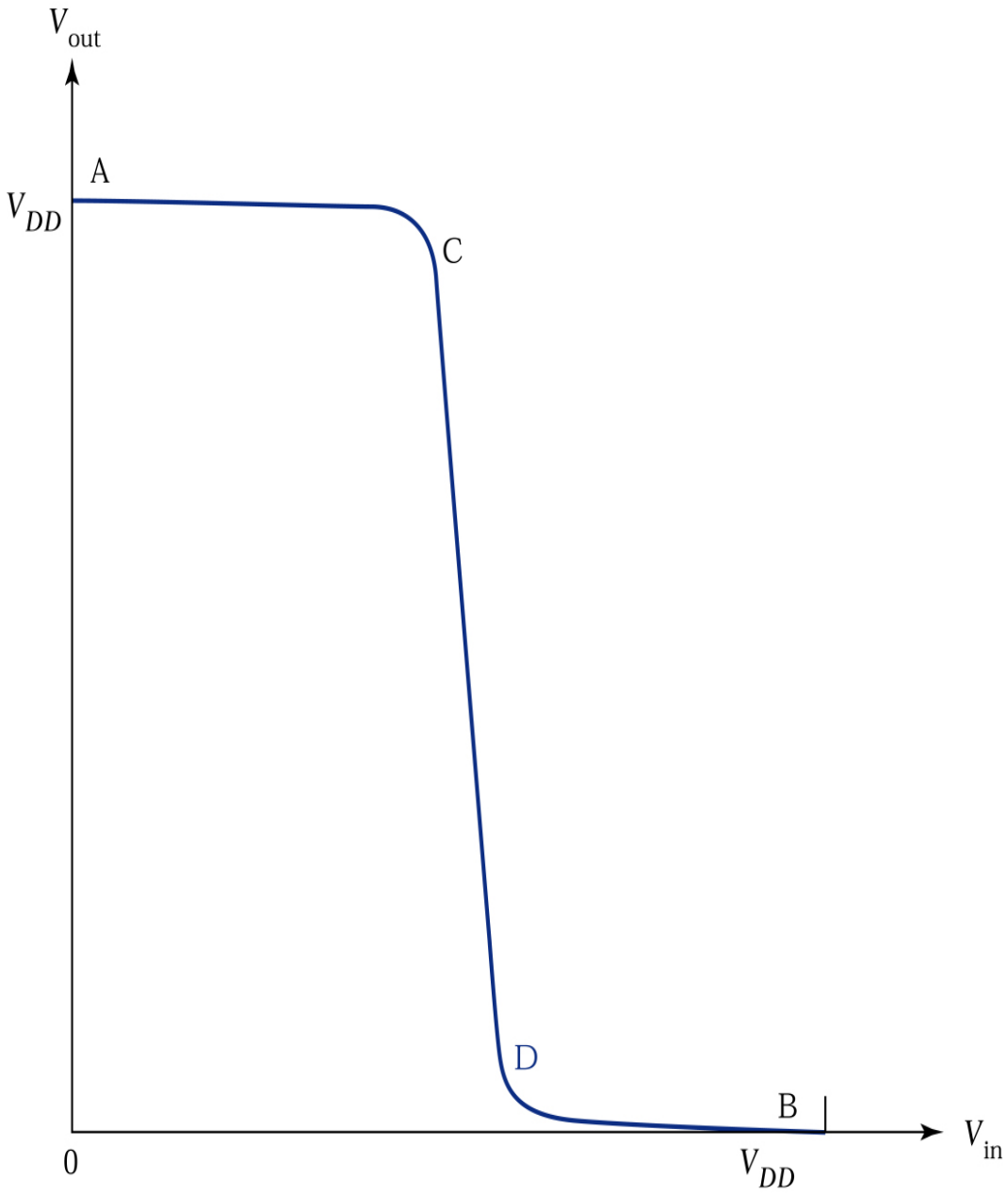


Figure 6.13. I_p and I_n as a function of V_{out}. The intercepts of I_p and I_n (circled) represent the steady-state operation points of the CMOS inverter.[11] The curves are labeled by the input voltages: $0 = V_{in0} < V_{in1} < V_{in2} < V_{in3} < V_{in4} = V_{DD}$.

Figure 6.14.
Transfer curve of a CMOS inverter.[11] Points labeled A, B, C, and D correspond to those points labeled in Fig. 13.



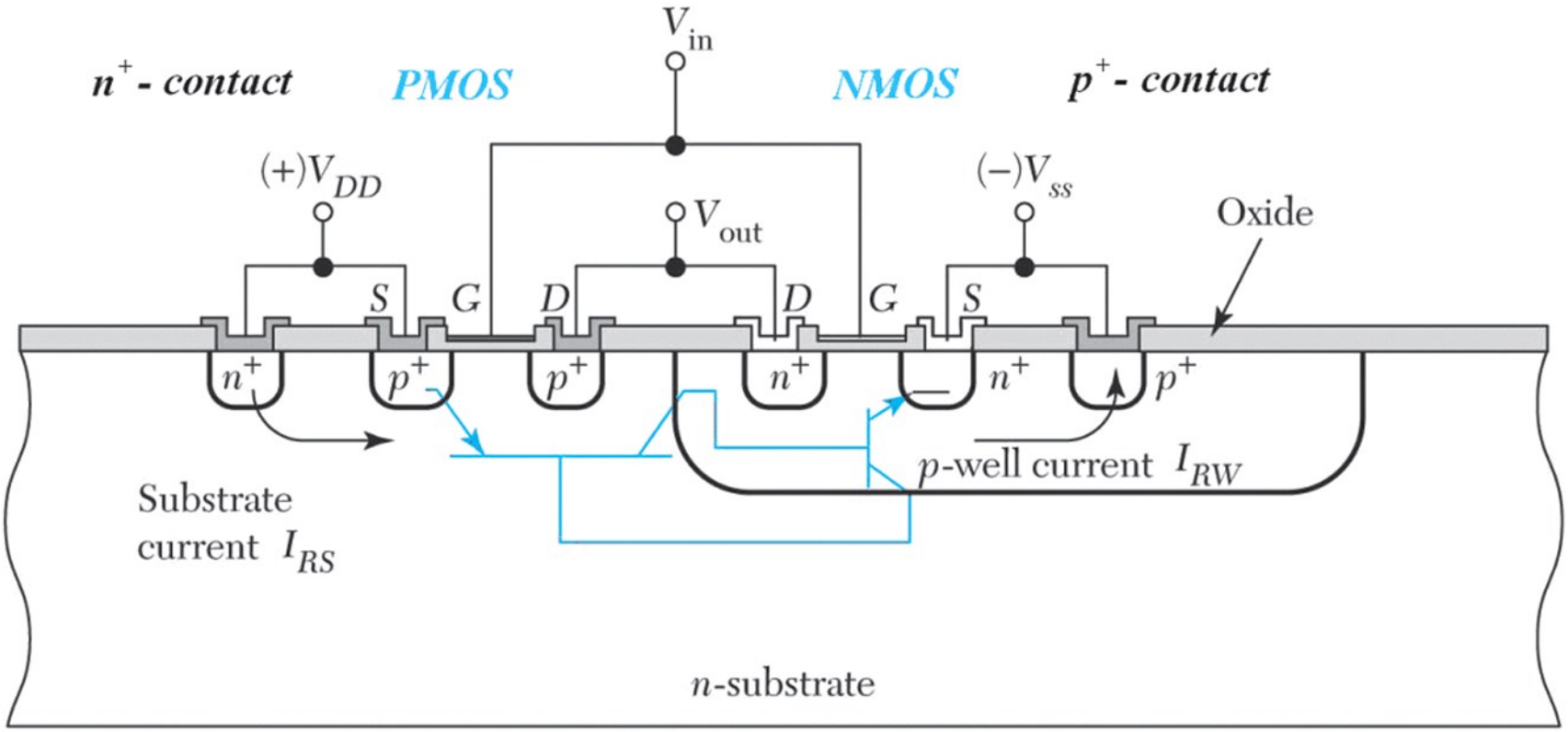


Figure 6.15

Figure 6.15. Cross section of a CMOS inverter fabricated with *p*-well technology.

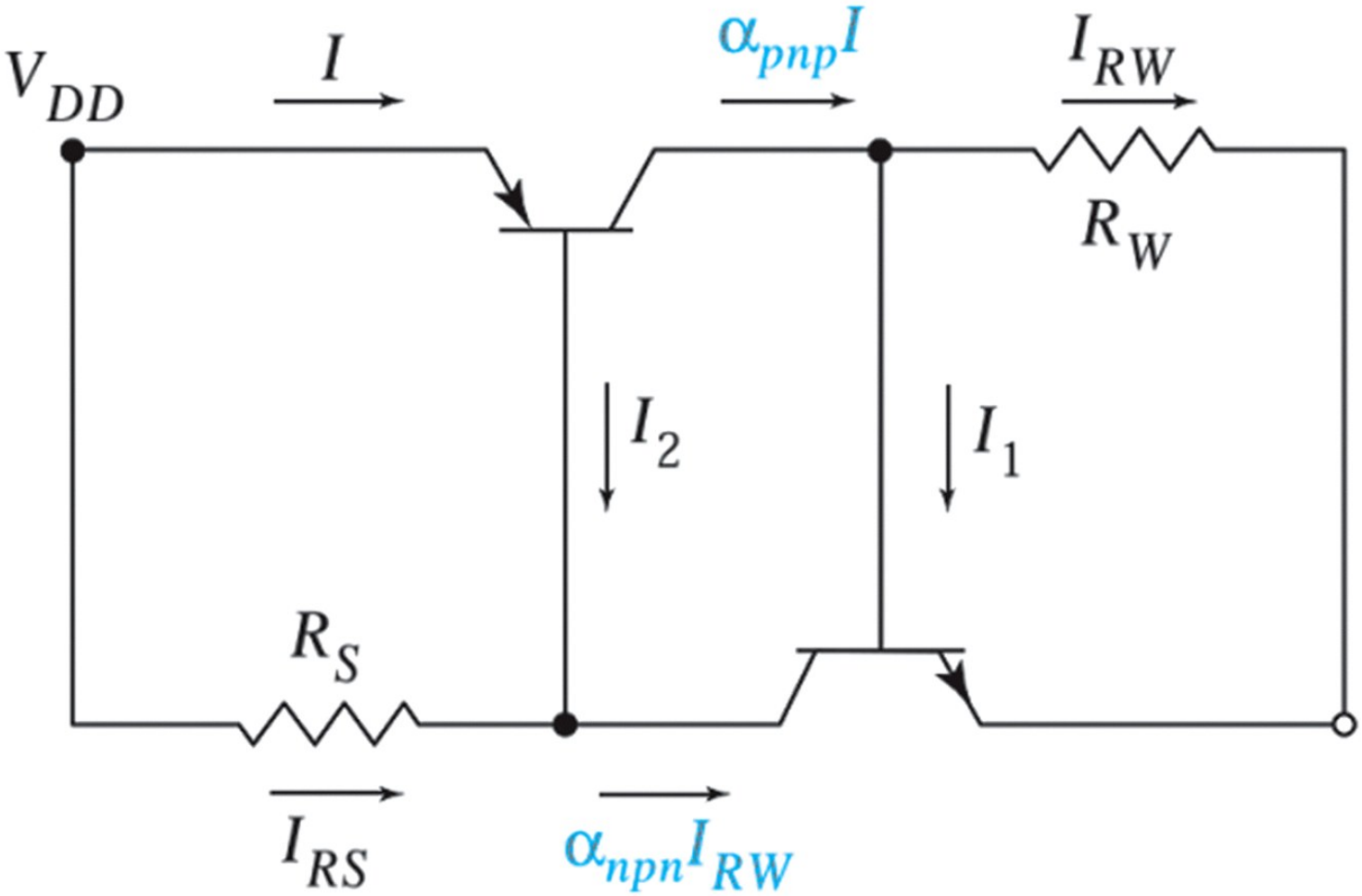


Figure 6.16

Figure 6.16.
Equivalent circuit of the *p*-well structure shown in Fig. 15.

如同PNPN結構

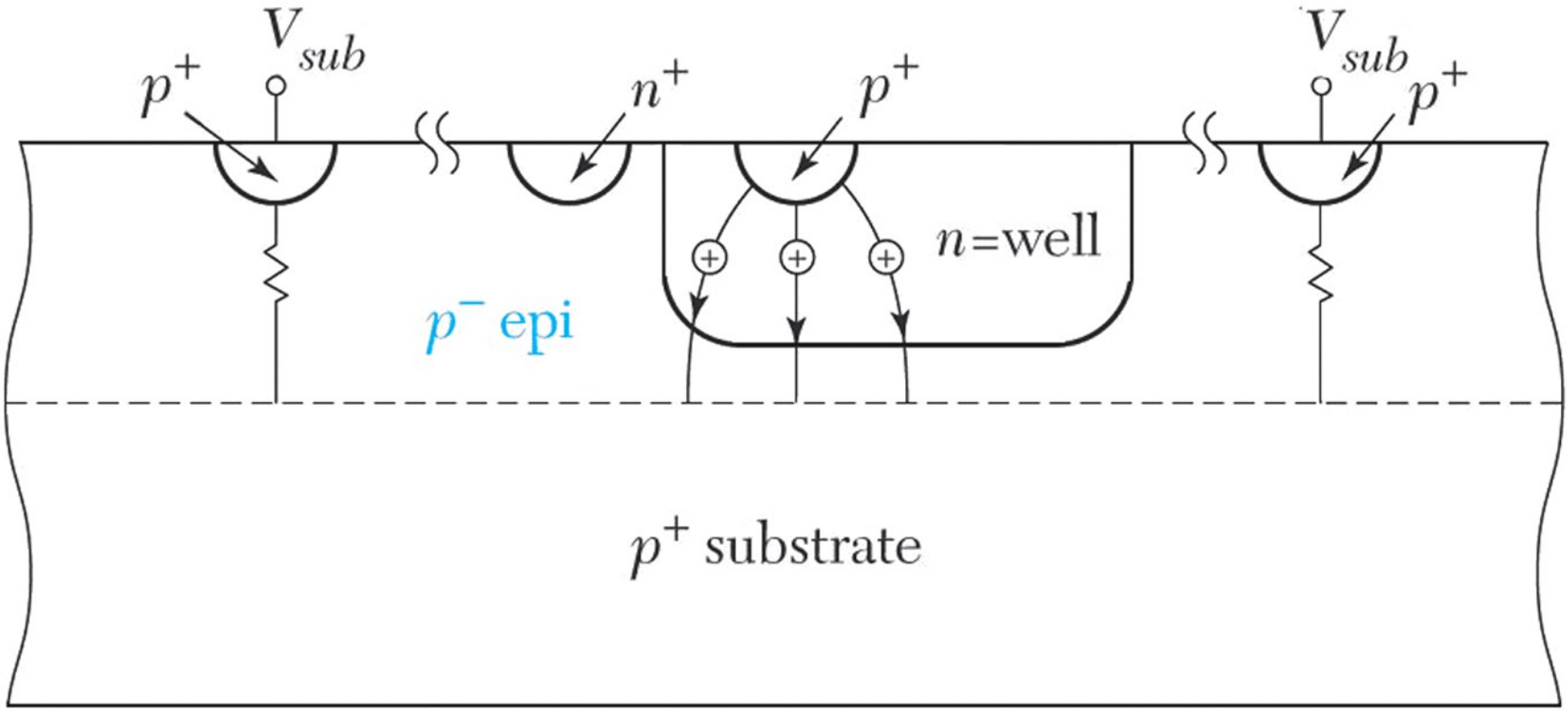


Figure 6.17

Figure 6.17.
Prevention of **latch-up** with a heavily doped substrate.[14]

Heavily doped substrate, Rw ↓,
Q2 不易on

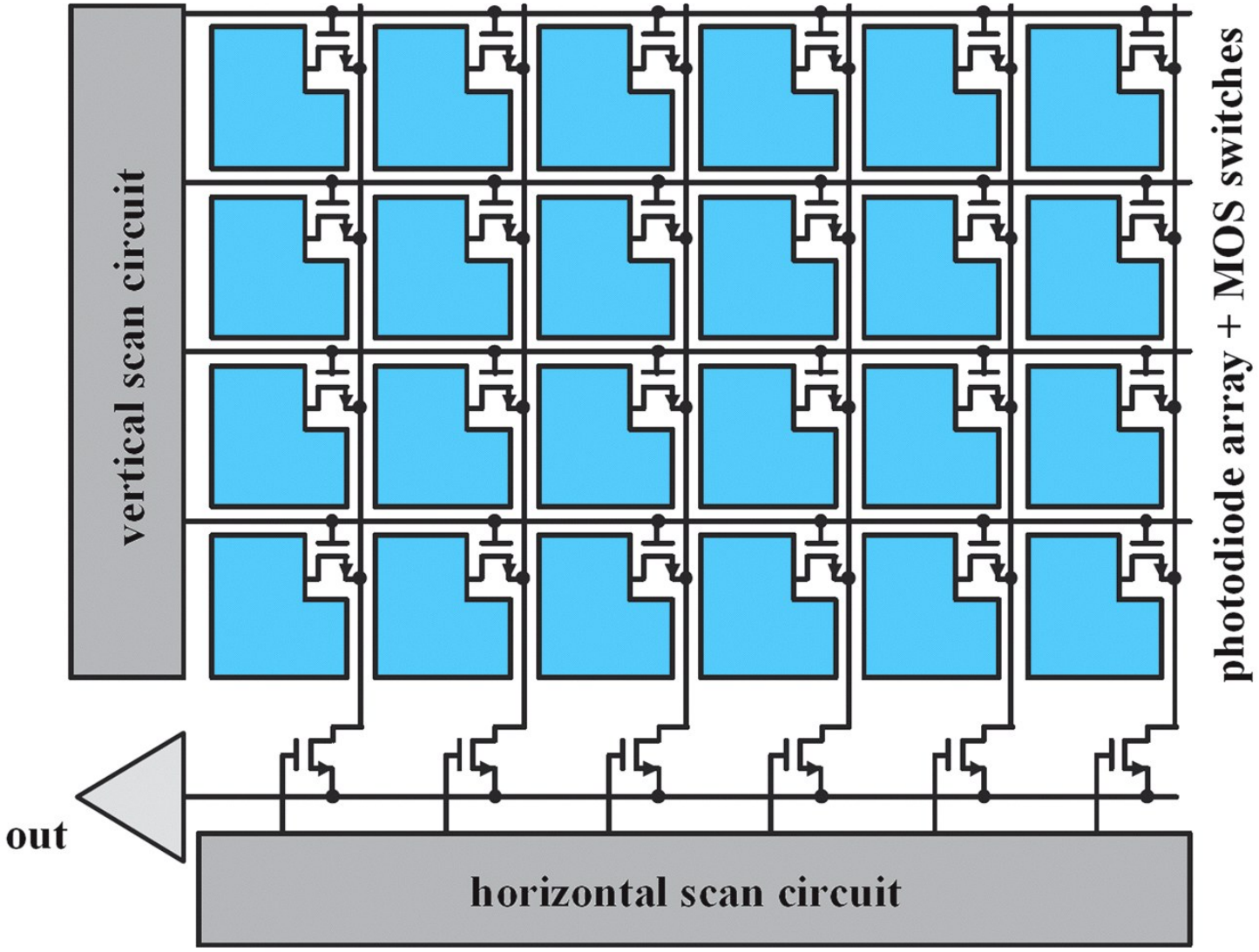


Figure 6.18

2D CMOS image sensor

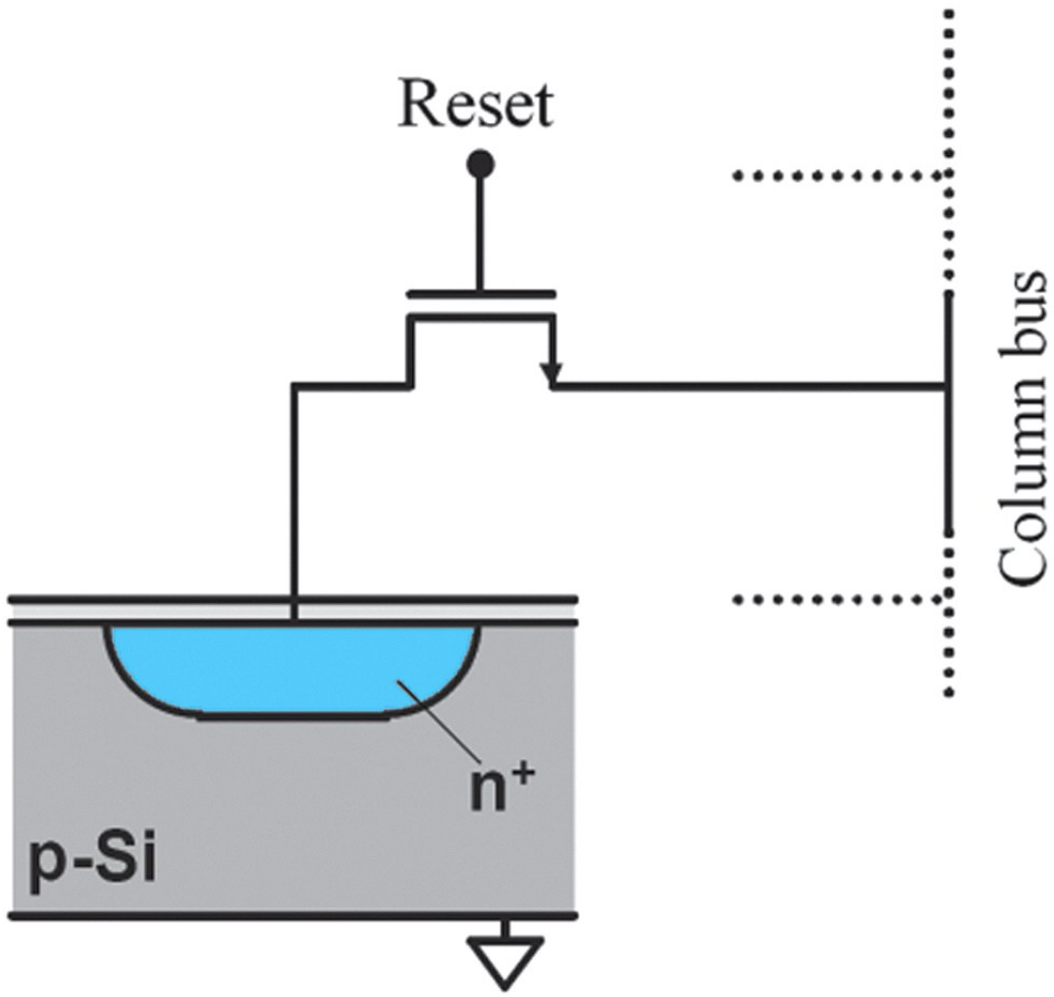


Figure 6.19a

Passive CMOS pixel with a single in-pixel transistor

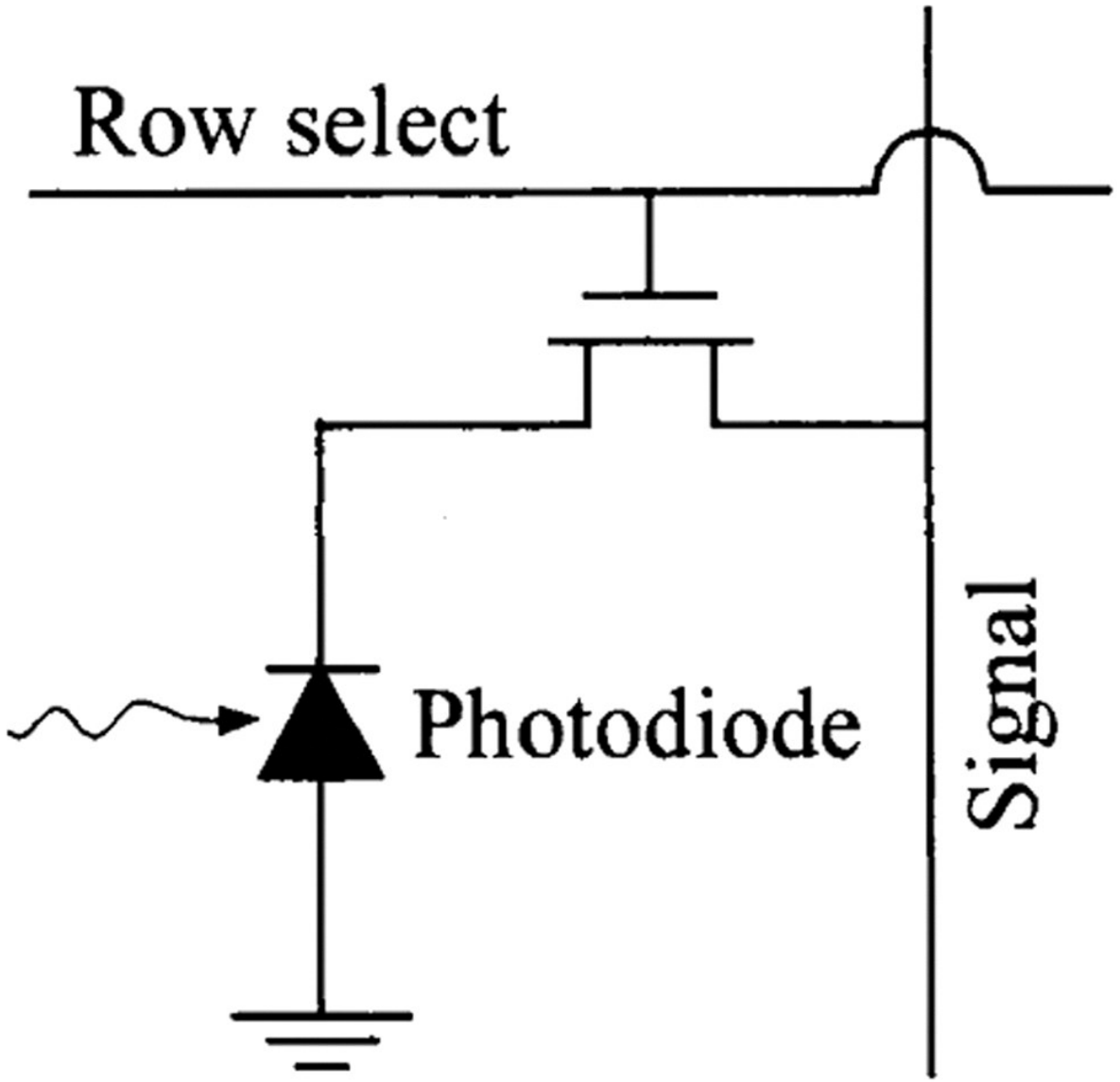


Figure 6.19b

Passive pixel sensor CMOS image sensor

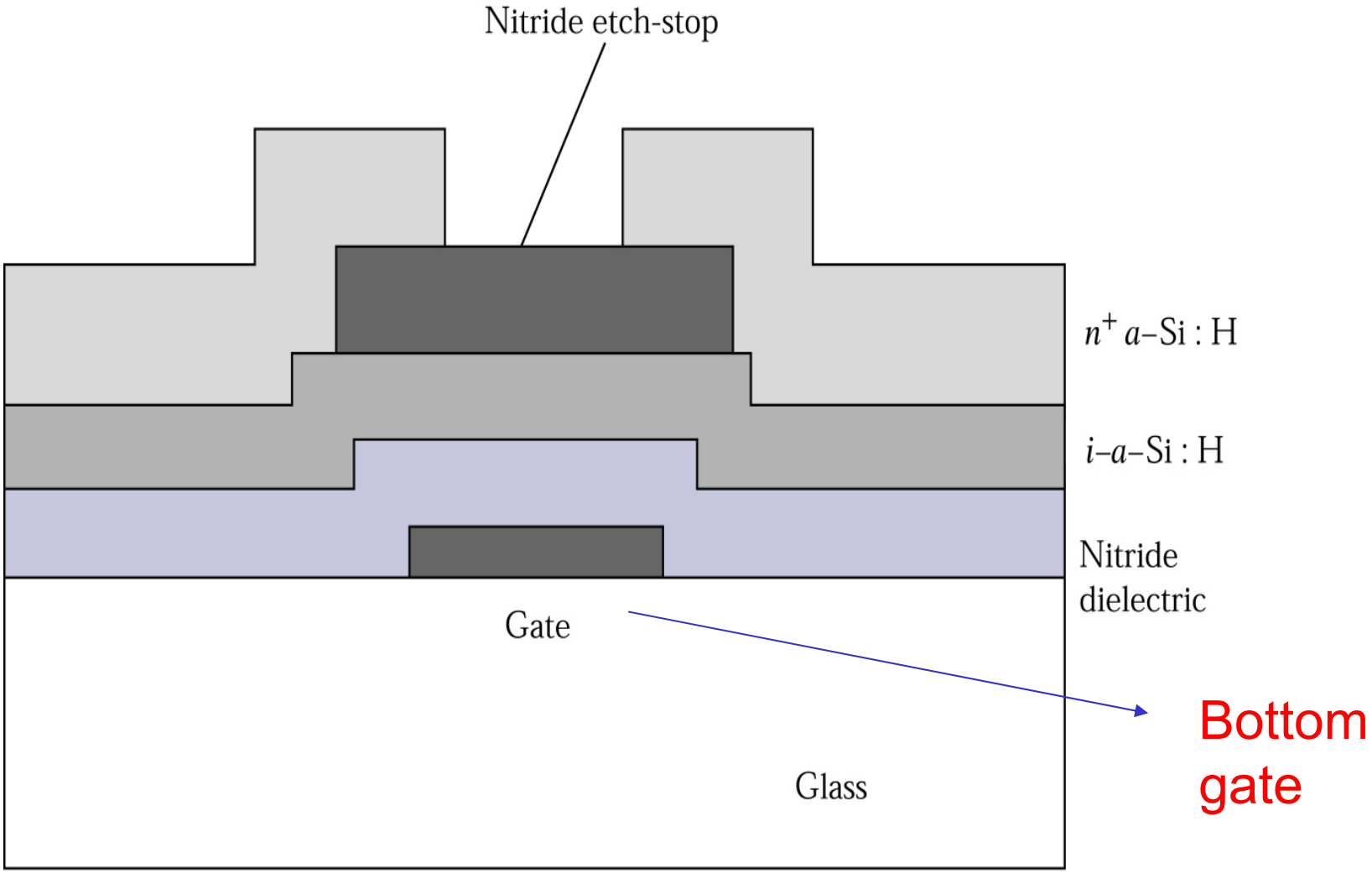
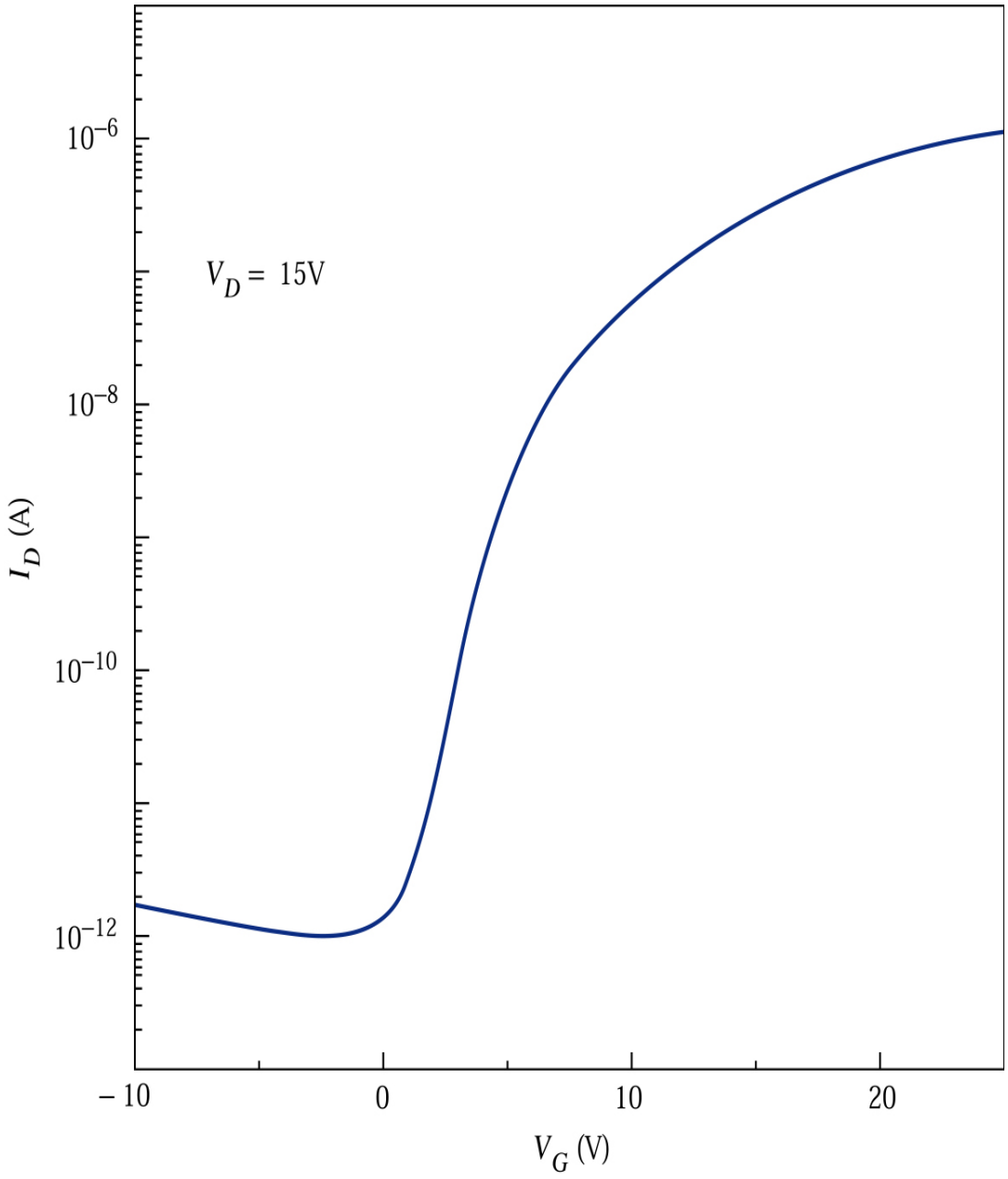


Figure 6.20. A typical **a-Si:H** thin film transistor (TFT) structure.

Figure 6.21.
Subthreshold characteristics of an a-SI:H TFT (*L*/*Z* – 10/60 μm/μm). The field-effect carrier mobility is 0.23 cm^2/ V-s.



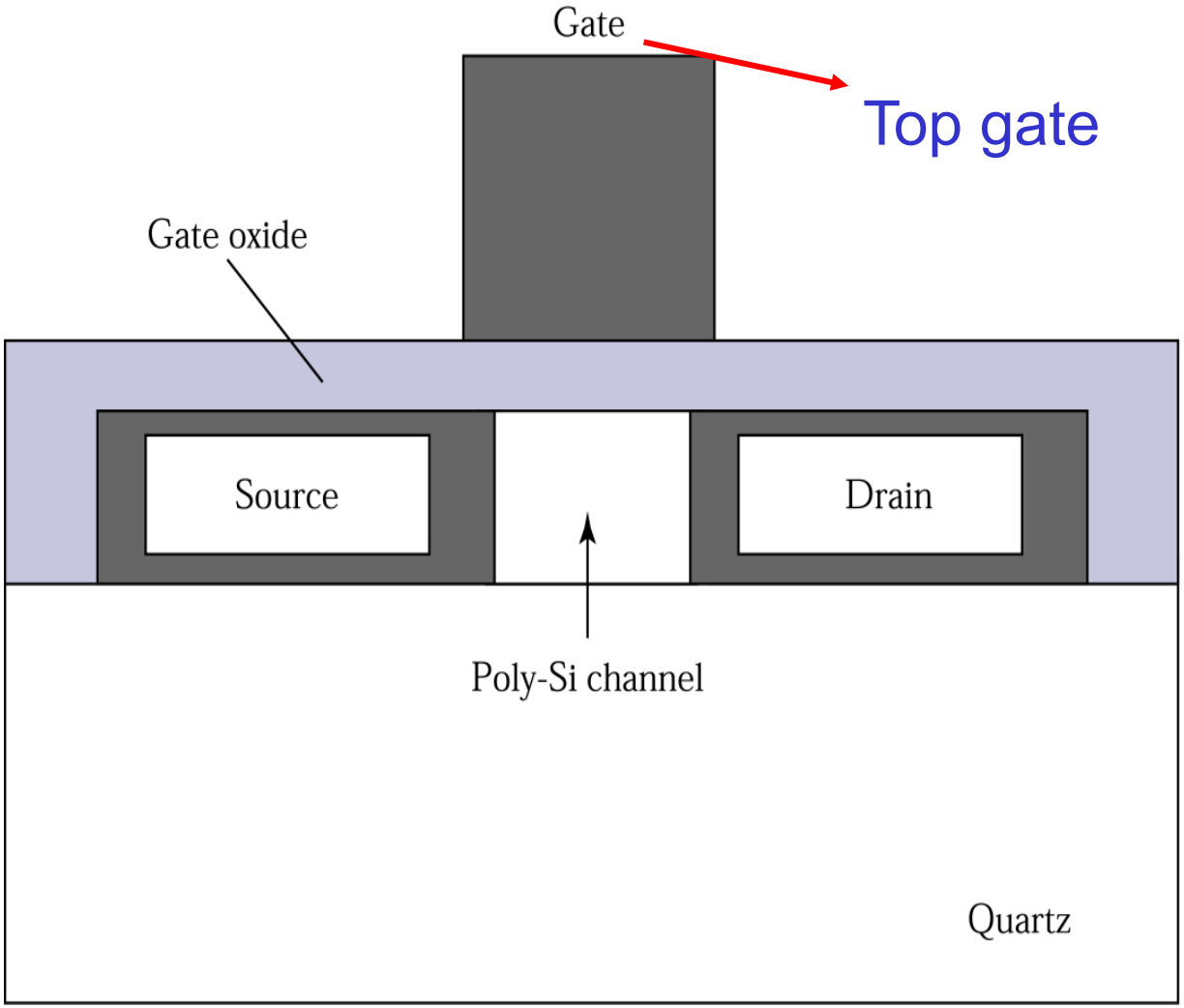
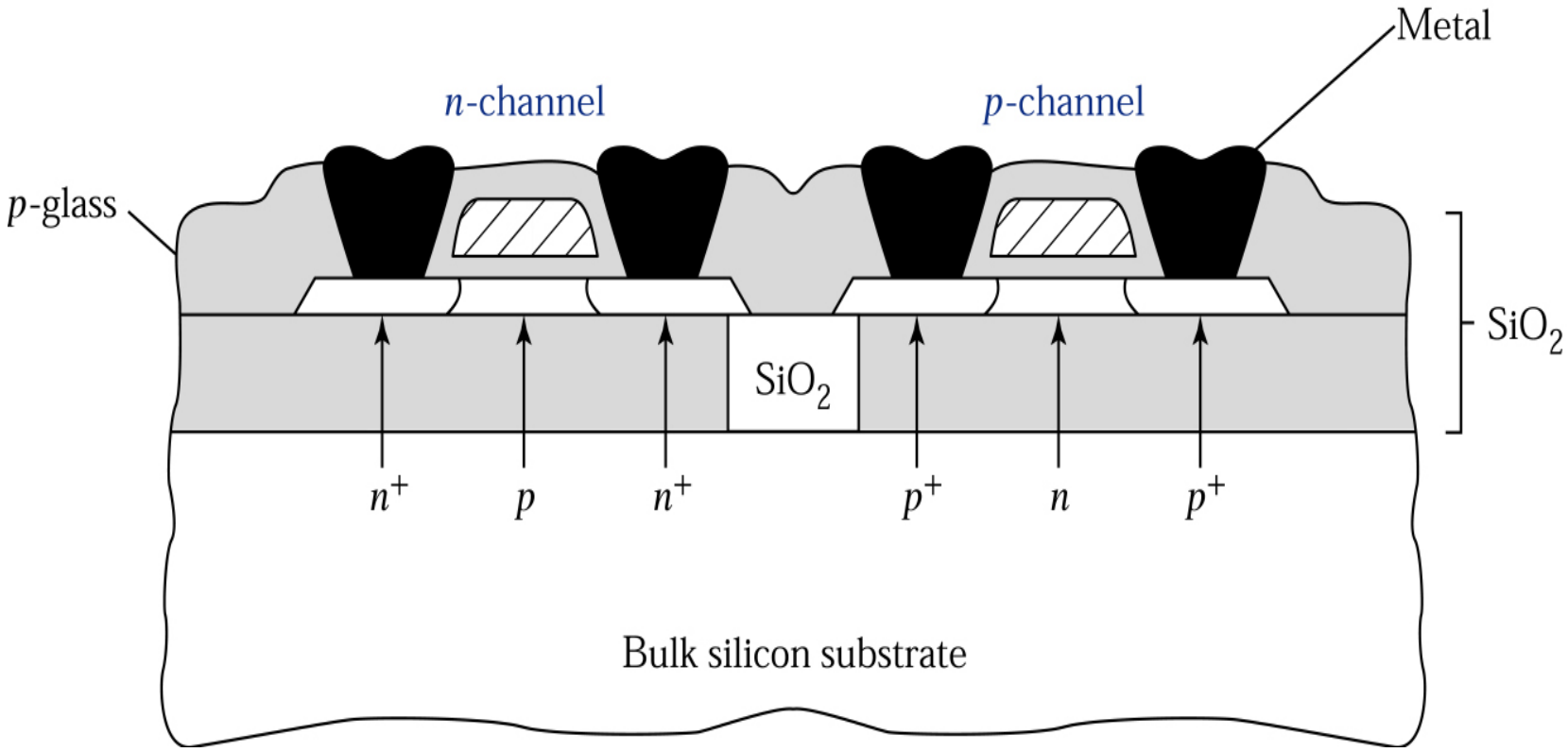


Figure 6.22. A **polysilicon** TFT structure.

Poly-Si, >600C, quartz, expensive, laser annealing



For high freq. application, but SOI wafer is expensive

Figure 6.23. Cross section of the silicon-on-insulator (SOI).

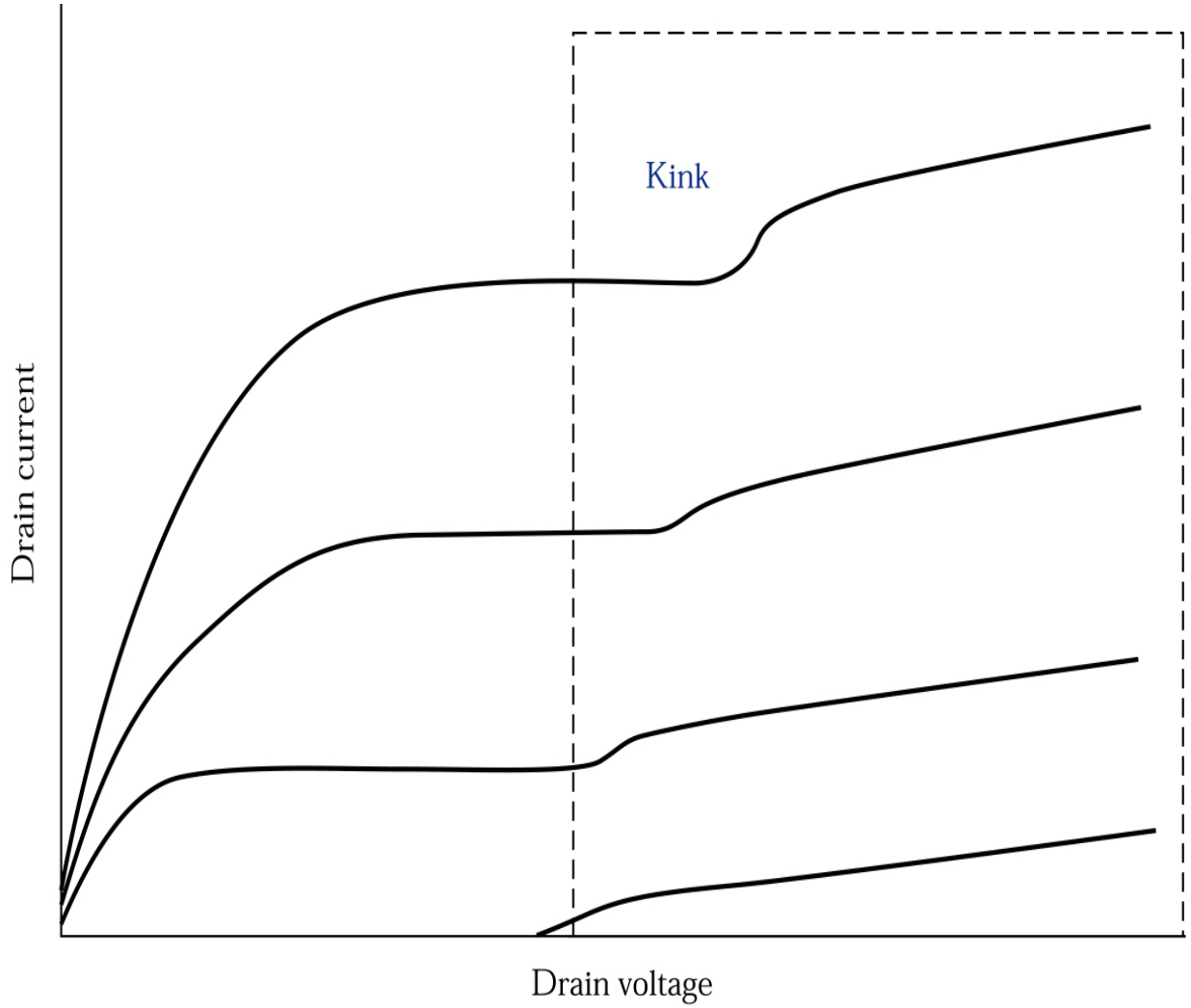


Figure 6.24. The **kink effect** in the output characteristics of an *n*-channel SOI MOSFET.[15]

Hot hole stored in sub, Vb上升, Vt 减少

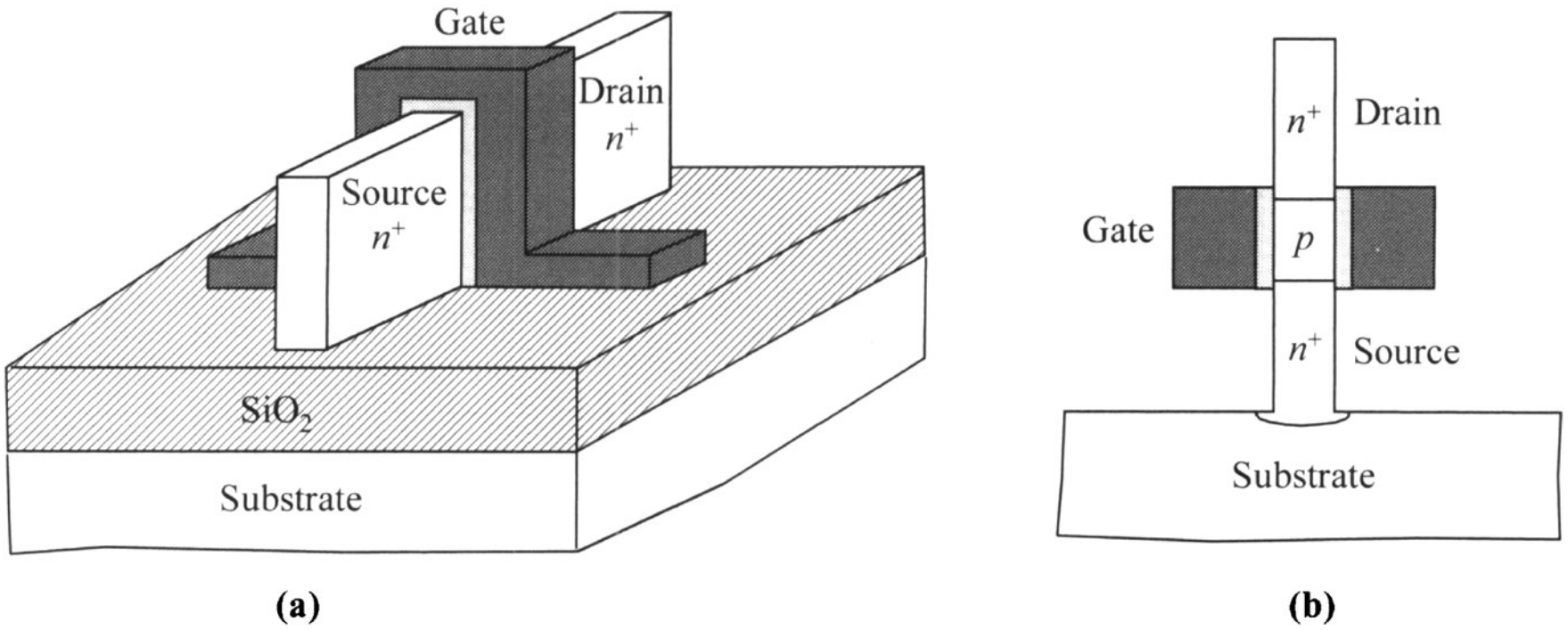


Figure 6.25

3D MOSFET, (a) horizontal (b) vertical structures

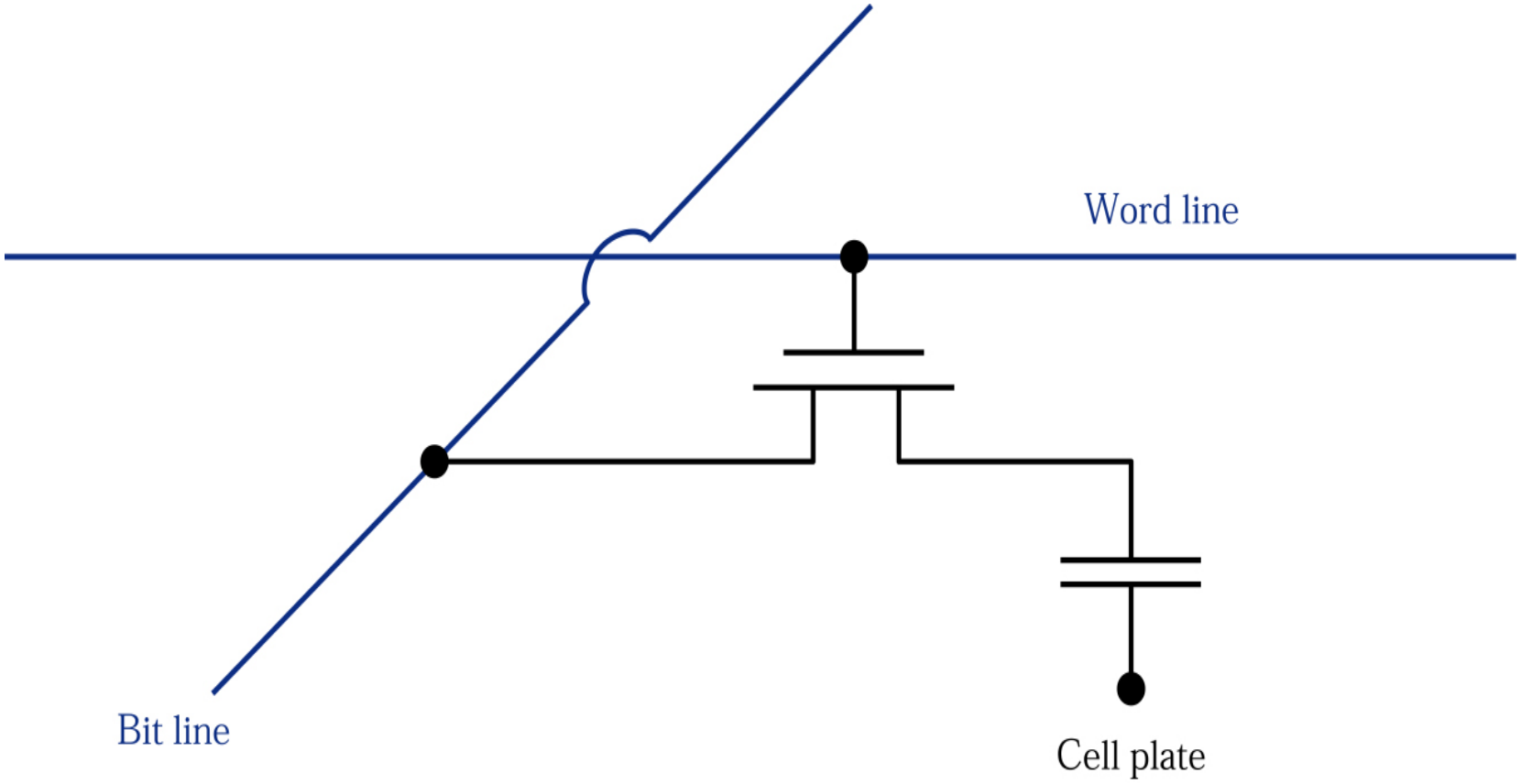


Figure 6.26. Basic configuration of a dynamic random access memory (DRAM) cell.[16]

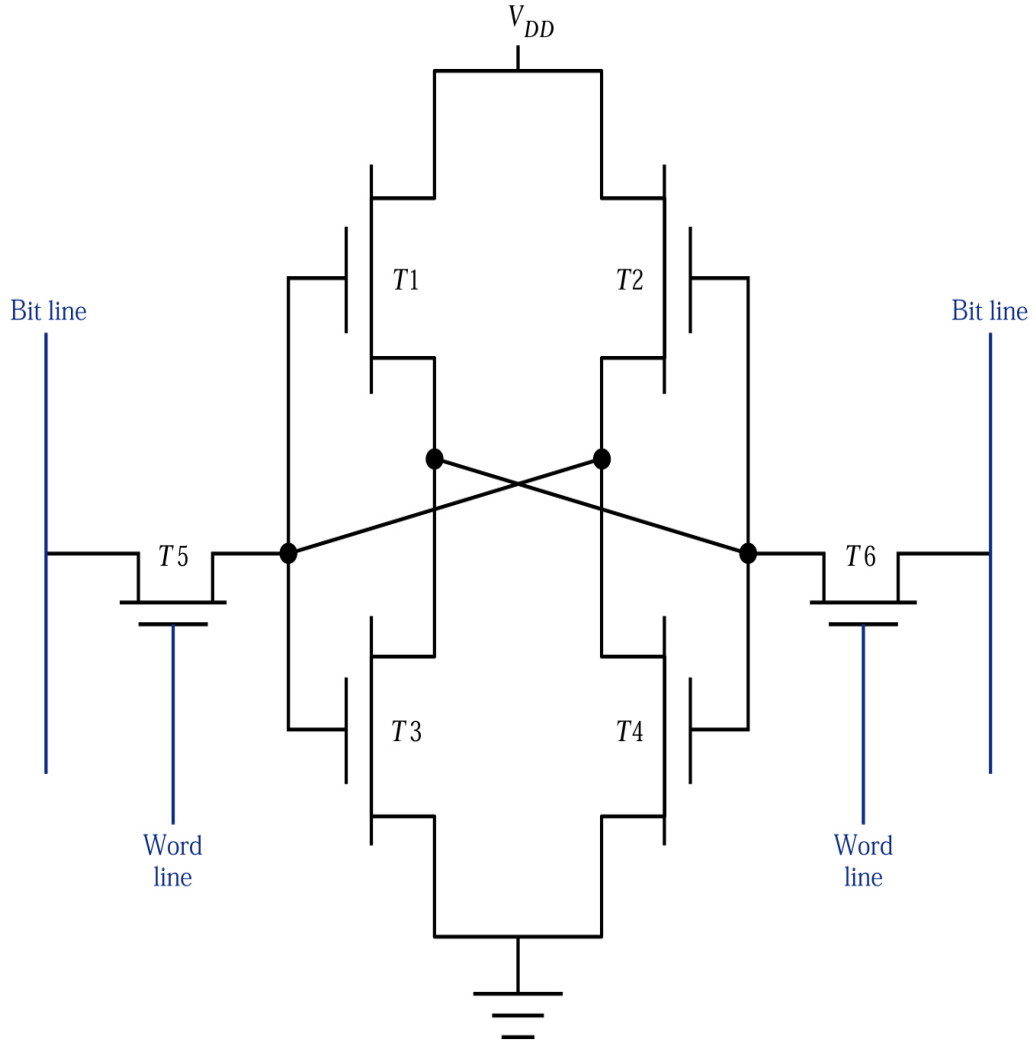


Figure 6.27. Configuration of a CMOS SRAM cell. T1 and T2 are load transistors (*p*-channel). T3 and T4 are drive transistors (*n*-channel). T5 and T6 are access transistors (*n*-channel).

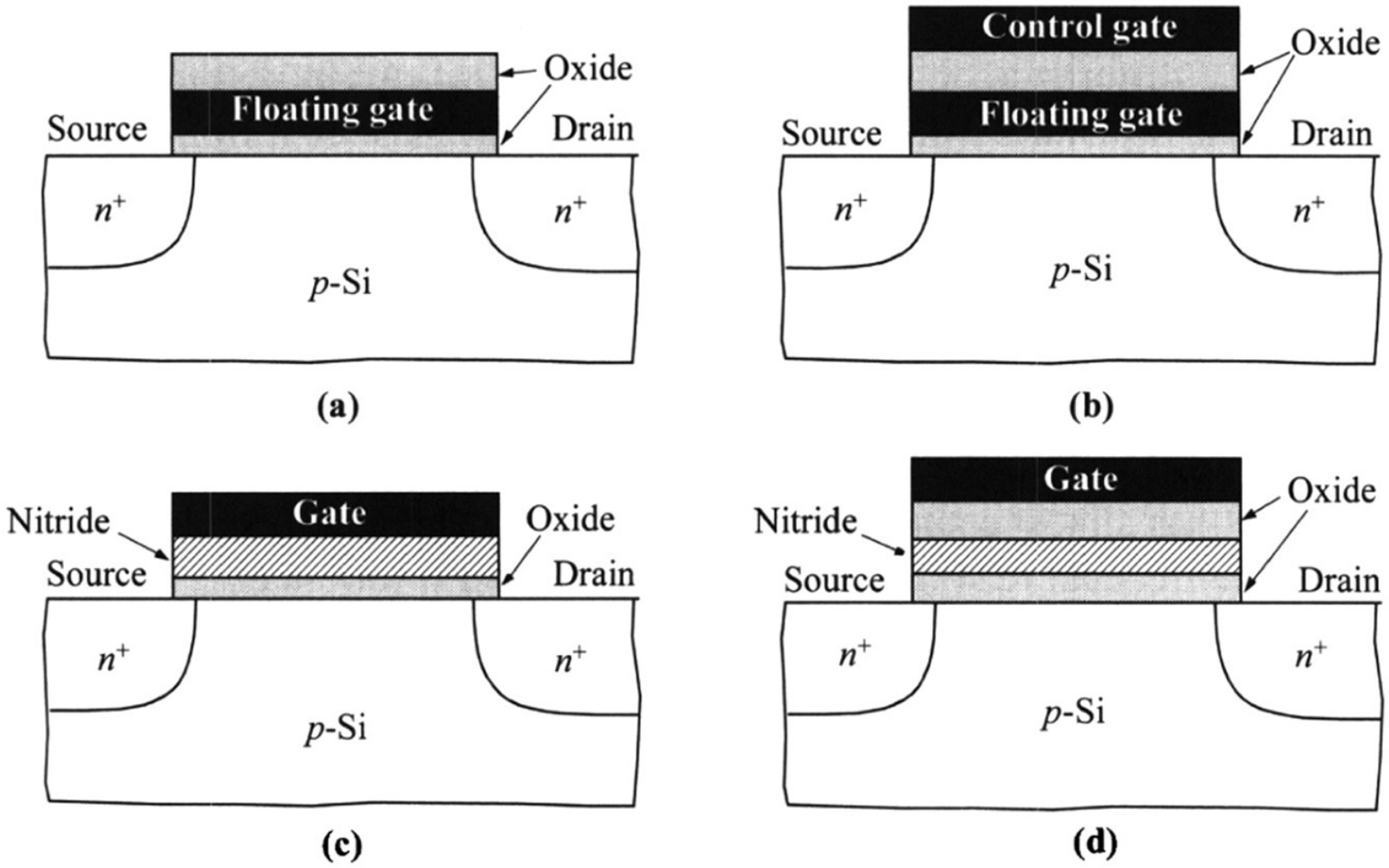


Figure 6.28

Floating gate: (a)FAMOS (b) stacked gate

Charge-trapping : (c) MNOS (d) SONOS

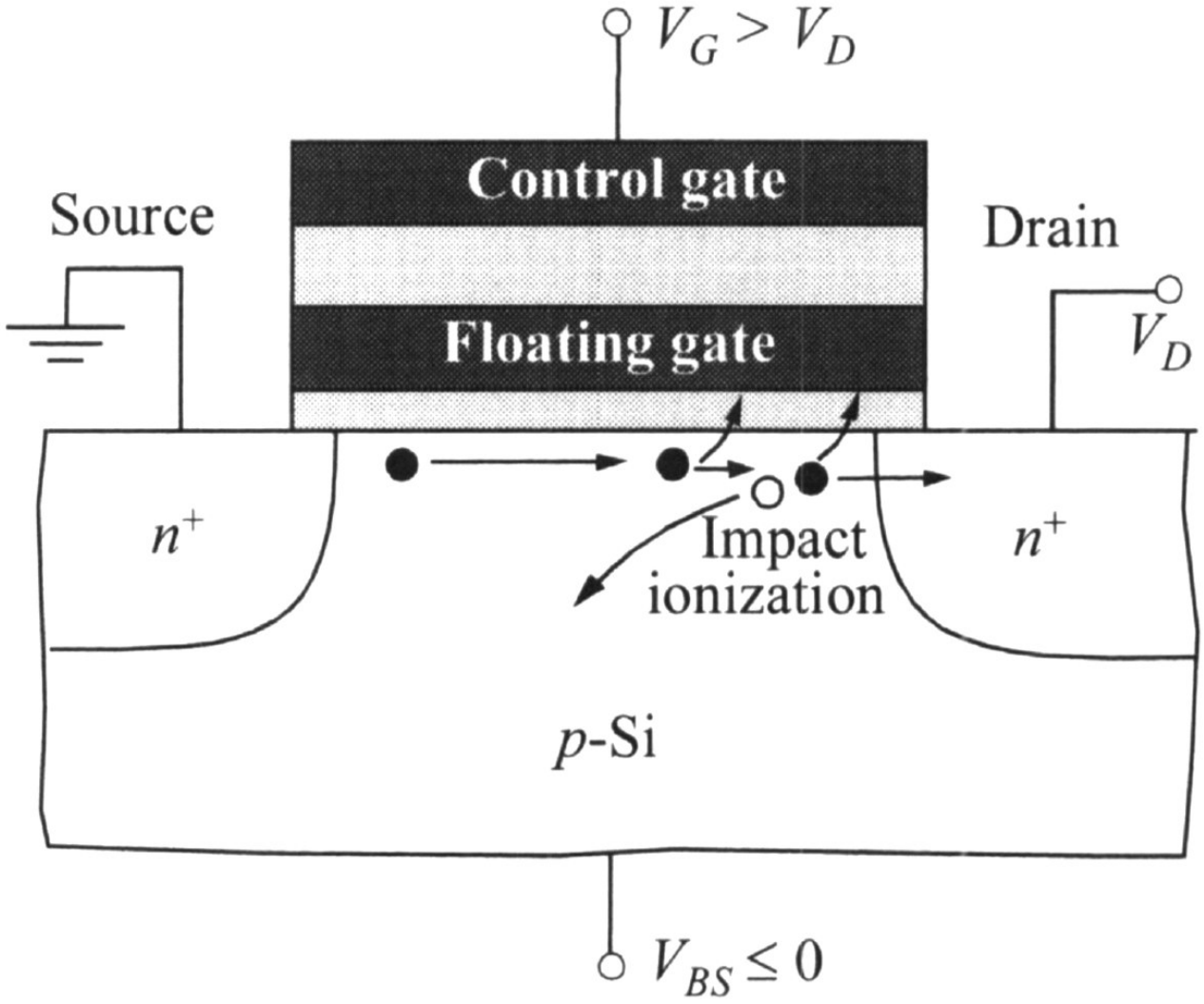


Figure 6.29a

Illustration of hot electron injection in an n-channel, floating-gate nonvolatile memory.

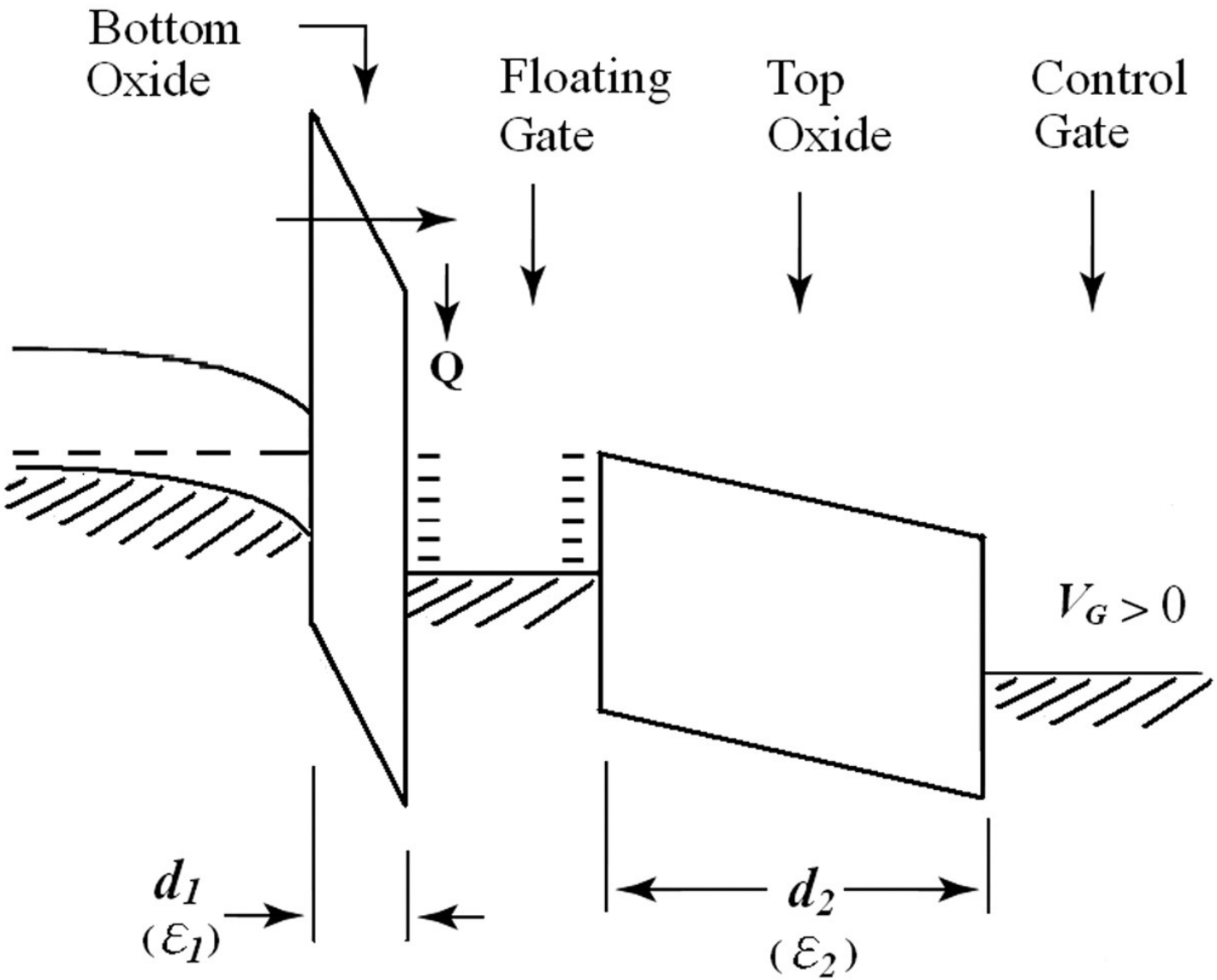


Figure 6.29b

Band diagram of programming condition

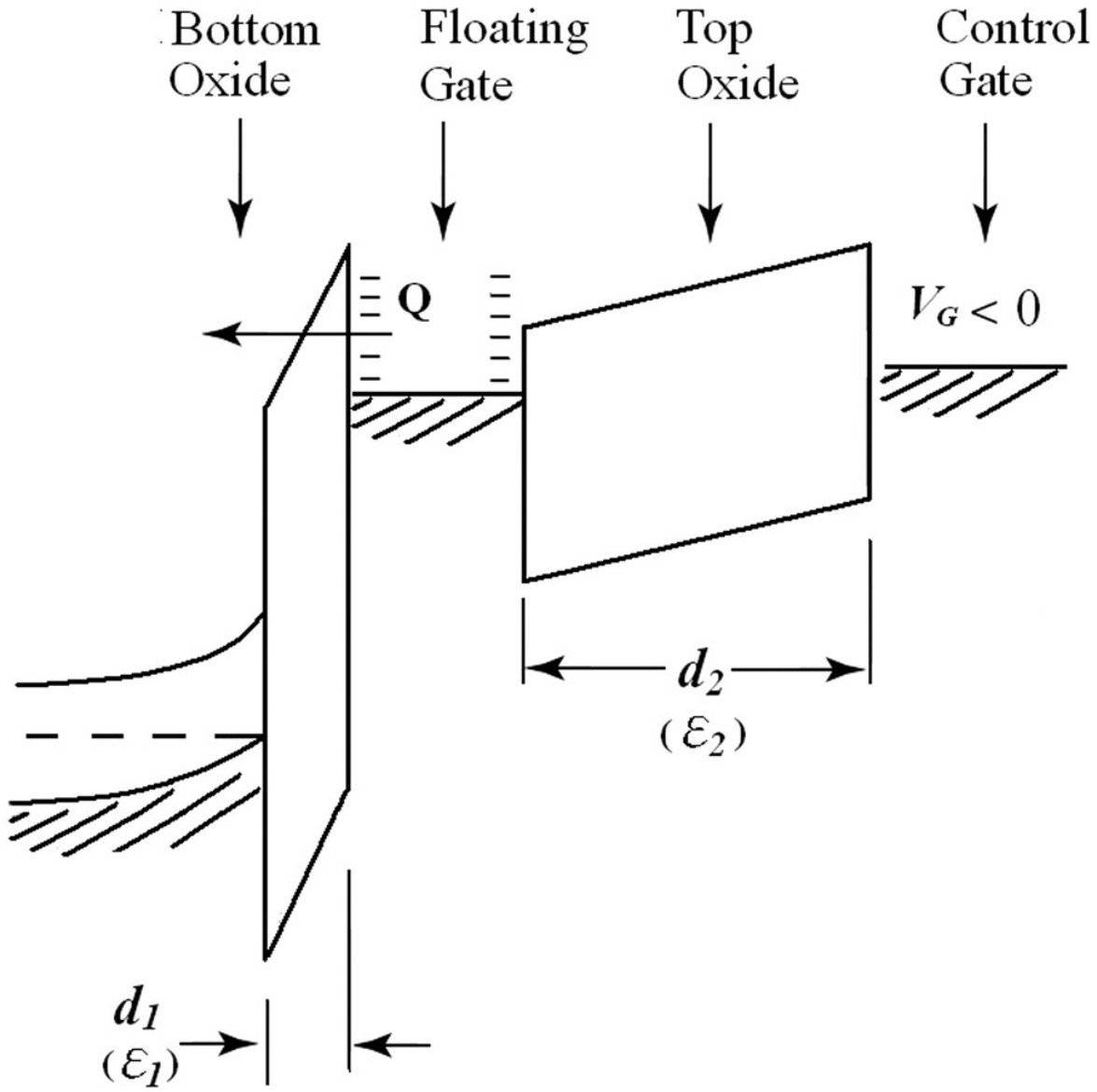


Figure 6.29c

Band diagram of erasing condition

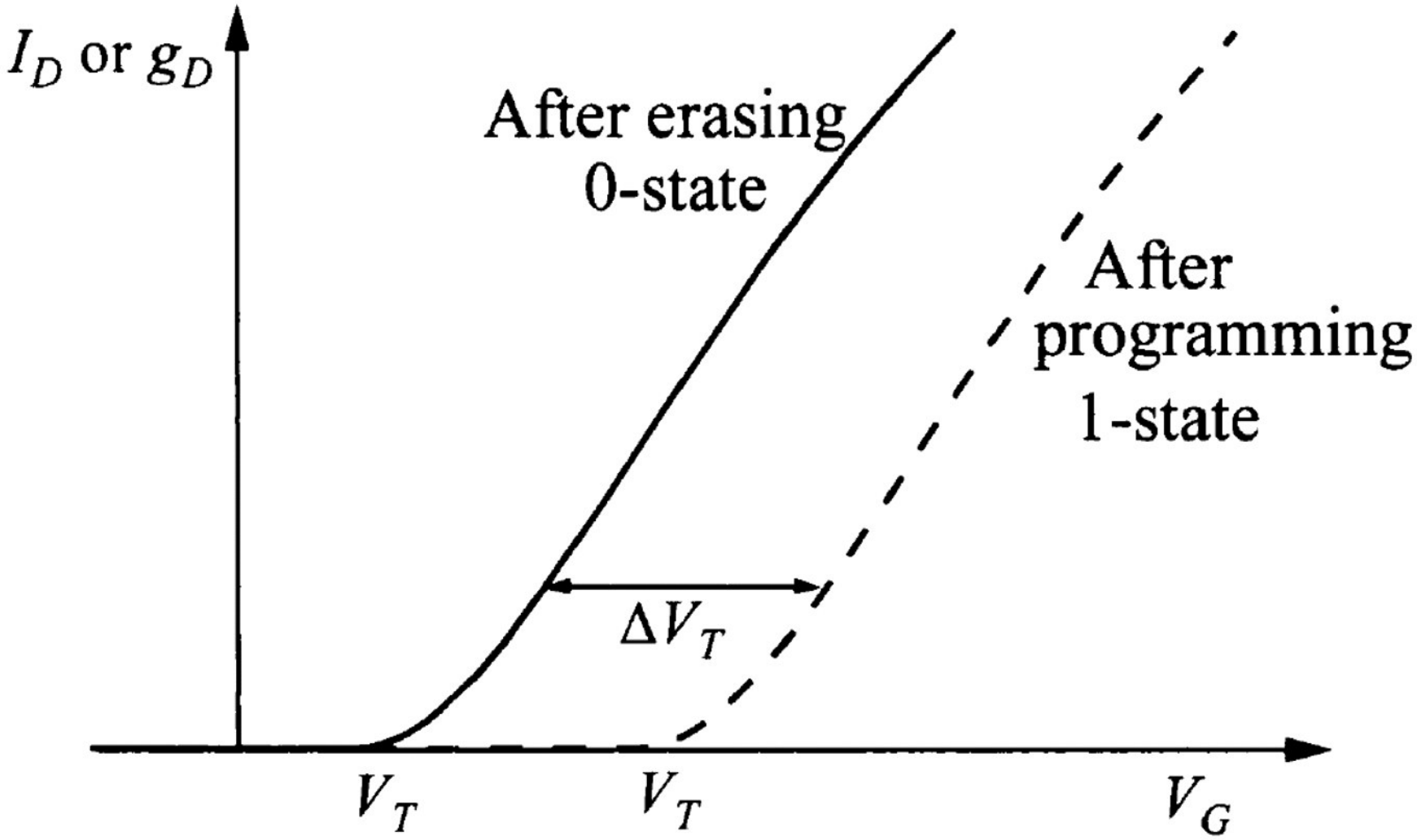


Figure 6.30

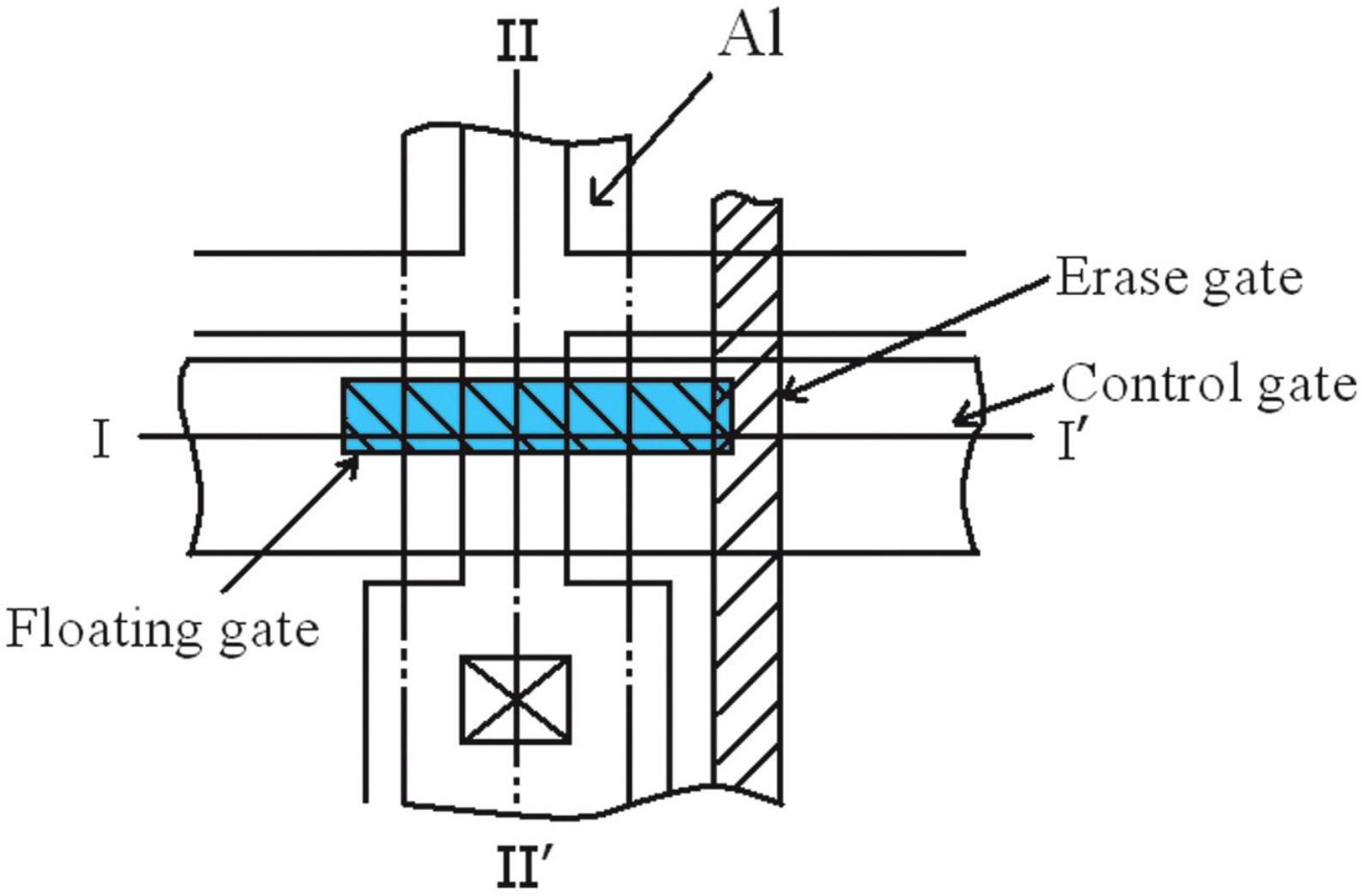


Figure 6.31a

Top view of flash memory device

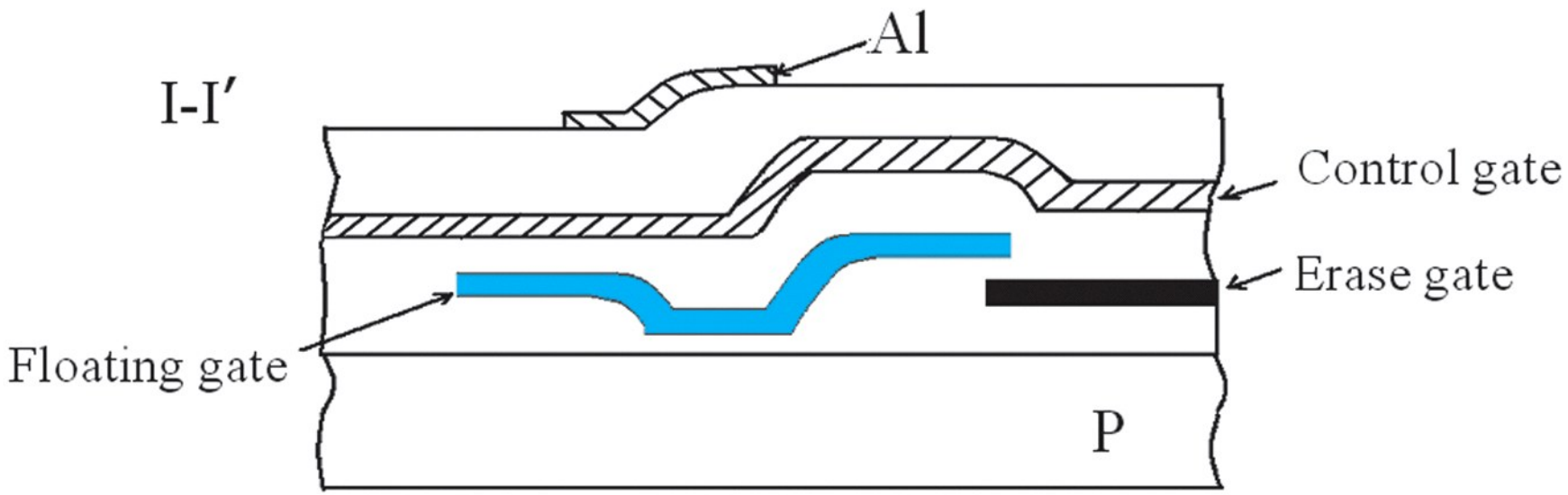


Figure 6.31b

Cross-section along I-I’ line

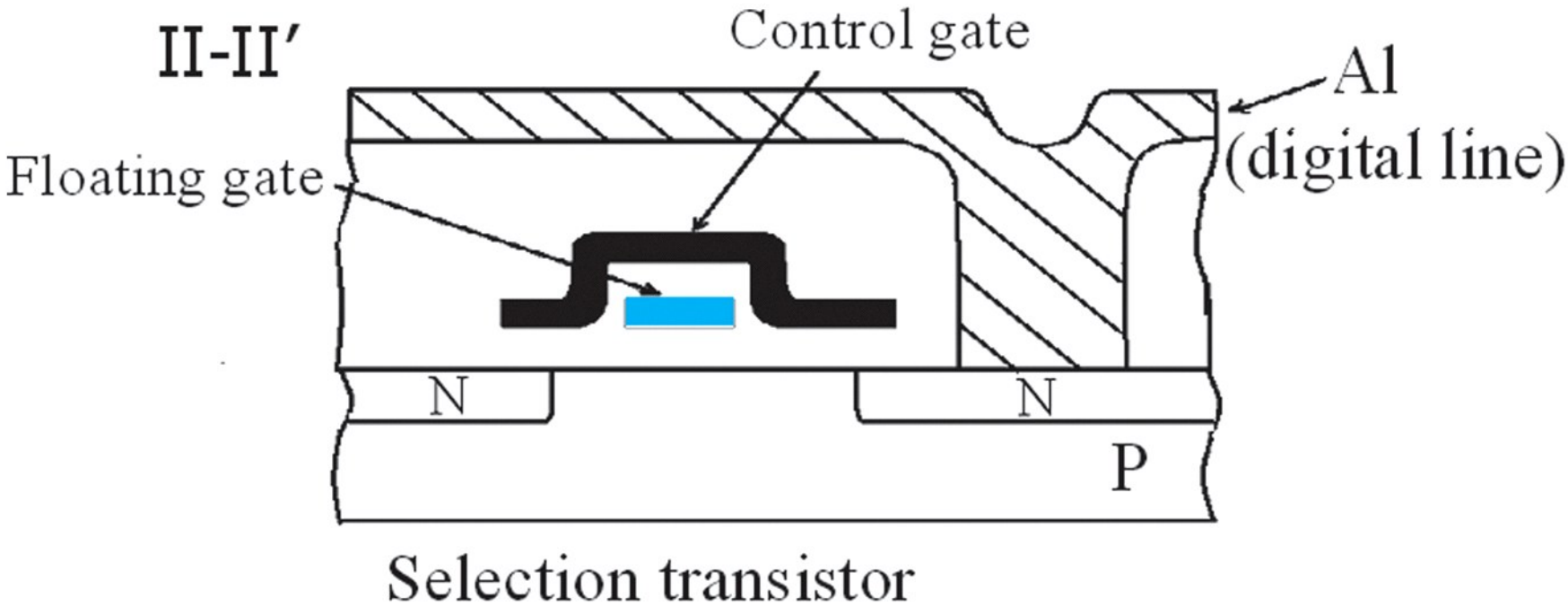


Figure 6.31c

Cross-section along II-II' line

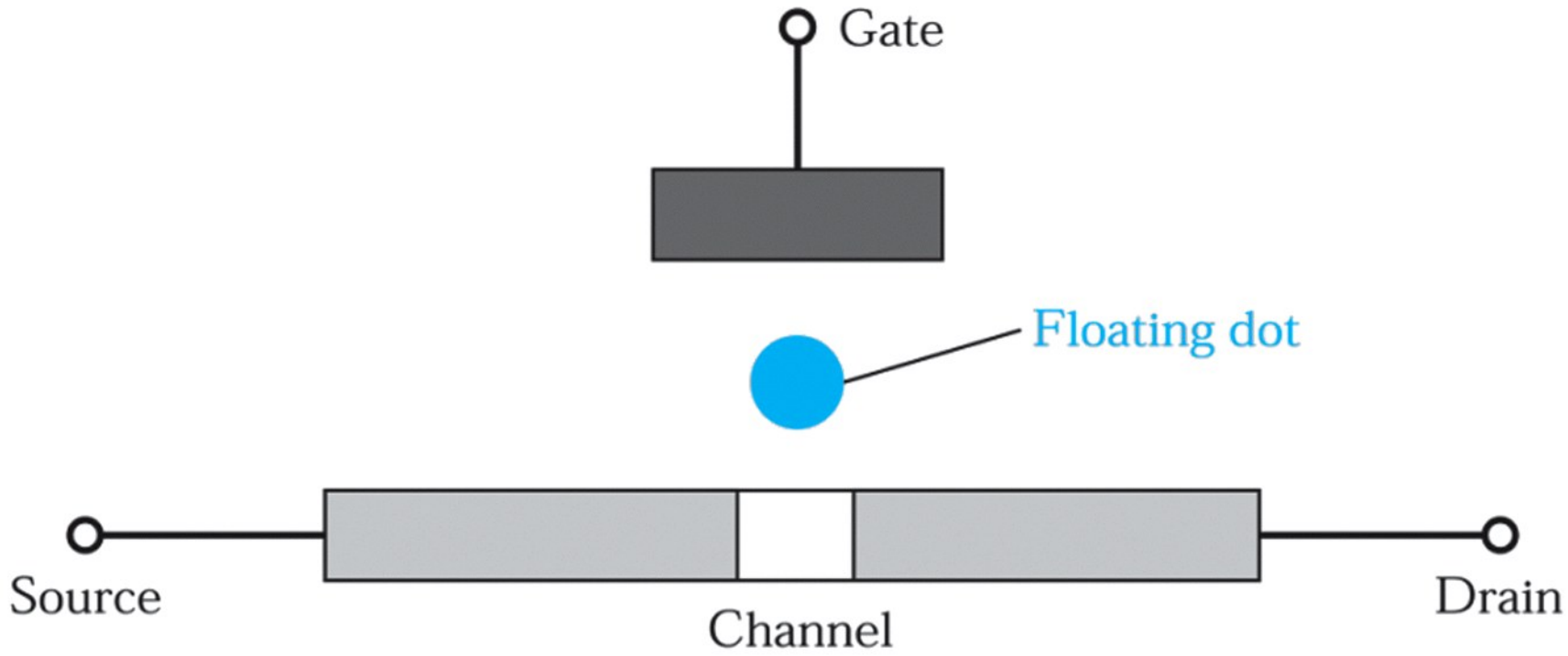


Figure 6.32

Single-electron memory cell.

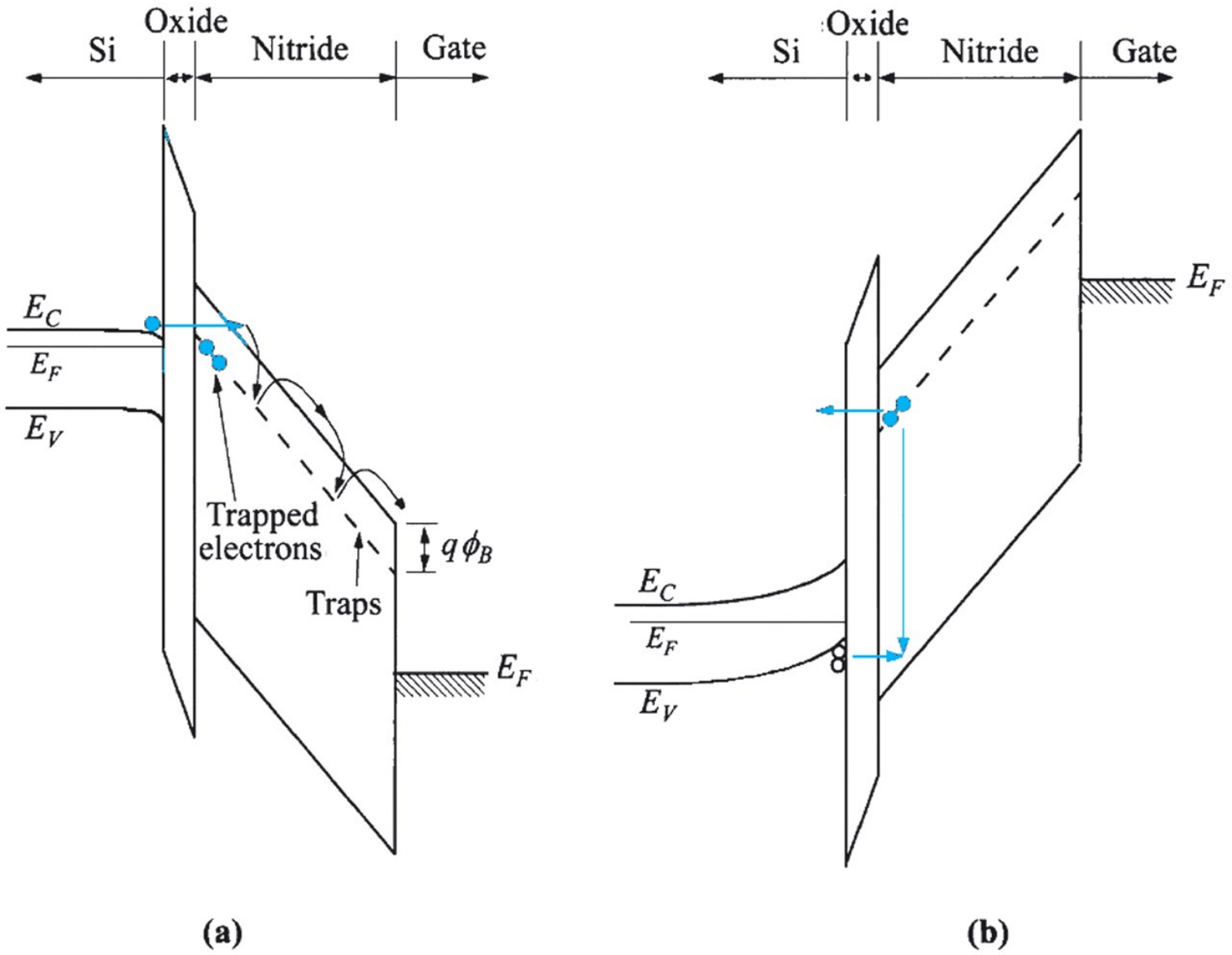


Figure 6.33

MNOS, (a)programming (b)erasing

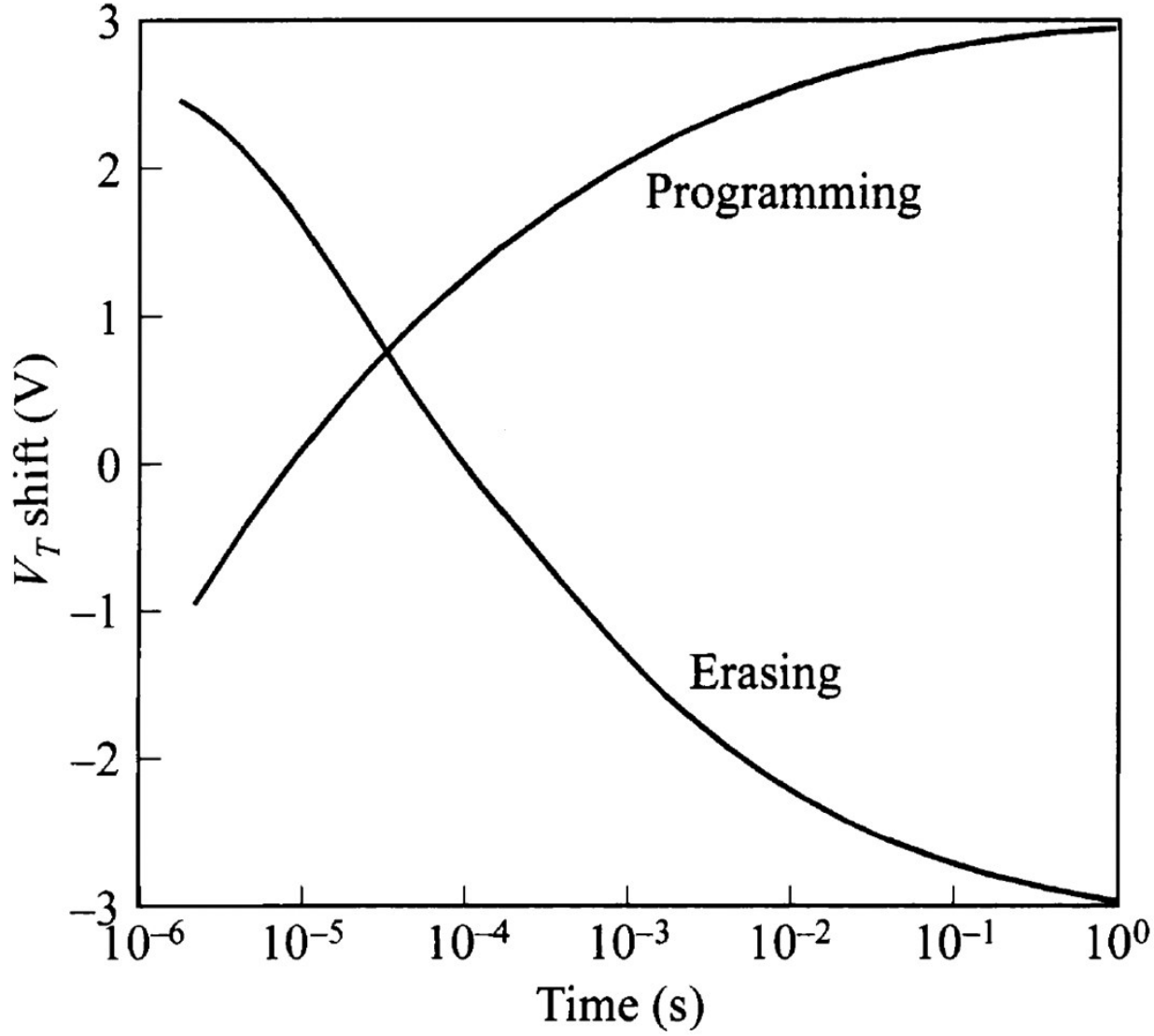


Figure 6.34

Programming and erasing rates for MNOS

Figure 6.35.
(*a*) V-shaped MOS (VMOS), (*b*) U-shaped MOS (UMOS), and (*c*) double-diffused MOS (DMOS) power device structures.[19]

Vd很大時, n^- depletion, 耐高壓

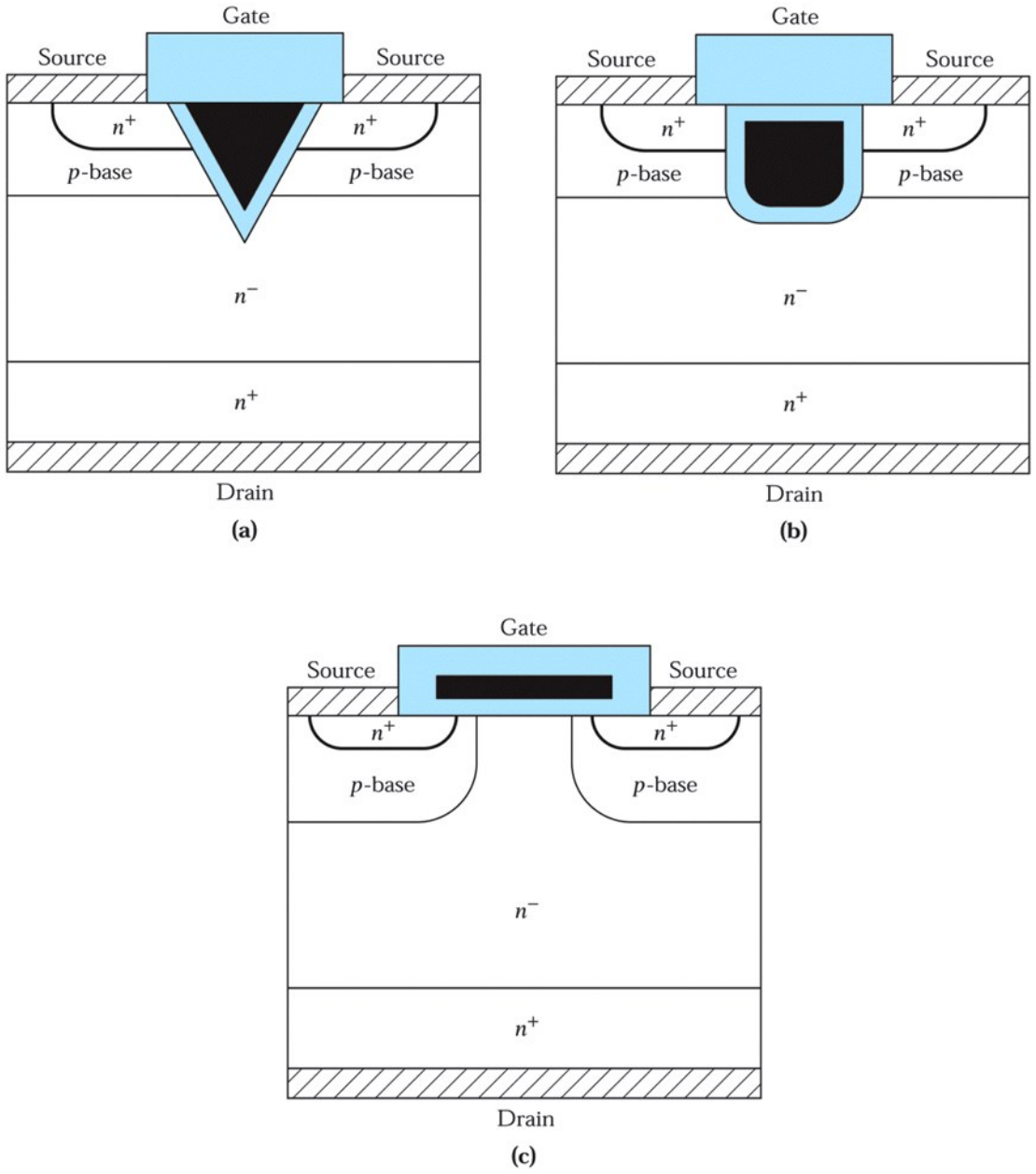


Figure 6.35

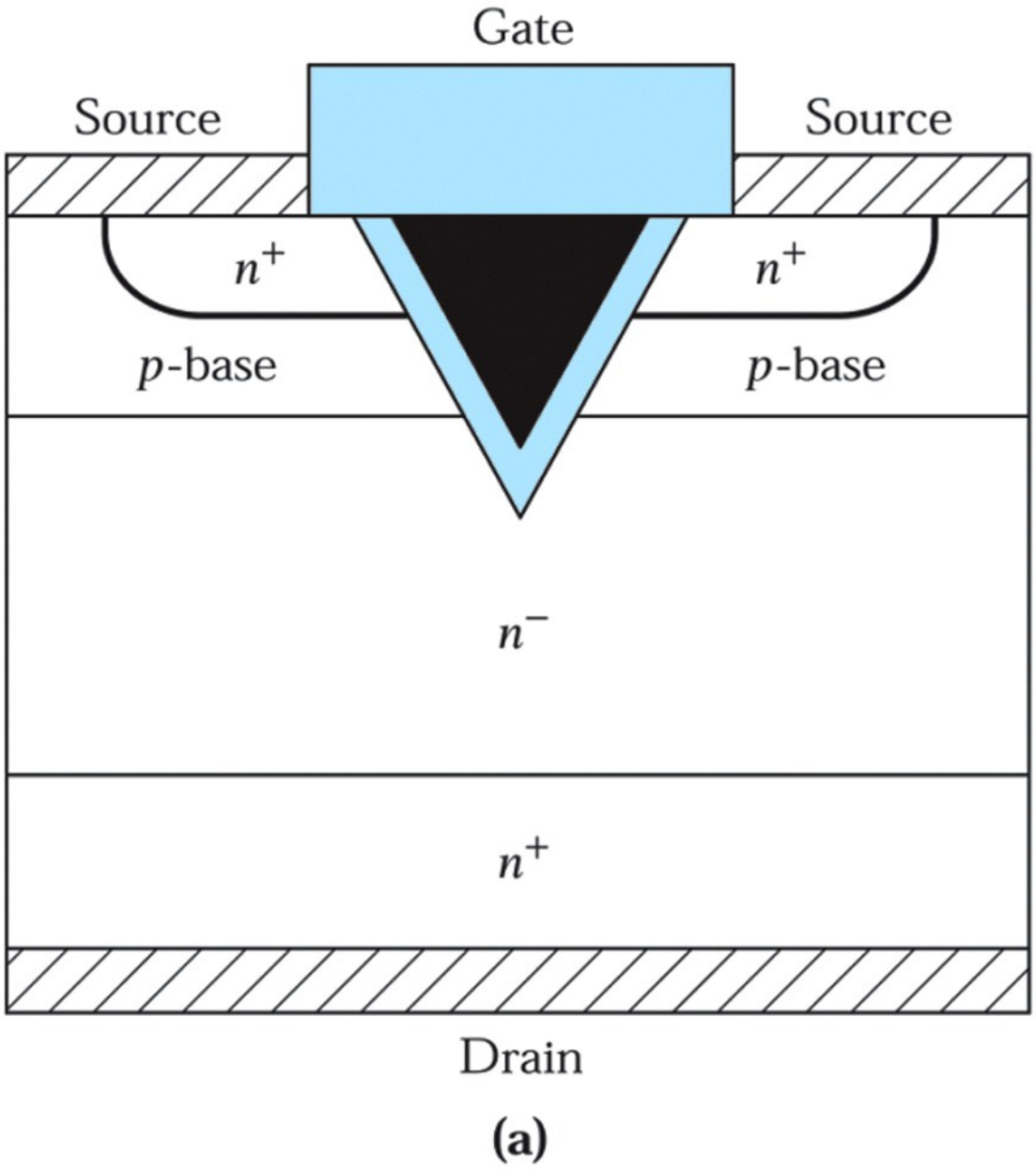


Figure 6.35a

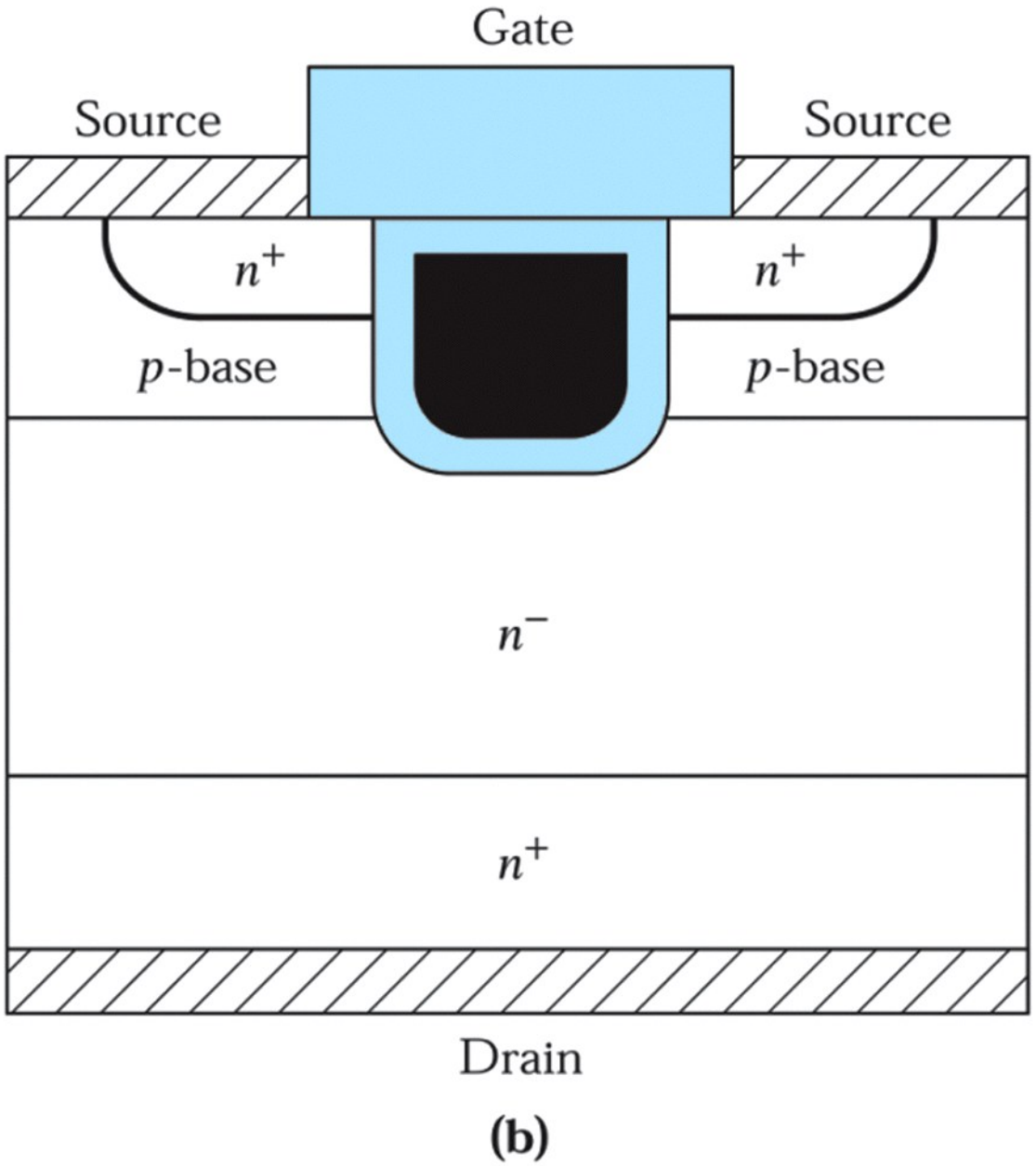


Figure 6.35b

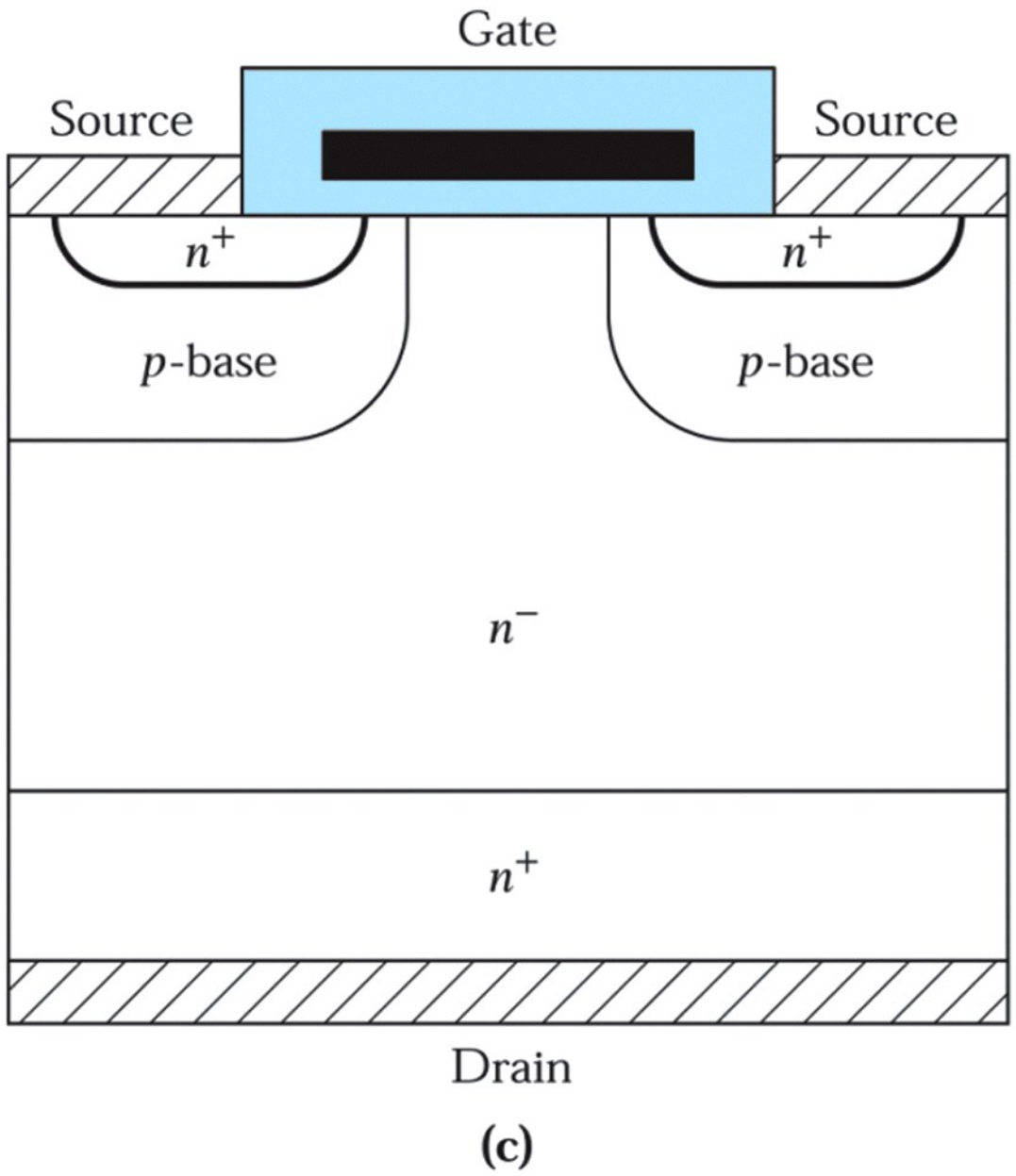


Figure 6.35c