Semiconductor Devices

THIRD EDITION

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Chapter 5

MOS Capacitor and MOSFET

affinity

先令其

$$q\Phi_{ms} \equiv (q\Phi_m - q\Phi_s) = q\Phi_m - [q\chi + E_g/2 + q\Psi_B] = 0 \qquad (1)$$

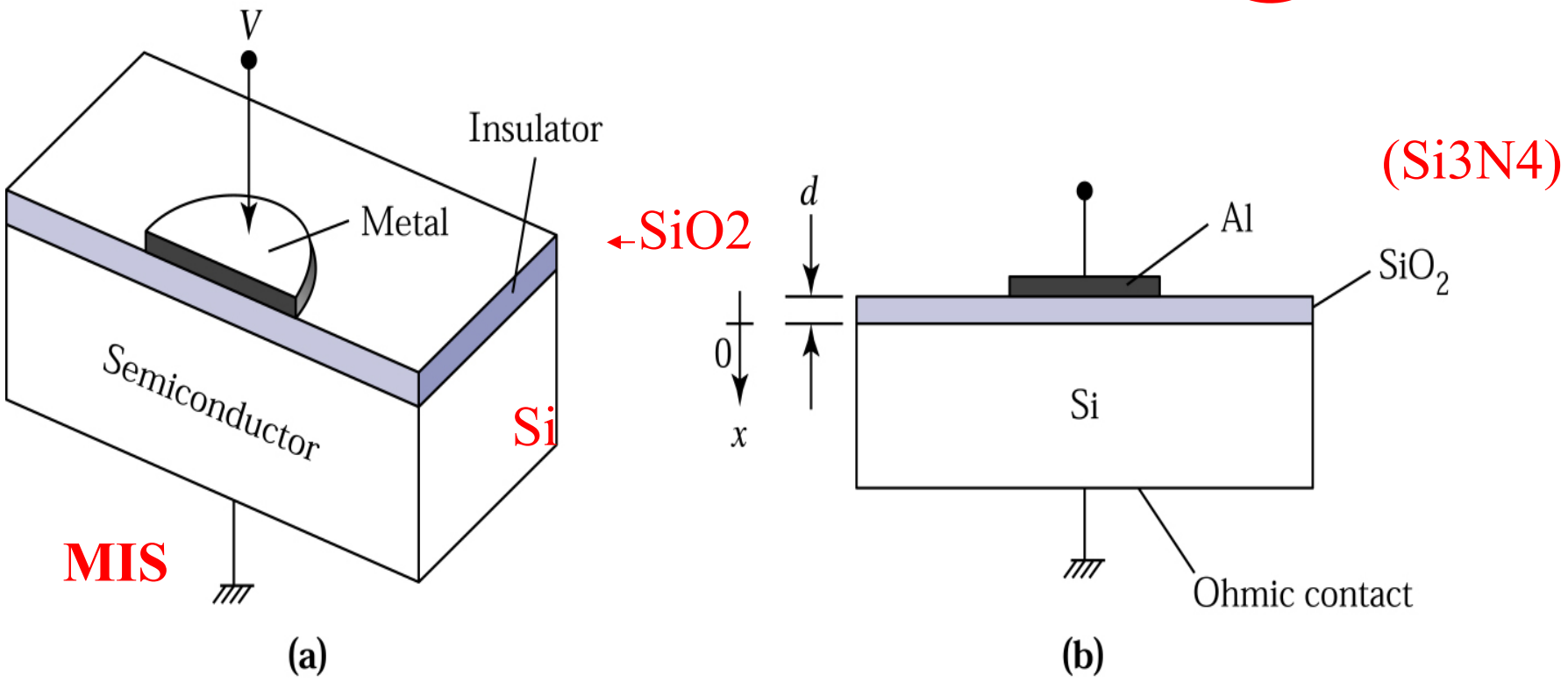


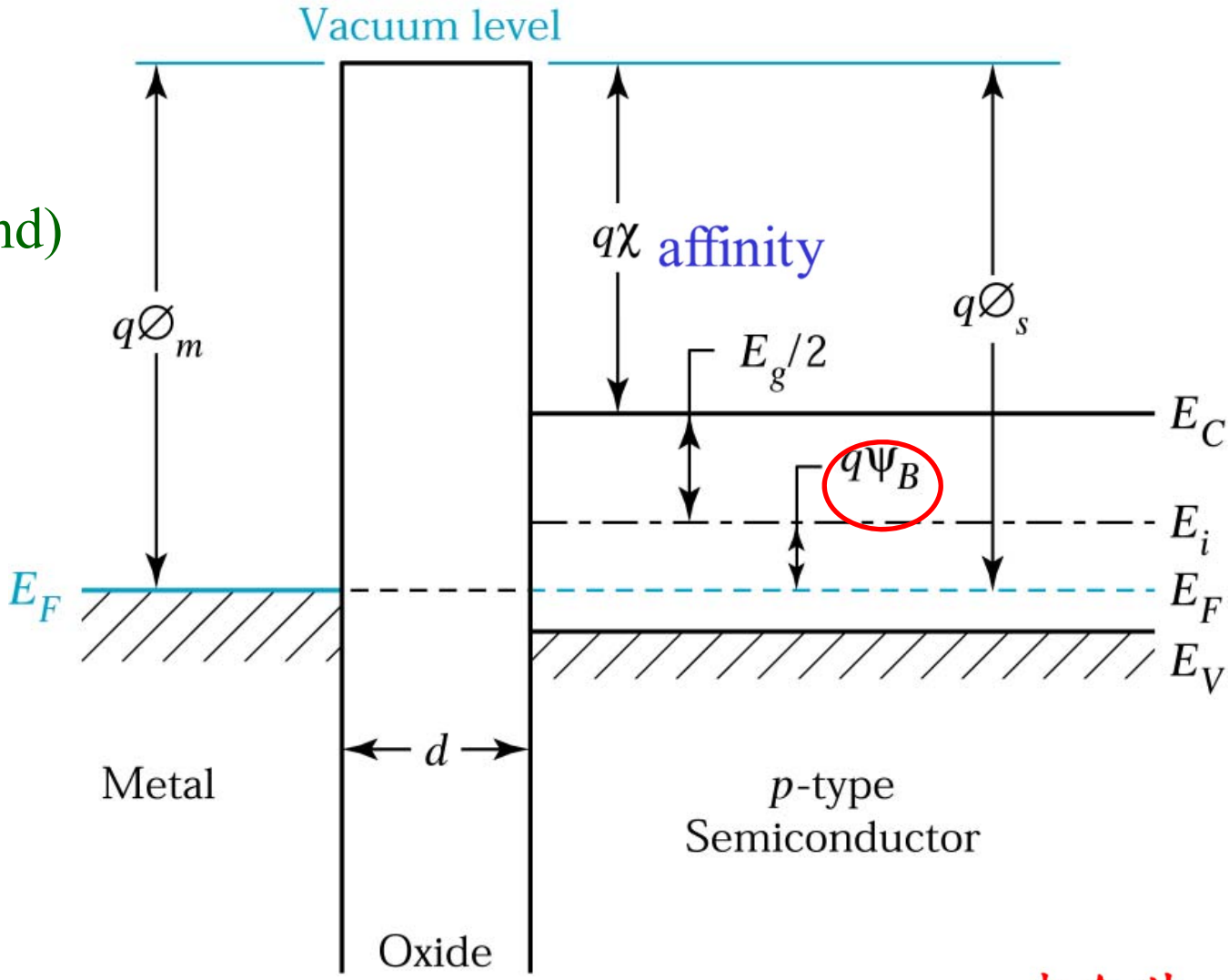
Figure 5.1. (*a*) Perspective view of a metal-oxide-semiconductor (MOS) diode. (*b*) Cross-section of an MOS diode.

Ideal MOS：

1.Φm= Φs(flat band)

2.Qm=Qs,某VG下

3.Rox→∞



先令其

$$q\Phi_{ms} \equiv (q\Phi_m - q\Phi_s) = q\Phi_m - [q\chi + E_g/2 + q\Psi_B] = 0$$

Figure 5.2. Energy band diagram of an ideal MOS diode at V = 0.

$$p_p = n_i e^{(E_i - E_F)/KT} \quad (2)$$

$$n_p = n_i e^{(E_F - E_i)/KT} \quad (3)$$

$E_F - E_i > 0$, n_p ↑ ↑

$$Q_s = Q_n - Q_{sc} = -qN_A W \quad (3)$$

單位面積空間

Figure 5.3.
Energy band diagrams and charge distributions of an ideal MOS diode in (*a*) accumulation, (*b*) depletion, and (*c*) inversion cases.

Inv.

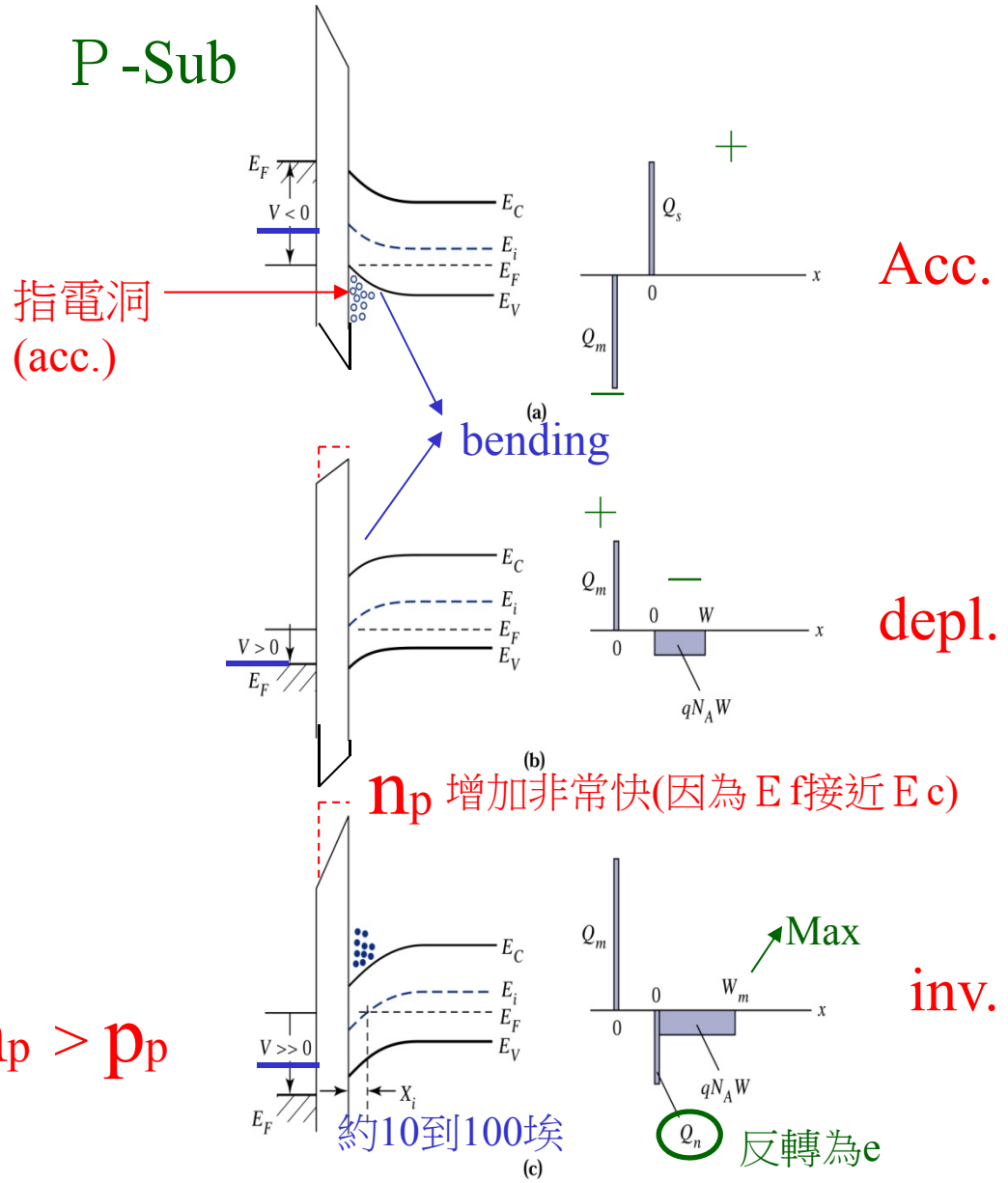
$$Q_s = Q_n + Q_{sc}$$

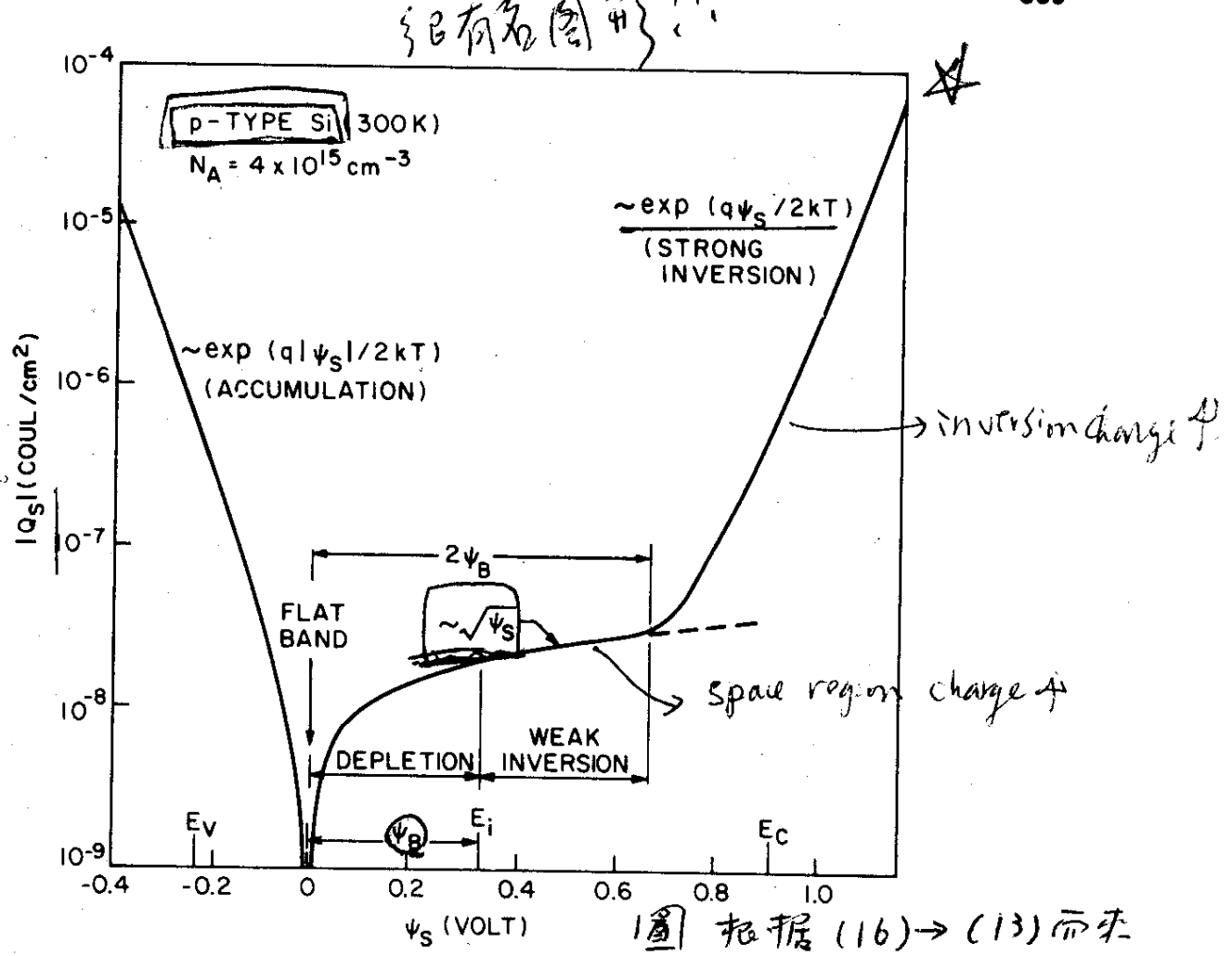
Strong inv. $$Q_{sc} = -qN_A W_m$$

固定 Max.

Strong inv. 後,負Q大部分由Qn提供

$n_p > p_p$





g. 5 Variation of space-charge density in the semiconductor as a function of the rface potential ψ_s for a *p*-type silicon with $N_A = 4 \times 10^{15}\ cm^{-3}$ at room temperature; ψ_B the potential difference between the Fermi level and the intrinsic level of the bulk miconductor. (After Garrett and Brattain, Ref. 13.)

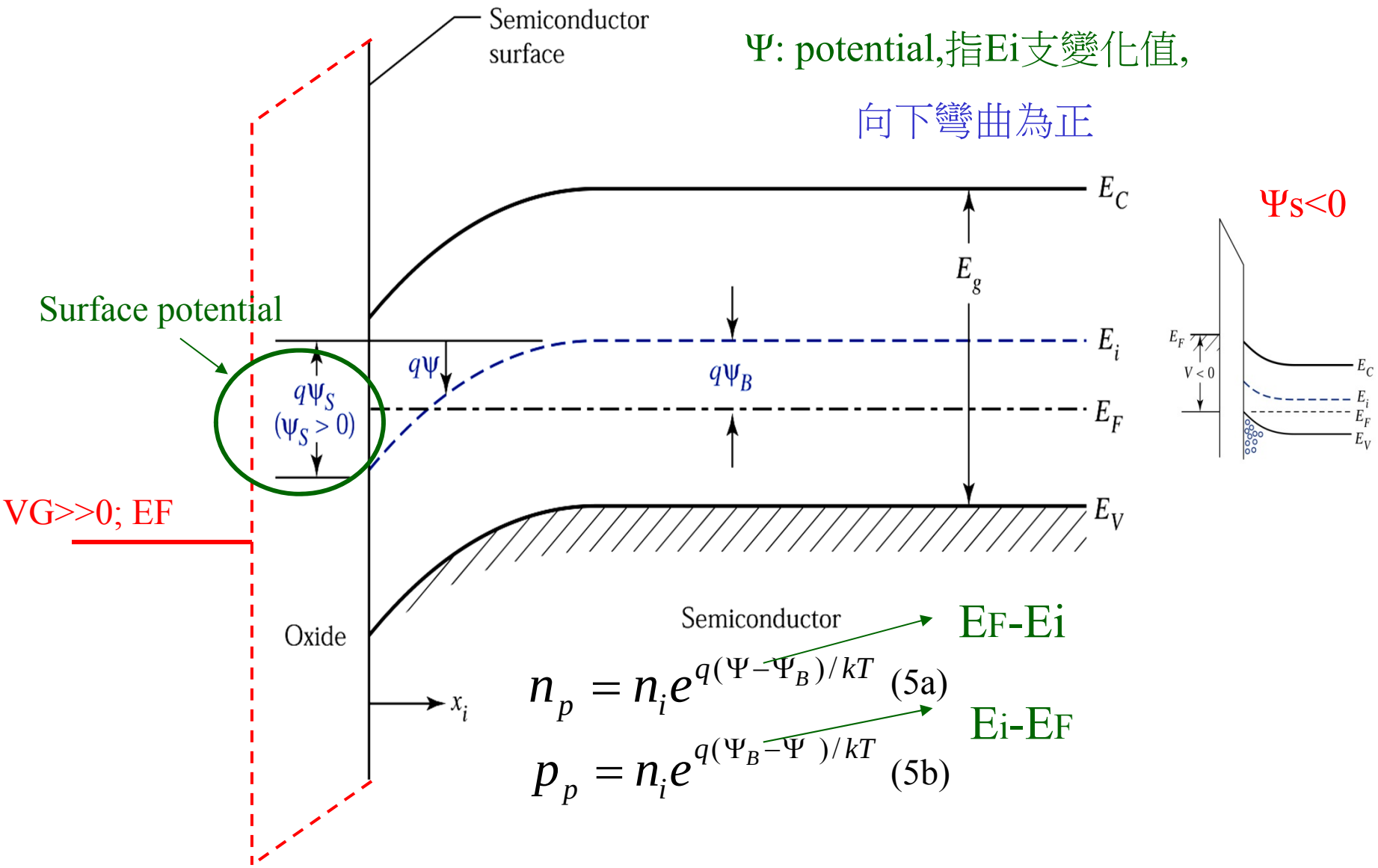


Figure 5.4. Energy band diagrams at the surface of a *p*-type semiconductor.

$\psi_s < 0$	Accumulation of holes (bands bend upward)
$\psi_s = 0$	Flat-band condition 在Si為平的
$\psi_B > \psi_s > 0$	Depletion of holes (bands bend downward)
$\psi_s = \psi_B$	Midgap with $n_s = n_p = n_i$ (intrinsic concentration)
$\psi_s > \psi_B$	Inversion (bands bend downward as shown in Fig. 24).
$\psi_s = 2\psi_B$	Strong inv. (ns=NA) EF-Ei = ΨB

Poisson equation :

$$\frac{d^2\Psi}{dx^2} = \frac{-\rho_s(x)}{\varepsilon_s} \qquad (7)$$

$$\frac{d\Psi}{dx} = \int_W^x \frac{qN_A}{\varepsilon_s} dx = (x - W)\frac{qN_A}{\varepsilon_s}$$

$$\Psi = \frac{qN_A}{\varepsilon_s}\left(\frac{x^2}{2} - Wx\right)\Big|_w^x$$

$$= \frac{qN_A}{2\varepsilon_s} W^2 \left(1 - \frac{x}{w}\right)^2$$

$$\Psi = \Psi_s\left[1 - \frac{x}{W}\right]^2 \qquad (8)$$

Surface potential Ψs is (x=0之Ψ)　　像n+p junction

$$\Psi_s = \frac{qN_A W^2}{2\varepsilon_s} \qquad (9)$$

定義 strong inv. : (W 達Wmax)

$$n_s = N_A \quad \longleftrightarrow \quad \psi_s = 2\psi_B$$

即 $$\Psi_s(inv) \approx 2\Psi_B = \frac{2KT}{q}\ln[\frac{N_A}{n_i}] \qquad (10)$$

Barrier (Vbi-V)

Strong inv.

$$W_m = \sqrt{\frac{2\varepsilon_s \Psi_s(inv)}{qN_A}} \cong \sqrt{\frac{2\varepsilon_s(2\Psi_B)}{qN_A}} = \sqrt{\frac{4\varepsilon_s KT\ln(N_A/n_i)}{q^2 N_A}} \qquad (11\&11a)$$

$$Q_{sc} = -qN_A W_m \cong -\sqrt{2q\varepsilon_s N_A(2\Psi_B)} \qquad (12)$$

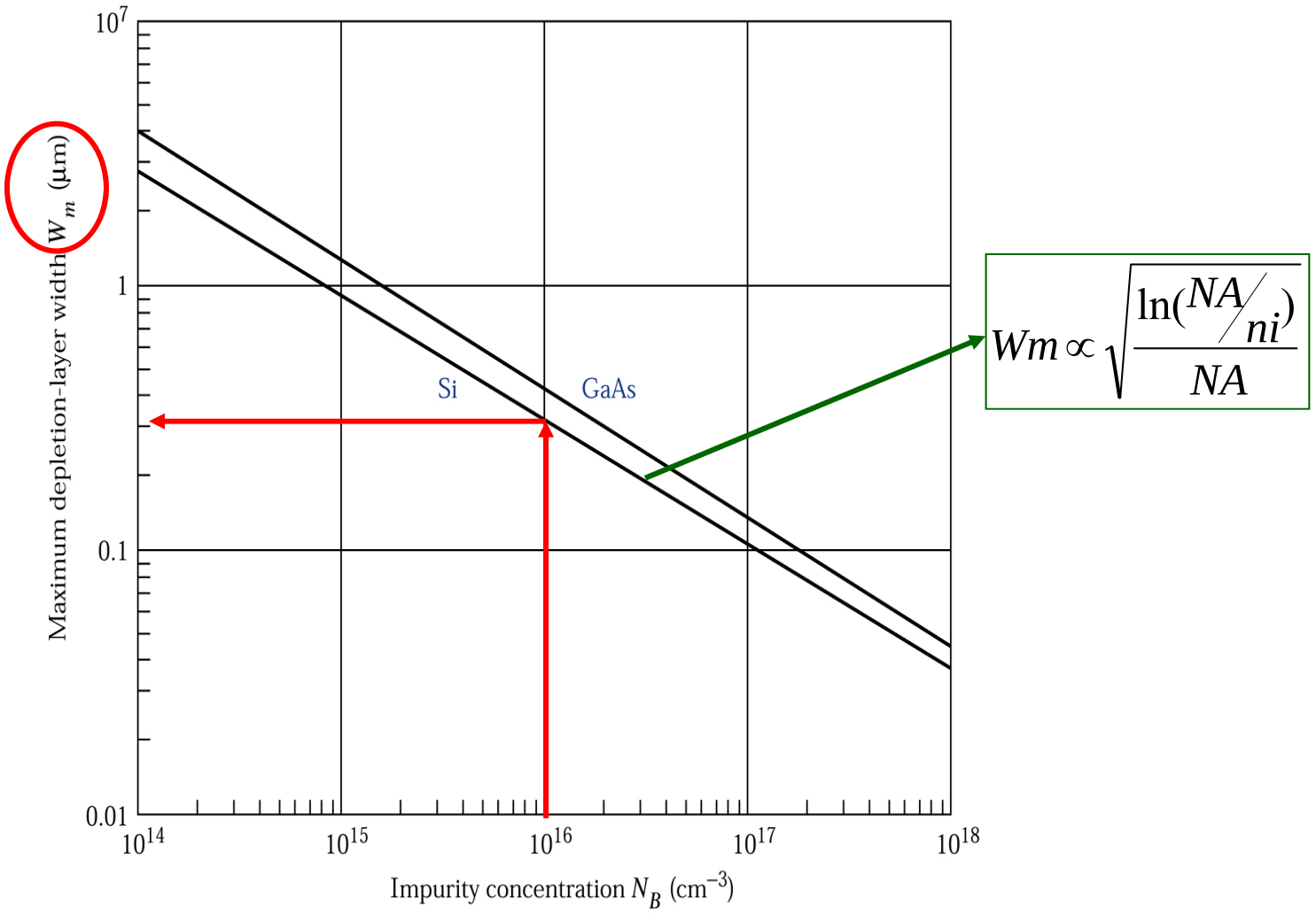


Figure 5.5. Maximum depletion-layer width versus impurity concentration of Si and GaAs under strong-inversion condition.

Ideal MOS curves (參看 F.6)

外加 → V ← SiO2上

$$V = V_o + \Psi_s \qquad (13)$$

Ψ_s → Si上

Si單位面積電荷 → $|Q_s|$

$$V_o = E_o d = \frac{|Q_s| d}{\varepsilon_{ox}} \equiv \frac{|Q_s|}{C_o} \qquad (14)$$

C_o → 單位面積電容

(C=Co 串 Cj) C_j ← 空乏區電容

$$C = \frac{C_o C_j}{C_o + C_j} \qquad (15)$$

$$Cj = \frac{\varepsilon_s}{W}$$

由9,13,14,15消去W →

depletion →

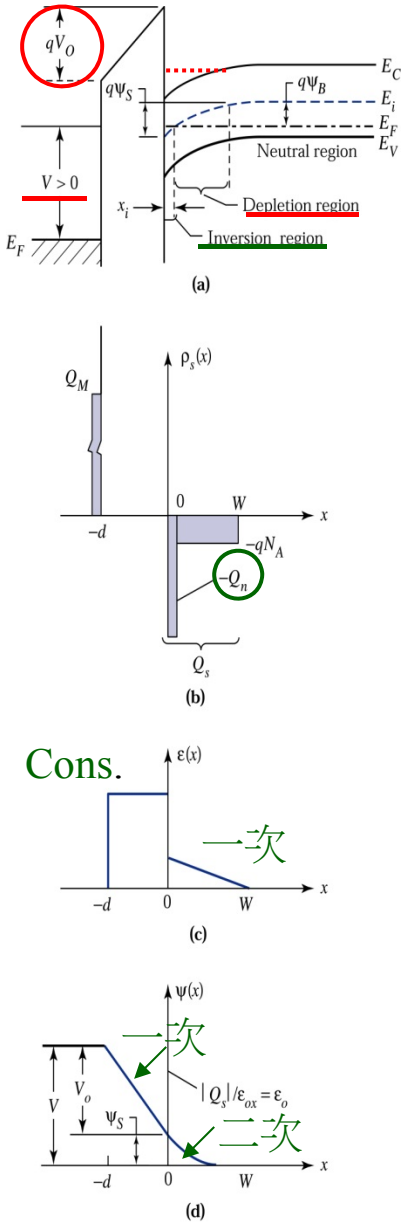
$$\frac{C}{C_o} = \frac{1}{\sqrt{1 + \frac{2\varepsilon_{ox}^2 V}{qN_A\varepsilon_s d^2}}} \qquad (16)$$

Dep.之 C-V曲線

Acc. C=Cox（無Cj)

最常用之MOS結構（P-Sub）

Figure 5.6.
(*a*) Band diagram of an ideal MOS diode. (*b*) Charge distributions under inversion condition. (*c*) Electric-field distribution. (*d*) Potential distribution.



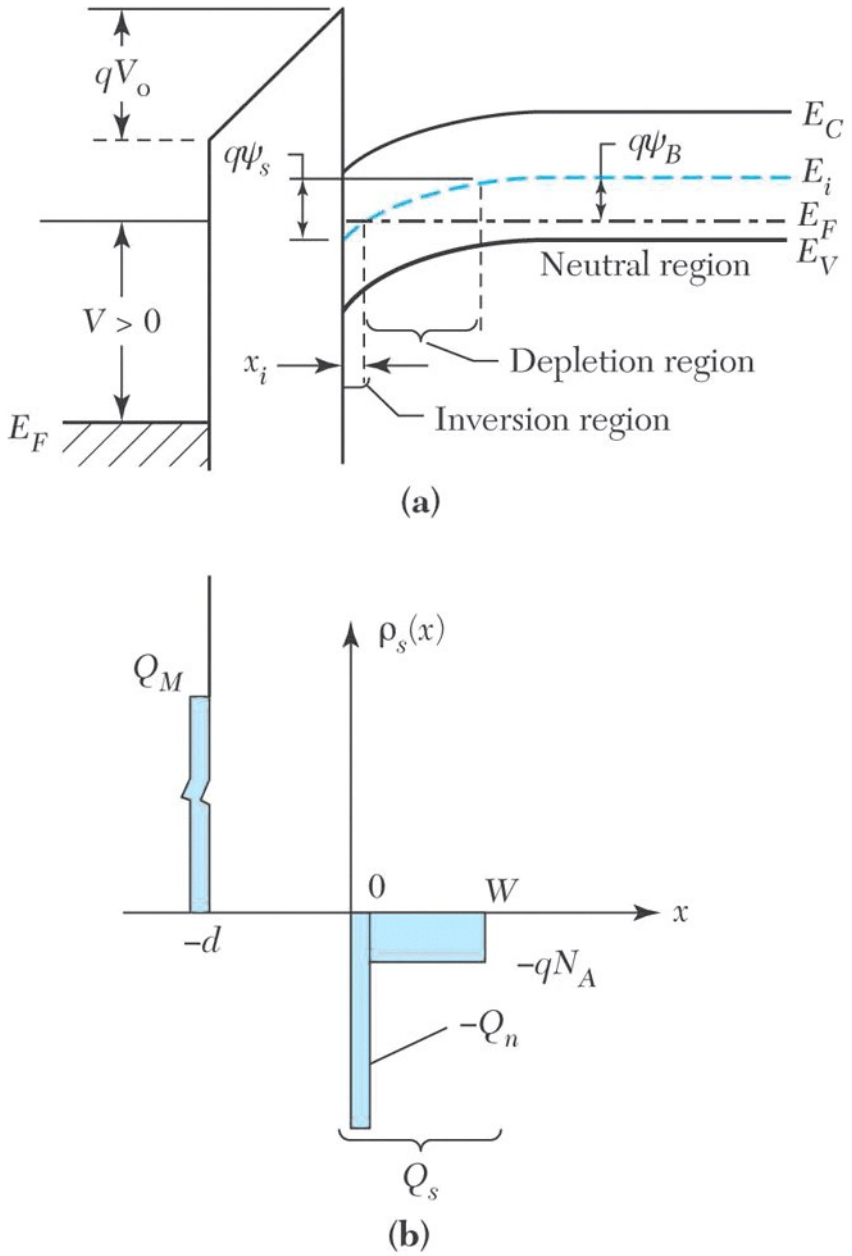
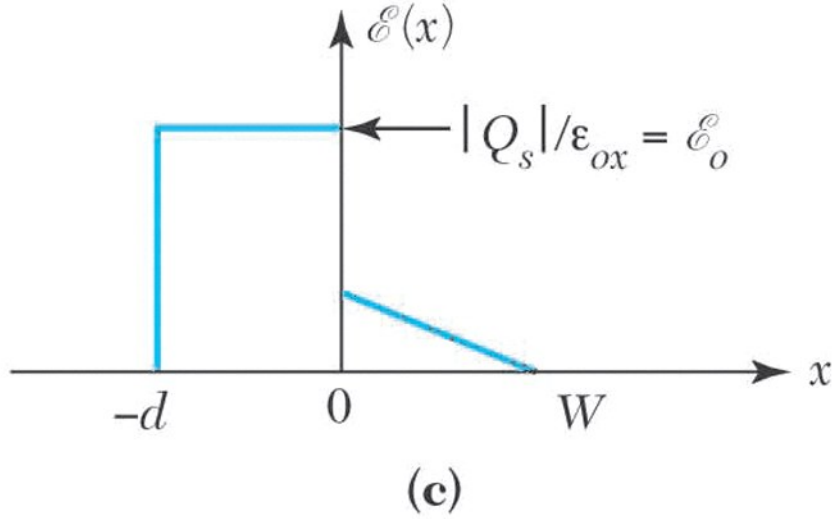


Figure 5.6ab



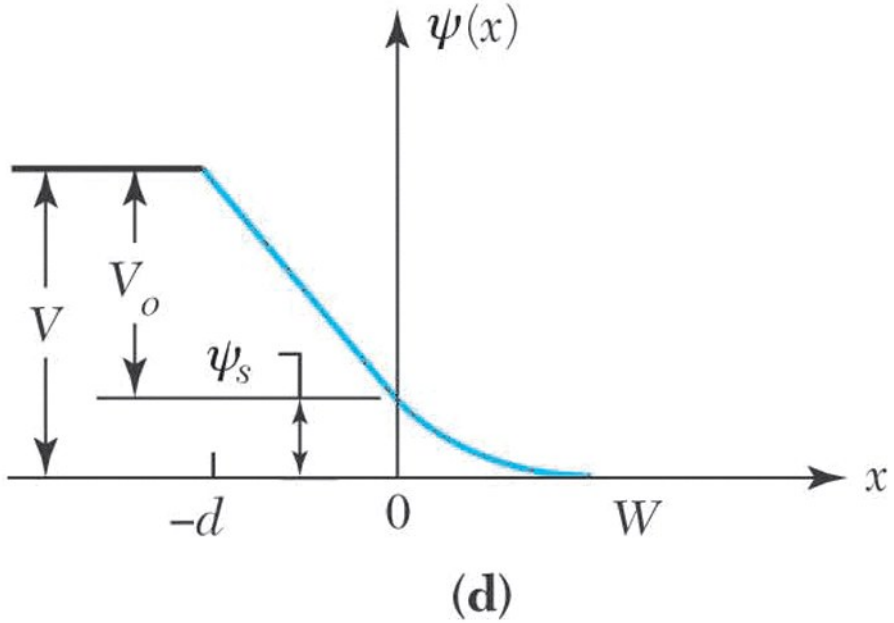


Figure 5.6cd

Qs(Qn太薄忽略)

Threshold (strong inv. 發生時)

$$V_T = \frac{qN_A W_m}{C_o} + \Psi_s(inv) \cong \frac{\sqrt{2\varepsilon_s qN_A(2\Psi_B)}}{C_o} + 2\Psi_B \qquad (17)$$

$$C_{\min} = \frac{\varepsilon_{ox}}{d + (\varepsilon_{ox}/\varepsilon_s)W_m} \qquad (18)$$

不變

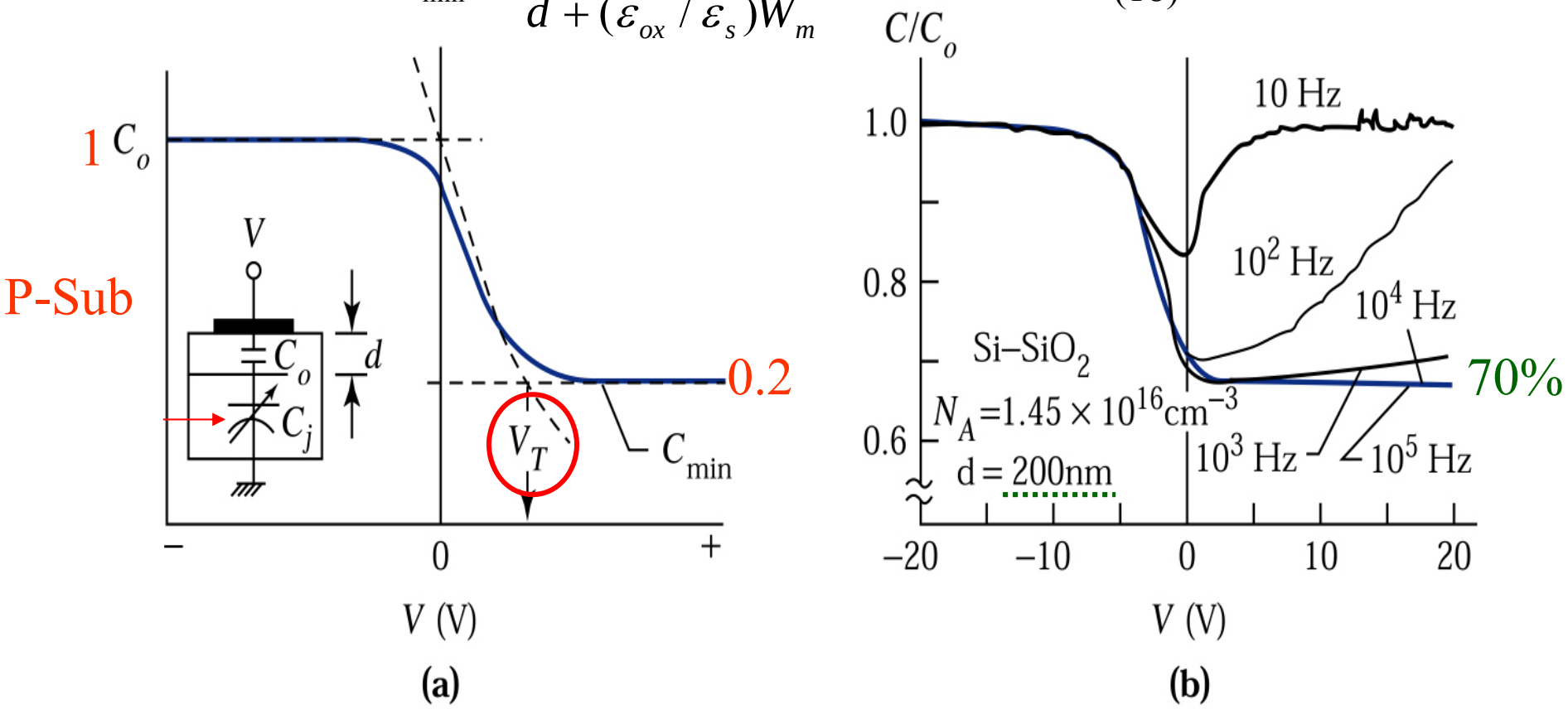
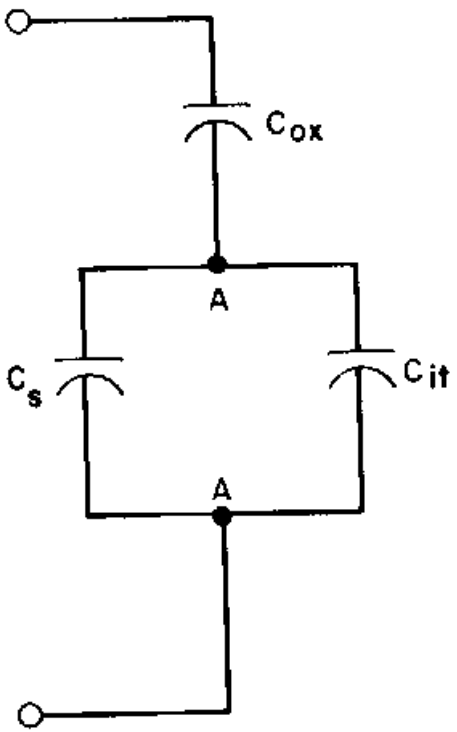


Figure 5.7. (*a*) High-frequency MOS *C-V* curve showing its approximated segments (dashed lines). Inset shows the series connection of the capacitors. (*b*) Effect of frequency on the *C-V* curve.[2]



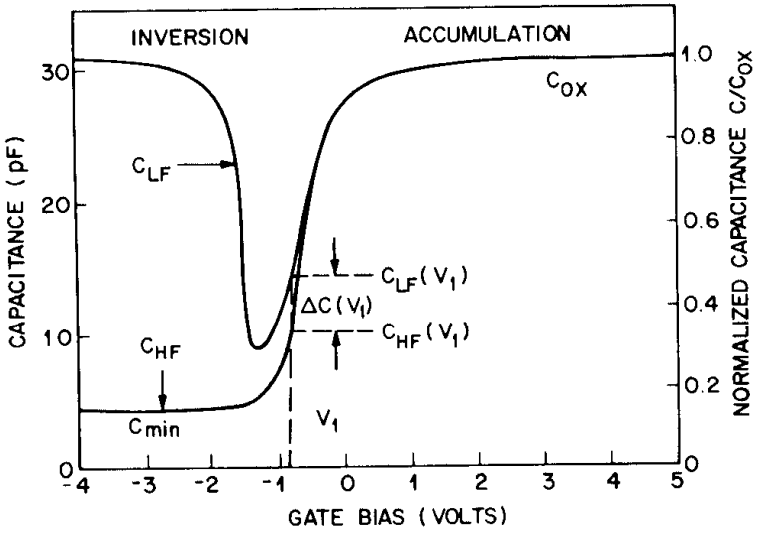


Fig. 8.9 High frequency capacitance C_{HF} and low frequency capacitance C_{LF} as functions of gate bias for an *n*-type sample illustrating the parameters needed to graphically extract interface trap level density using the high-low frequency capacitance method. After Wagner and Berglund.[7]

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}}$$

frequency capacitance measured a
ields

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - C_s.$$

$$C_s = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}.$$

) becomes

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}.$$

$$C_{LF} = \Delta C + C_{HF} \qquad (8.23)$$

$C = C_{LF} - C_{HF}$. Substituting (8.23) into (8.22) yields

$$D_{it} = \frac{C_{ox}}{q}\left[\left(\frac{1}{\Delta C/C_{ox} + C_{HF}/C_{ox}} - 1\right)^{-1} - \left(\frac{1}{C_{HF}/C_{ox}} - 1\right)^{-1}\right]$$

$$= \frac{\Delta C}{q}\left(1 - \frac{C_{HF} + \Delta C}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1} \qquad (8.24)$$

C_{it} is related to D_{it} by (8.13). Equation (8.24) from Wagner
[17] is plotted in Fig. 8.8 with

$$D_{it} = D_{ito}\frac{1000}{x_o} \qquad (8.25)$$

Problem

For an ideal metal–SiO_2–Si diode having $N_A = 10^{16}\ cm^{-3}$ and $d = 250$ Å, calculate the minimum capacitance on the C–V curve of Fig. 27*a*. The relative dielectric constant of SiO_2 is 3.9.

Solution

$$C_o = \frac{\epsilon_{ox}}{d} = \frac{3.9 \times (8.85 \times 10^{-14})}{250 \times 10^{-8}} = 1.38 \times 10^{-7}\ \text{F/cm}^2$$

$$Q_{sc} = -qN_A W_m = -1.6 \times 10^{-19} \times 10^{16} \times (3 \times 10^{-5}) = -4.8 \times 10^{-8}\ \text{C/cm}^2 .$$

We used Fig. 25 for W_m;

$$\psi_s(\text{inv}) = 2\psi_B = \frac{2kT}{q} \ln \left(\frac{N_A}{n_i} \right) = 0.69\ \text{V}$$

$$V_T = -\frac{Q_{sc}}{C_o} + 2\psi_B = 0.35 + 0.69 = 1.04\ \text{V} .$$

The minimum capacitance $C_{\min}$ at V_T is

$$C_{\min} = \frac{\epsilon_{ox}}{d + (\epsilon_{ox}/\epsilon_s) W_m} = \frac{3.9 \times (8.85 \times 10^{-14})}{2.5 \times 10^{-6} + (3.9/11.9) 3 \times 10^{-5}}$$

$$= 2.8 \times 10^{-8}\ \text{F/cm}^2 .$$

Therefore, $C_{\min}$ is about 20% of C_o.

Figure 5.8.
Work function difference as a function of background impurity concentration for Al, *n*+-, and *p*+ polysilicon gate materials.

Ideal qΦms =0

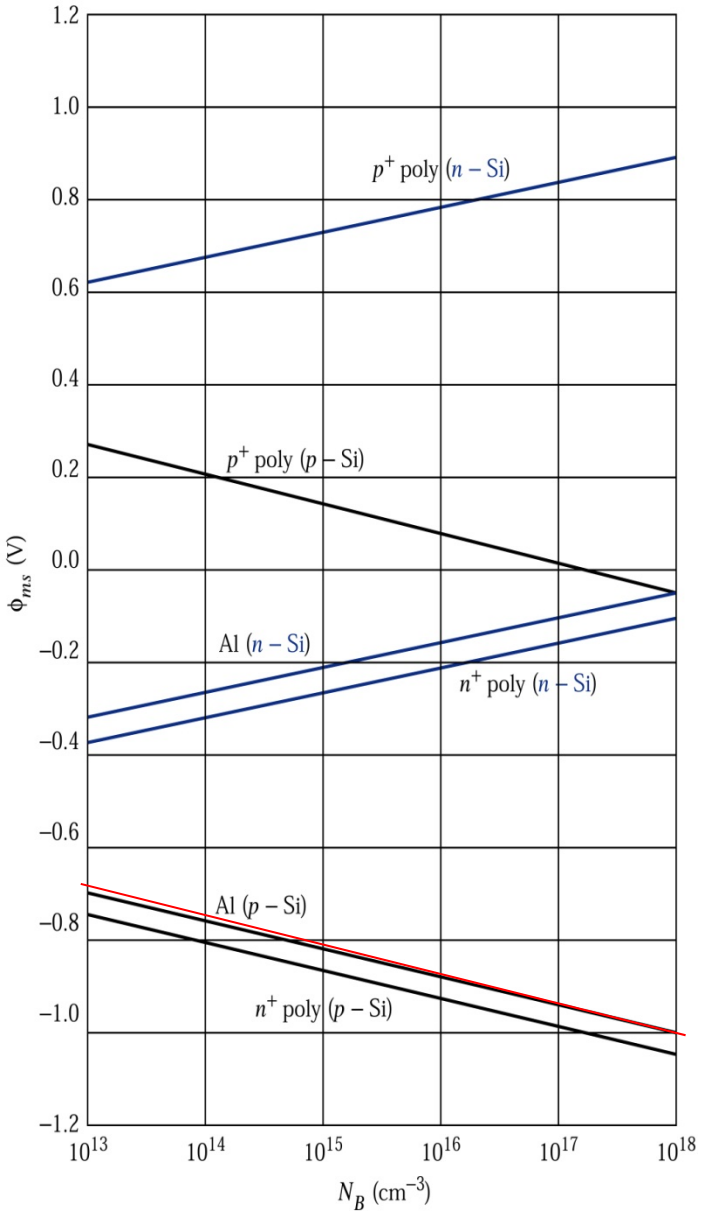
qΦms= qΦm- qΦs

Al: qΦm = 4.1eV

n+-poly: qΦm=3.95eV

通常為負

P-Sub,負更多



$$V_{FB} = \frac{q\Phi_{ms}}{q} = \Phi_m - \Phi_s$$

Flat-band (在Si),定義Ψs=0

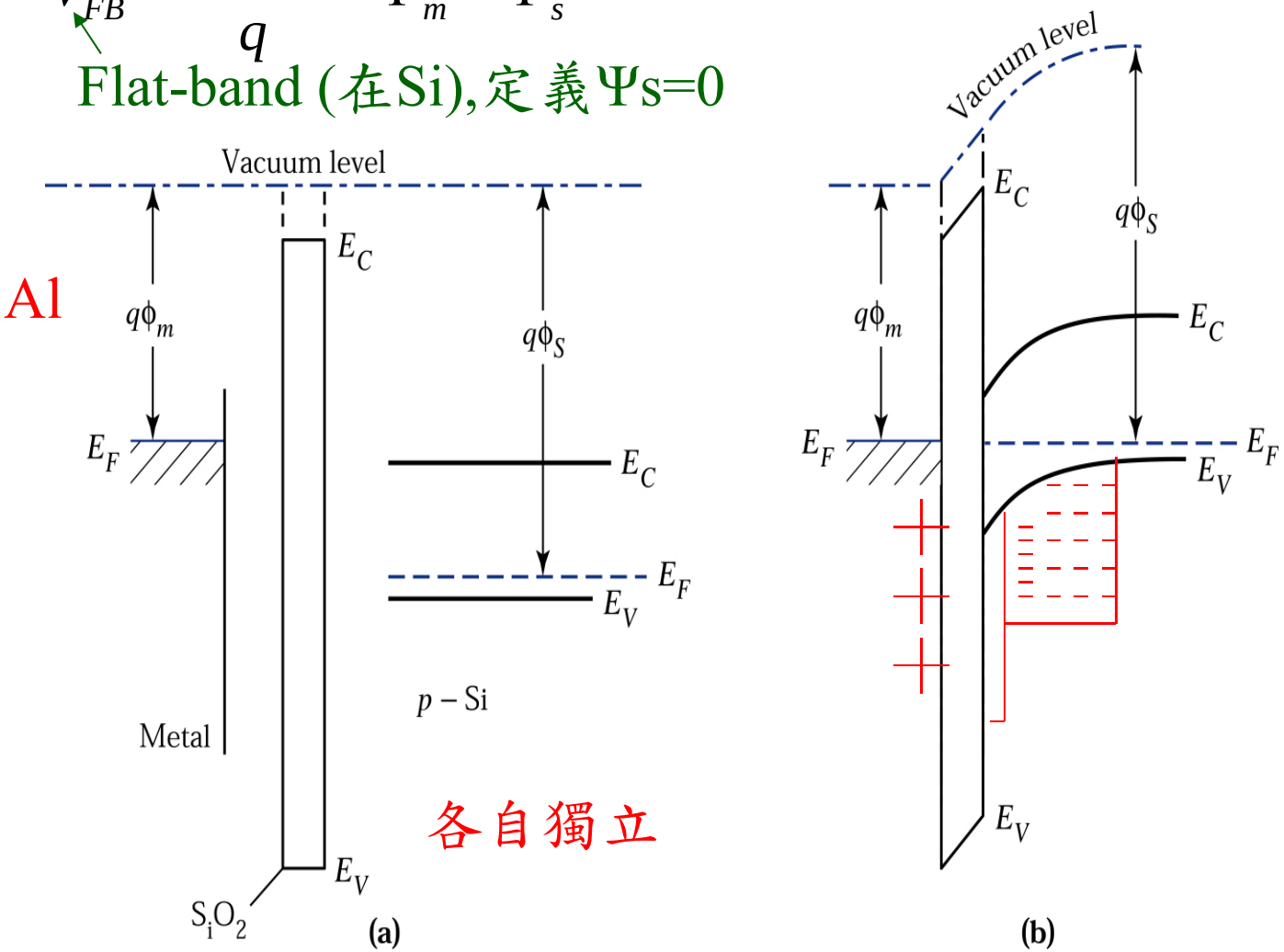


Figure 5.9. (*a*) Energy band diagram of an isolated metal and an isolated semiconductor with an oxide layer between them. (*b*) Energy band diagram of an MOS diode in thermal equilibrium.

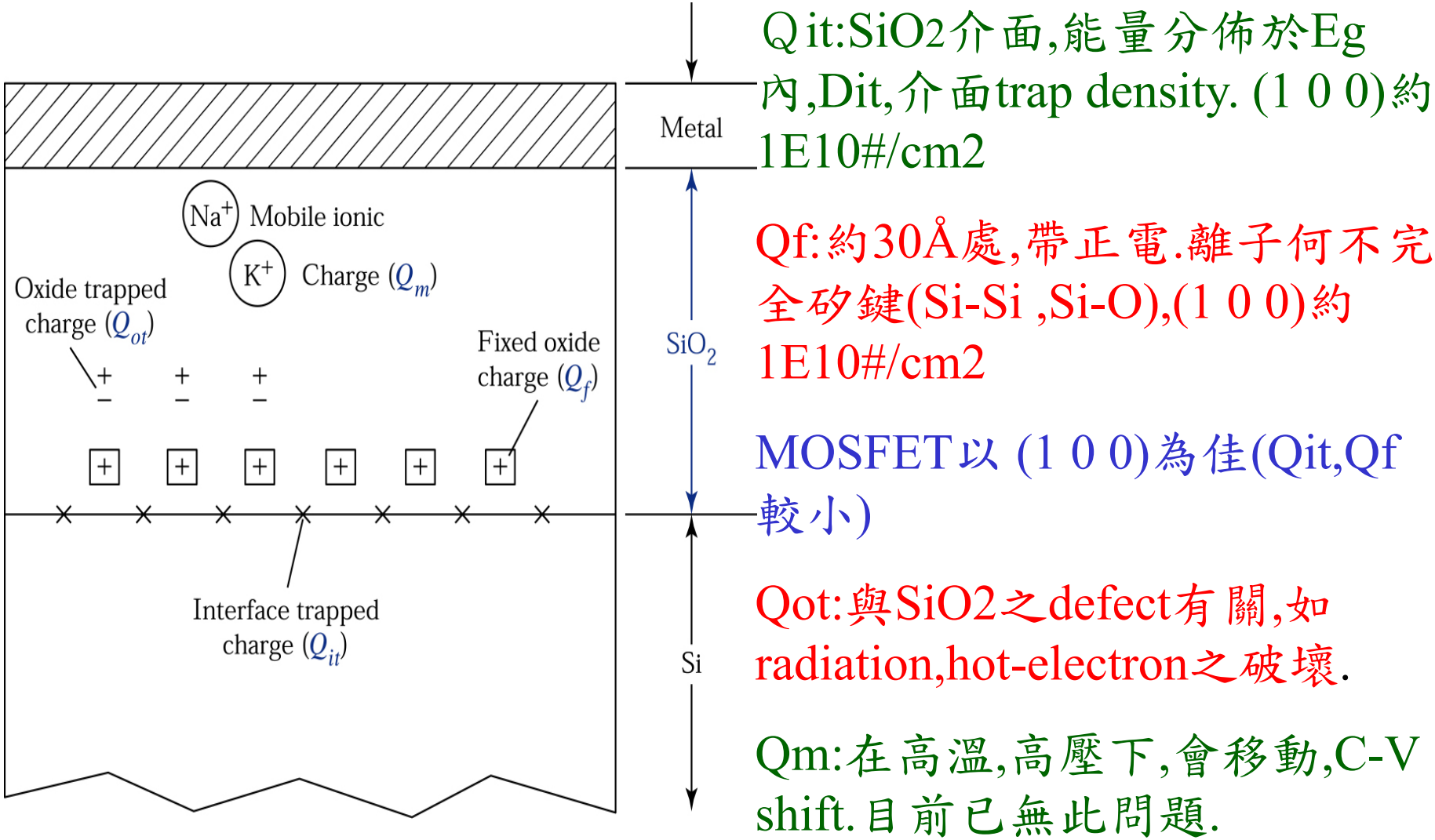


Figure 5.10. Terminology for the charges associated with thermally oxidized silicon.[3]

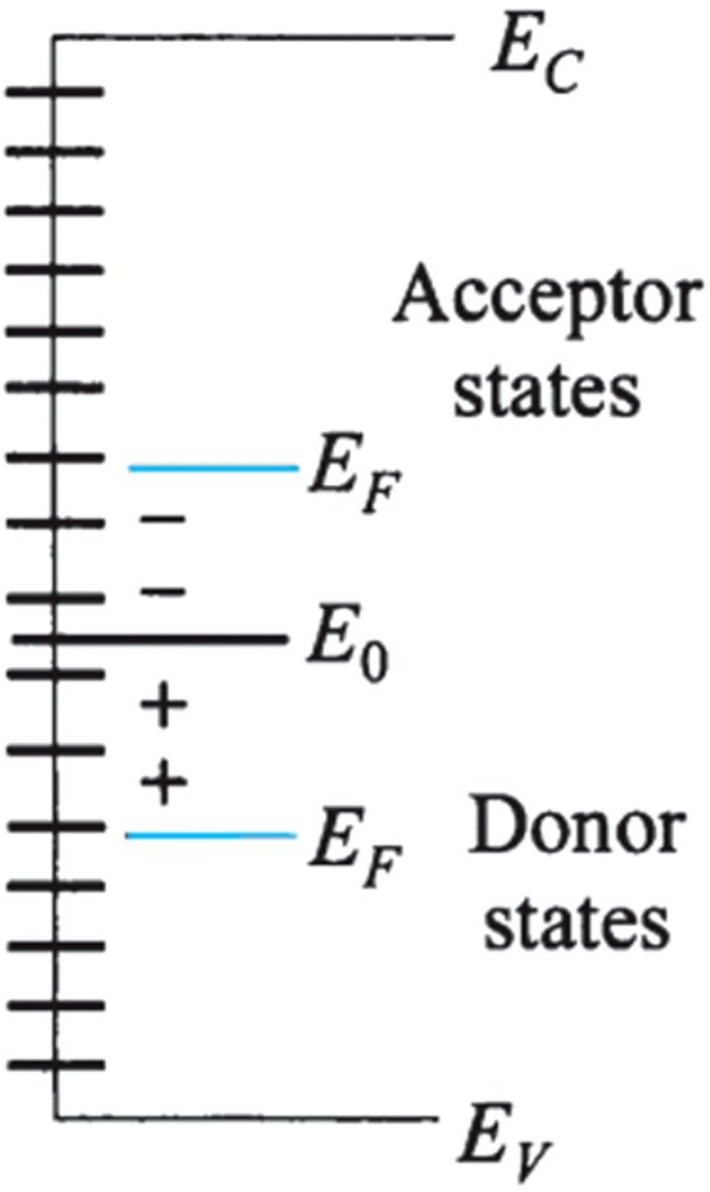


Figure 5.11

In general, acceptor states exist in the upper half of the bandgap and donor states exist in the lower half of the bandgap.

An acceptor state is neutral if the Fermi level is below the state and becomes negatively charged if the Fermi level is above the state.

A donor state is neutral if the Fermi level is above the state and becomes positively charged if the Fermi level is below the state.

The charge of the interface states is then a function of the gate voltage applied across the MOS capacitor.

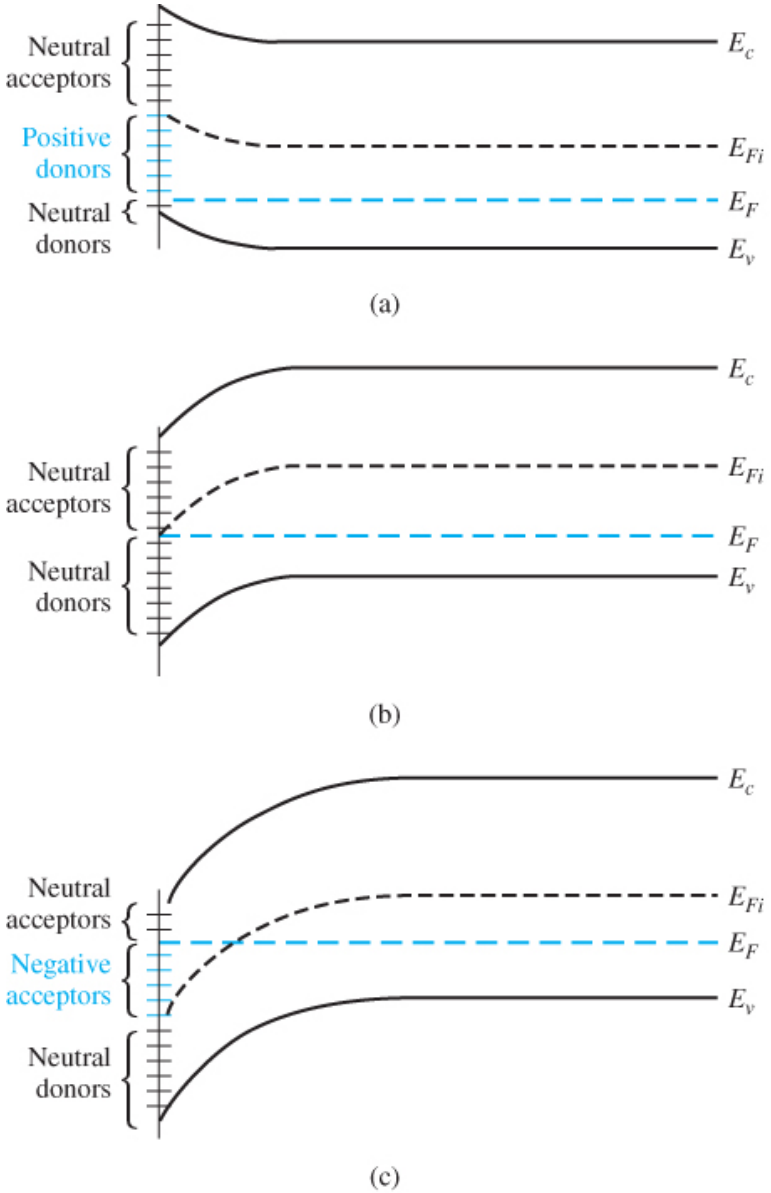


Figure 10.32 | Energy-band diagram in a p-type semiconductor showing the charge trapped in the interface states when the MOS capacitor is biased (a) in accumulation, (b) at midgap, and (c) at inversion.

there is a net posi- tive charge trapped in the donor states.

there is now a net negative charge in the acceptor states.

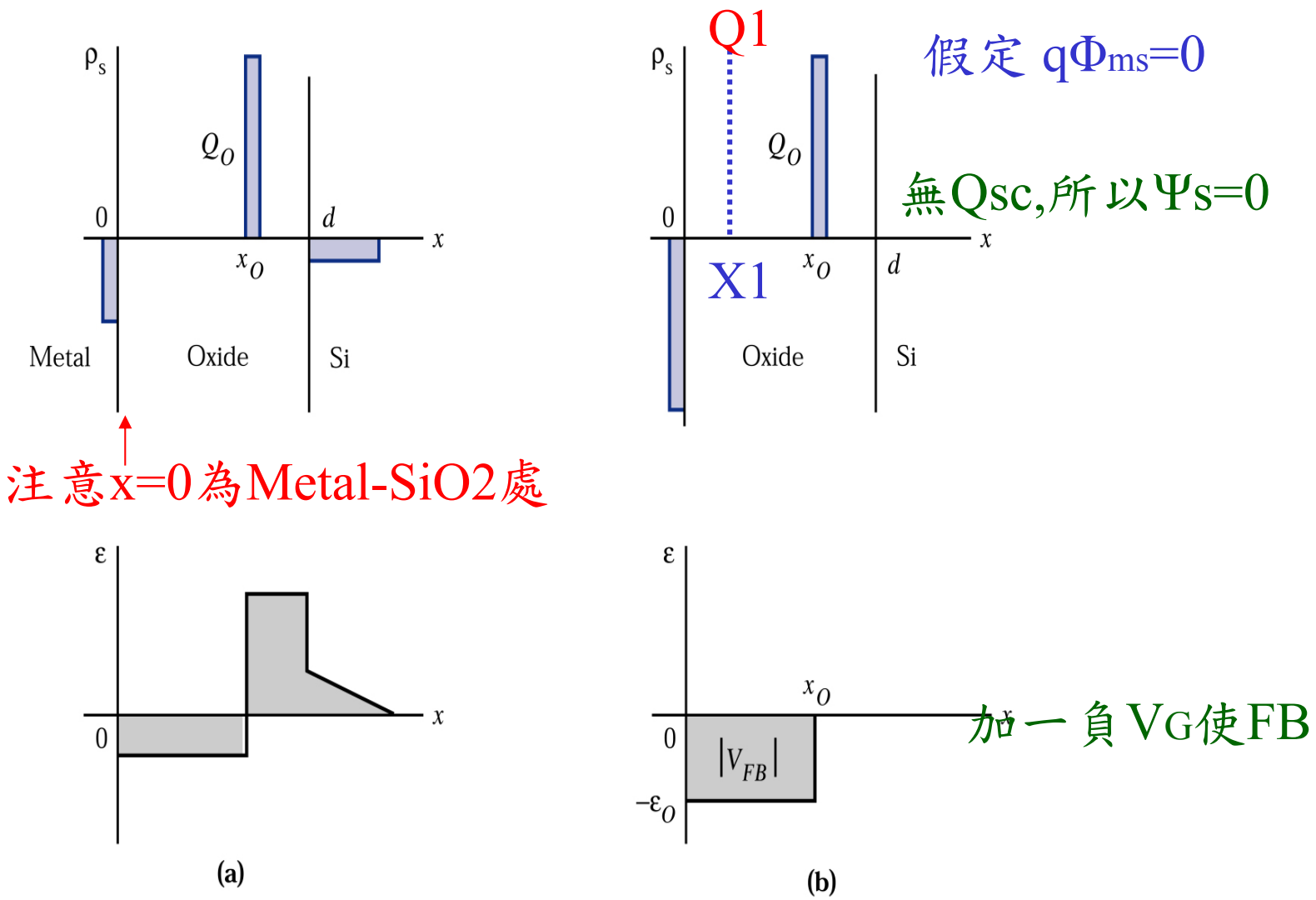


Figure 5.12. Effect of a sheet charge within the oxide.[2] (*a*) Condition for $V_G = 0$. (*b*) Flat-band condition.

Qo:單位面積電荷, Co:單位面積電容

$$V_{FB} = -\mathscr{E}_o x_o = -\frac{Q_o}{\epsilon_{ox}} x_o = -\frac{Q_o}{C_o}\frac{x_o}{d} . \qquad (19)$$

當Qo接近SiO2/Si時 (Xo=d)

$$V_{FB} = -\frac{Q_o}{C_o}\left[\frac{d}{d}\right] = -\frac{Q_o}{C_o} . \qquad (20)$$

若Qo任意分布

Xo Qo

$$V_{FB} = -\frac{1}{C_o}\left[\frac{1}{d}\int_0^d x\,\rho(x)\,dx\right] \qquad (21)$$

ρ(x): volume charge density

得知ρot(x), ρm(x),可求出Qot,Qm對V_{FB}之影響

$$Q_{ot} \equiv \frac{1}{d}\int_0^d x\,\rho_{ot}(x)\,dx \qquad (22a)$$

$$Q_m \equiv \frac{1}{d}\int_0^d x\,\rho_m(x)\,dx . \qquad (22b)$$

(若Q為正,VG須加負)

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} . \qquad (23)$$

+Qit/Cox

無Q時,VFB=Φms

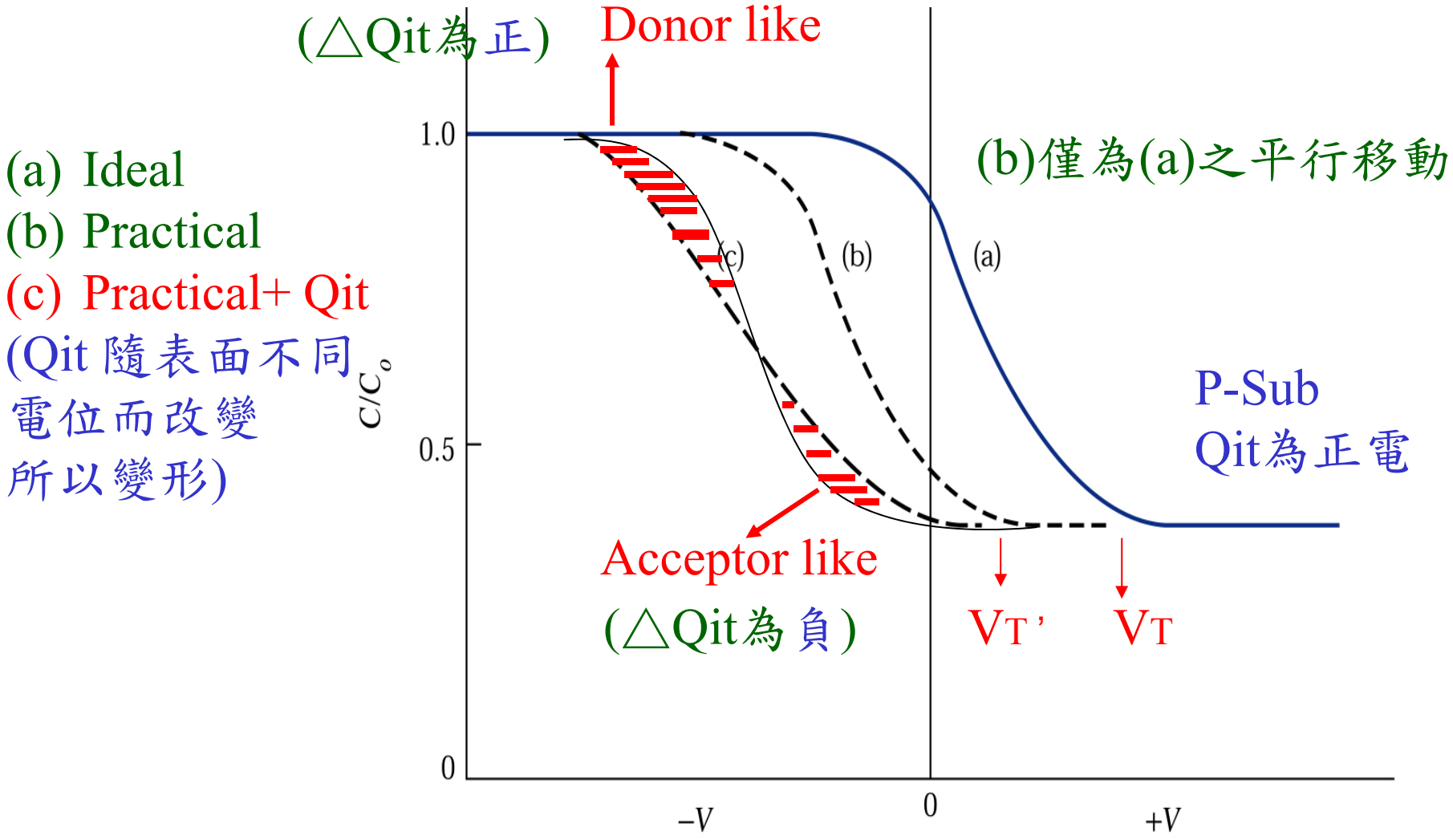
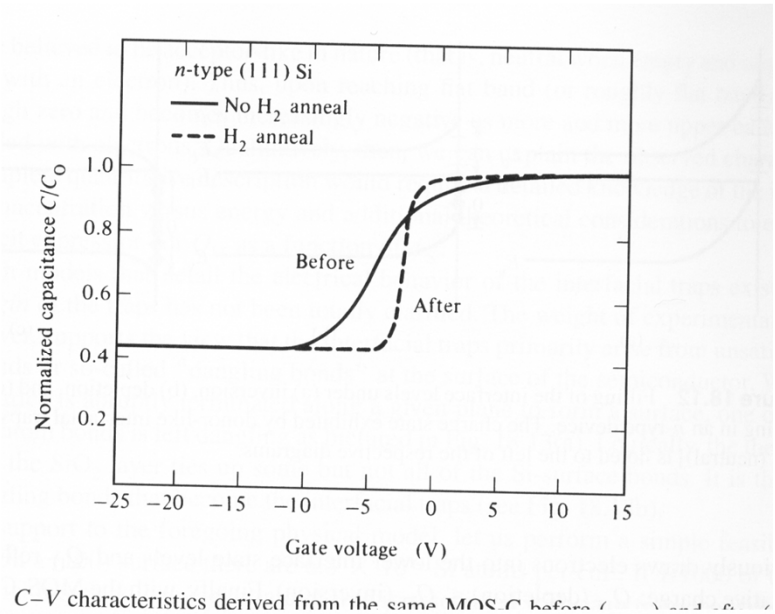


Figure 5.13. Effect of a fixed oxide charge and interface traps on the *C-V* characteristics of an MOS diode.



C–V characteristics derived from the same MOS-C before (

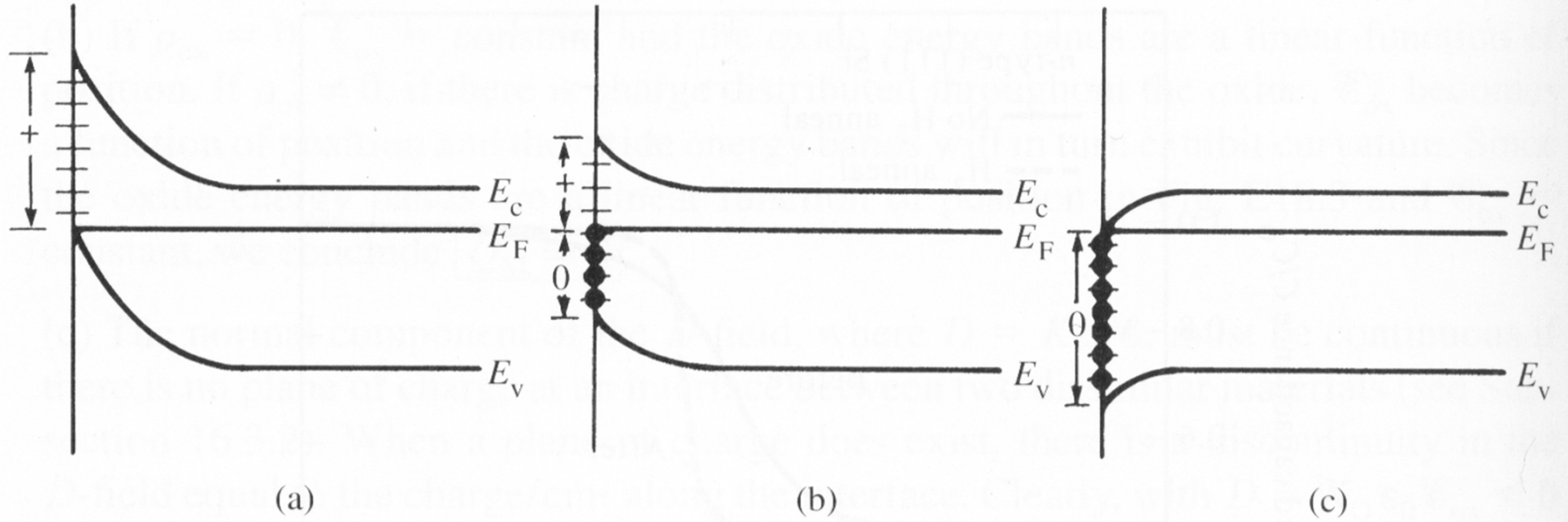


Figure 18.12 Filling of the interface levels under (a) inversion, (b) depletion, and (c) accumulation biasing in an *n*-type device. The charge state exhibited by donor-like interfacial traps ["+" (plus) or "0" (neutral)] is noted to the left of the respective diagrams.

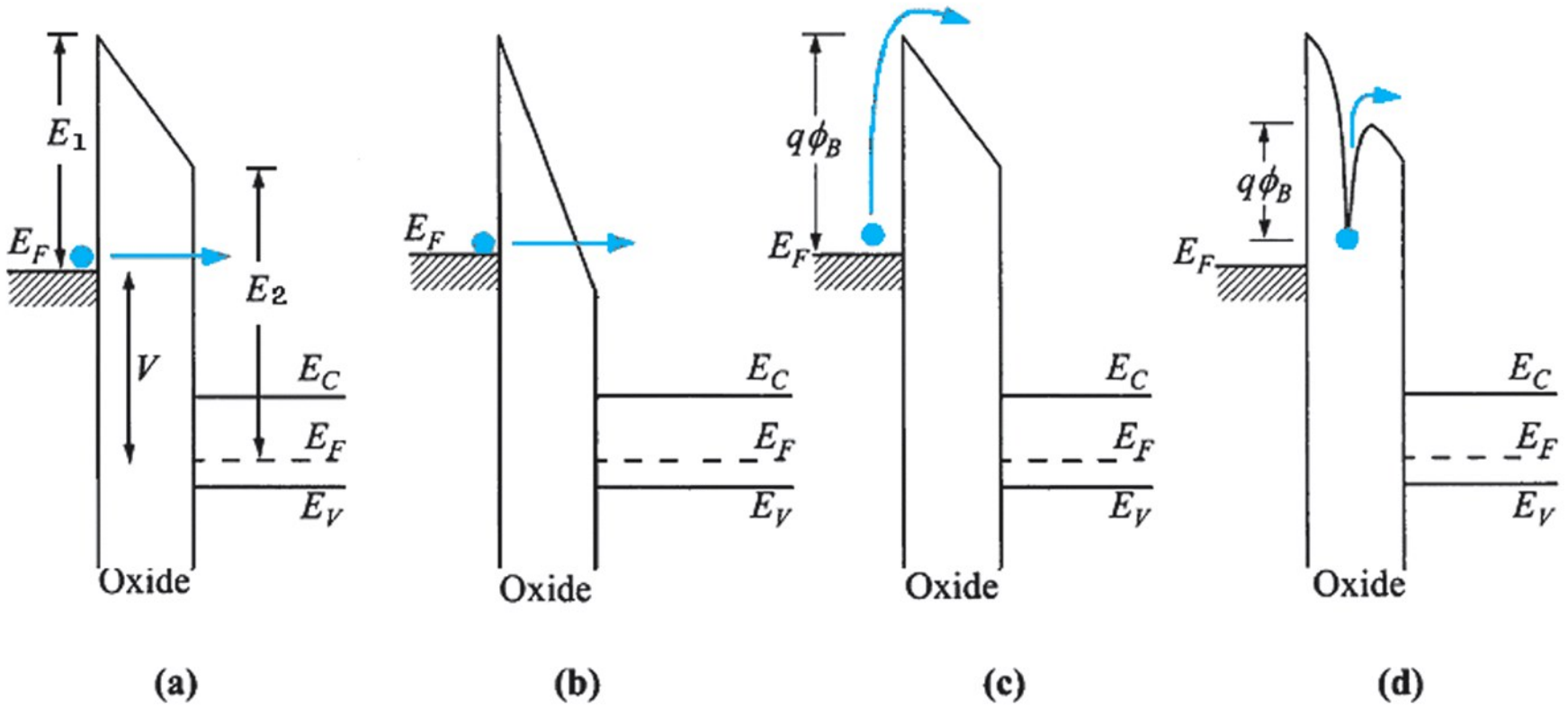


Figure 5.14

Conduction mechanisms in MOS,
(a) Direct tunneling (b) Fowler-Nordheim tunneling
(c) Thermionic emission (d) Frenkel-Poole emission

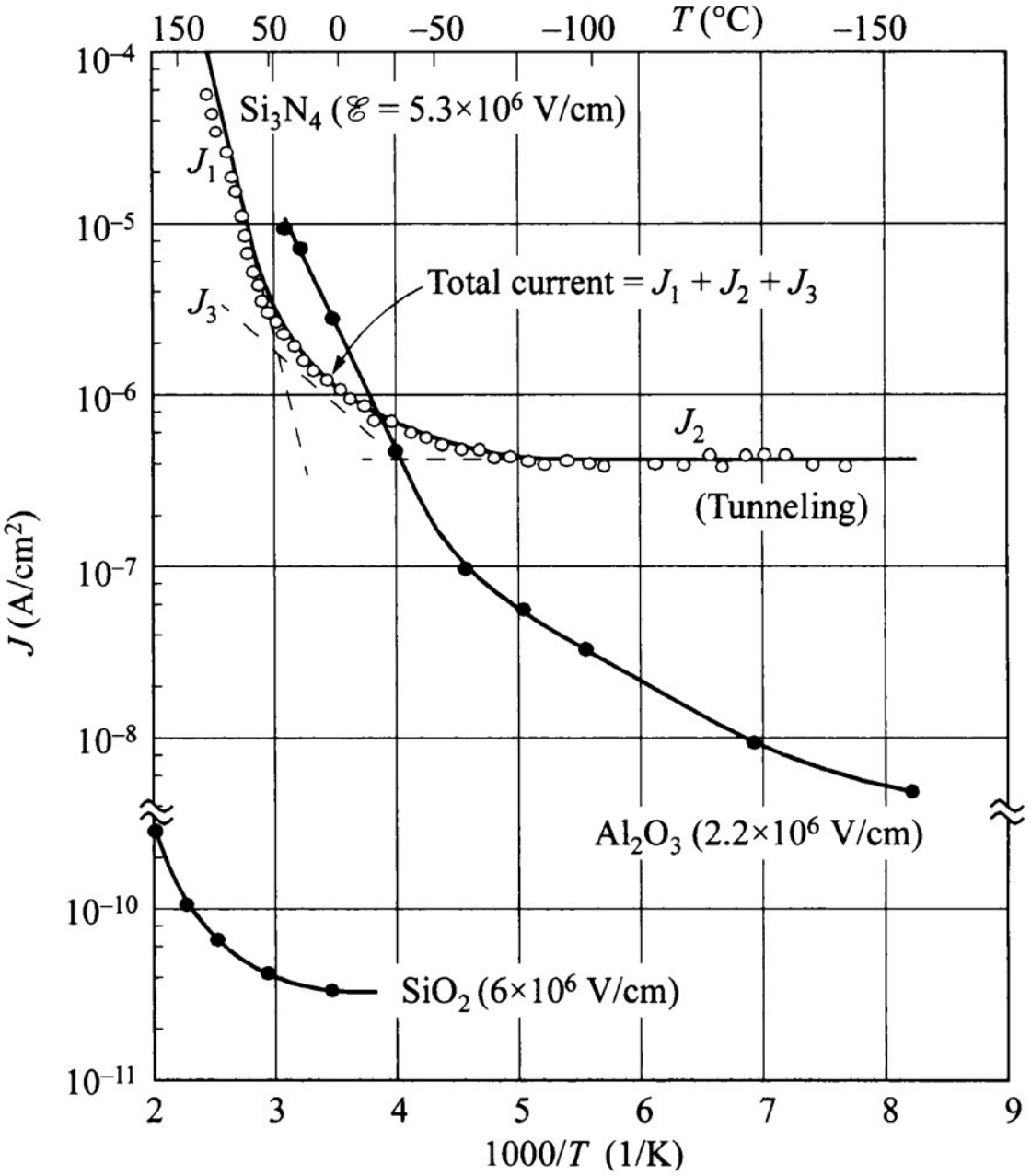


Figure 5.15

Dielectric Breakdown

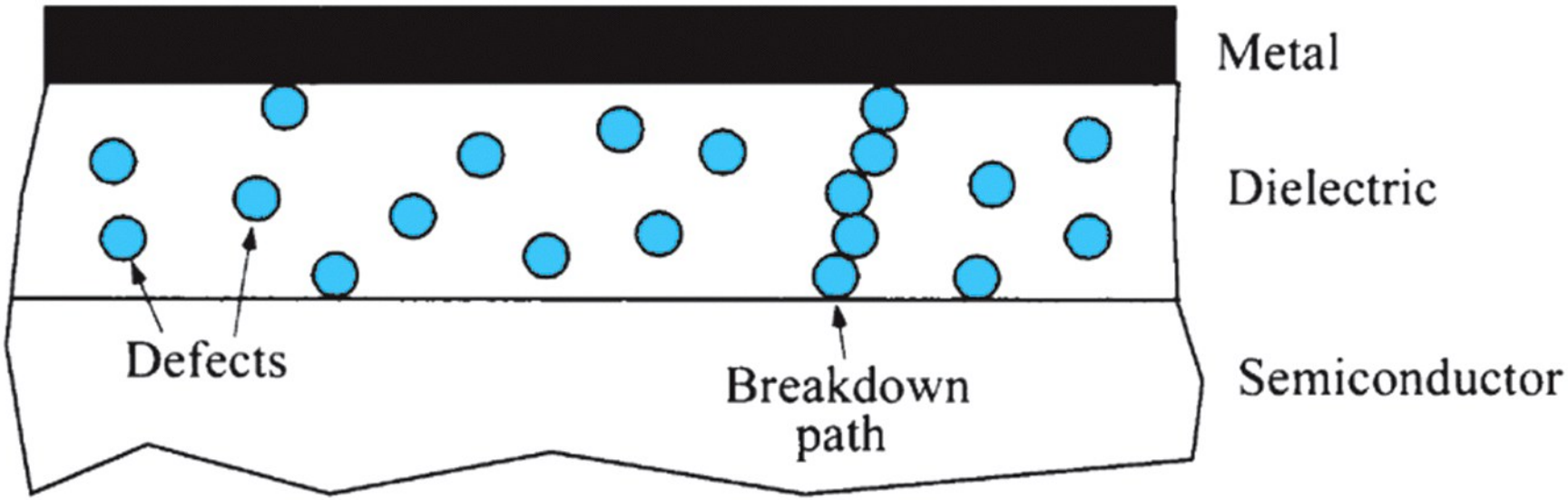


Figure 5.16

Percolation theory

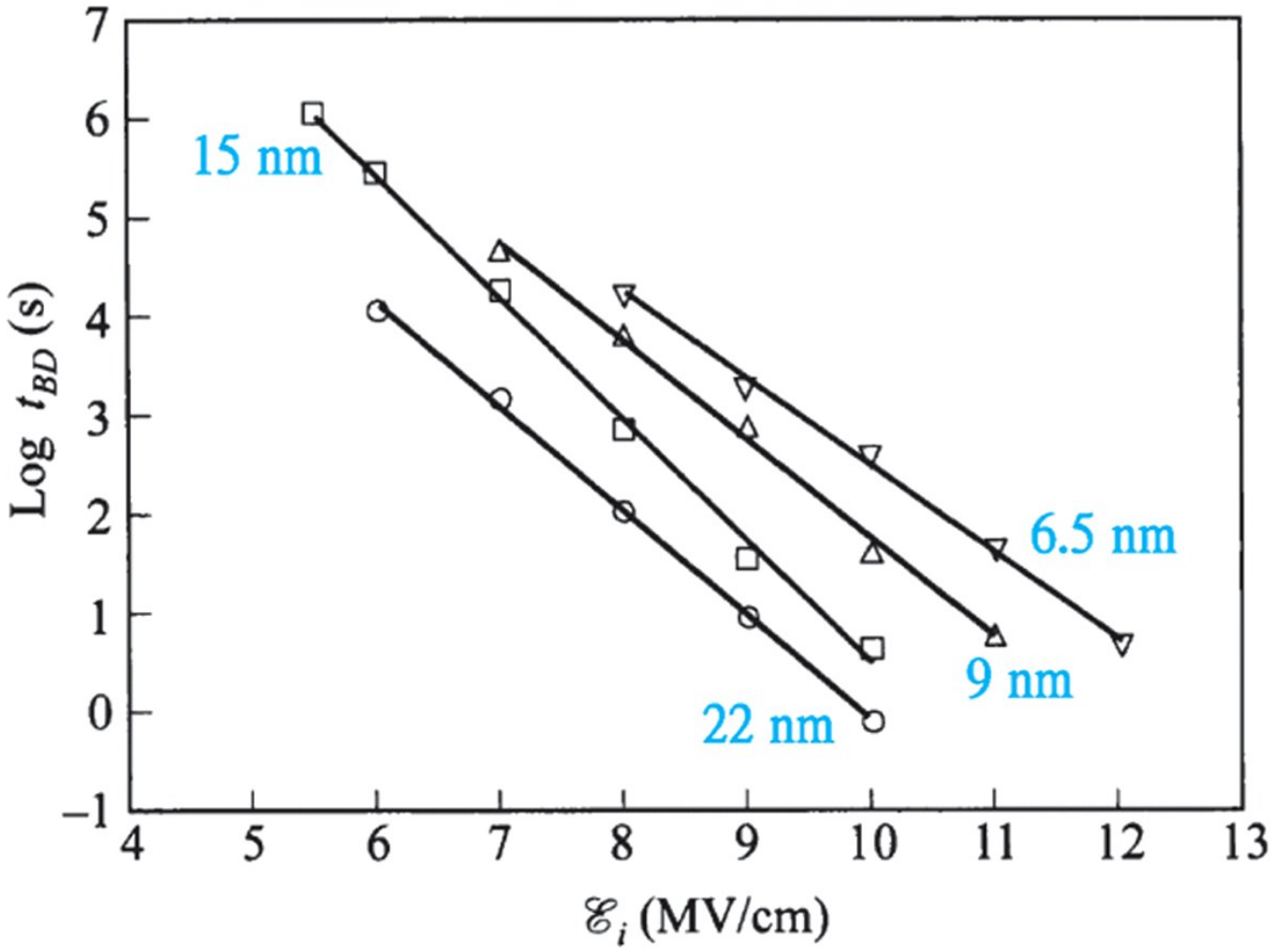


Figure 5.17

Time to breakdown vs oxide field for various thicknesses

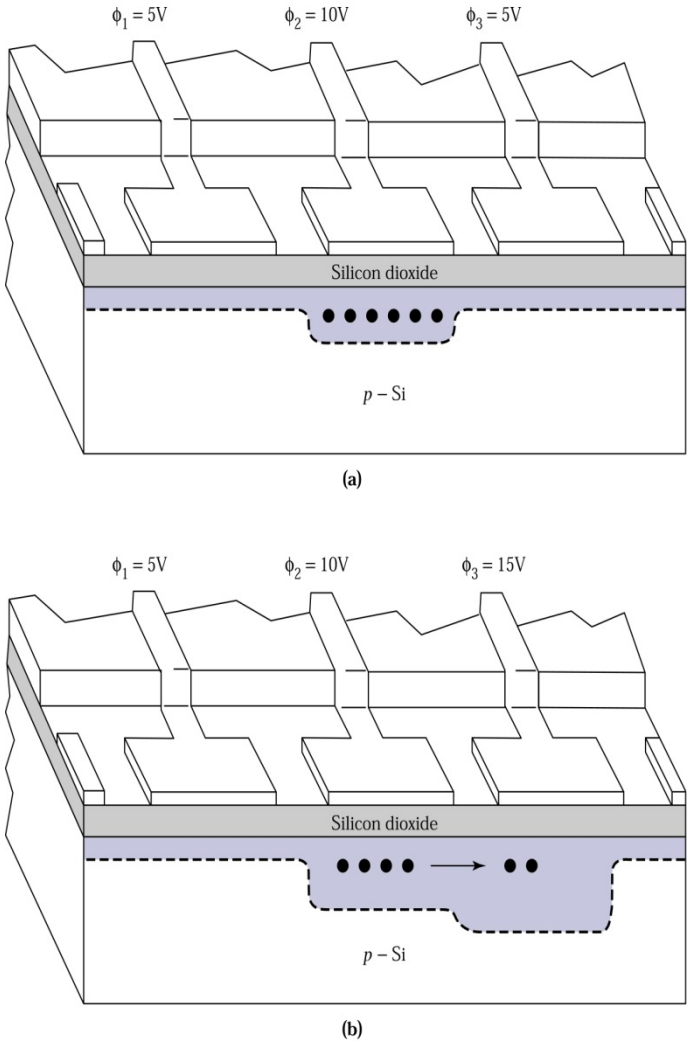


Image sensing
Signal processing

Figure 5.18. Cross section of a three-phase charge-coupled device.[4] (*a*) High voltage on $ø_2$. (*b*) $ø_3$ pulsed to a higher voltage for charge transfer.

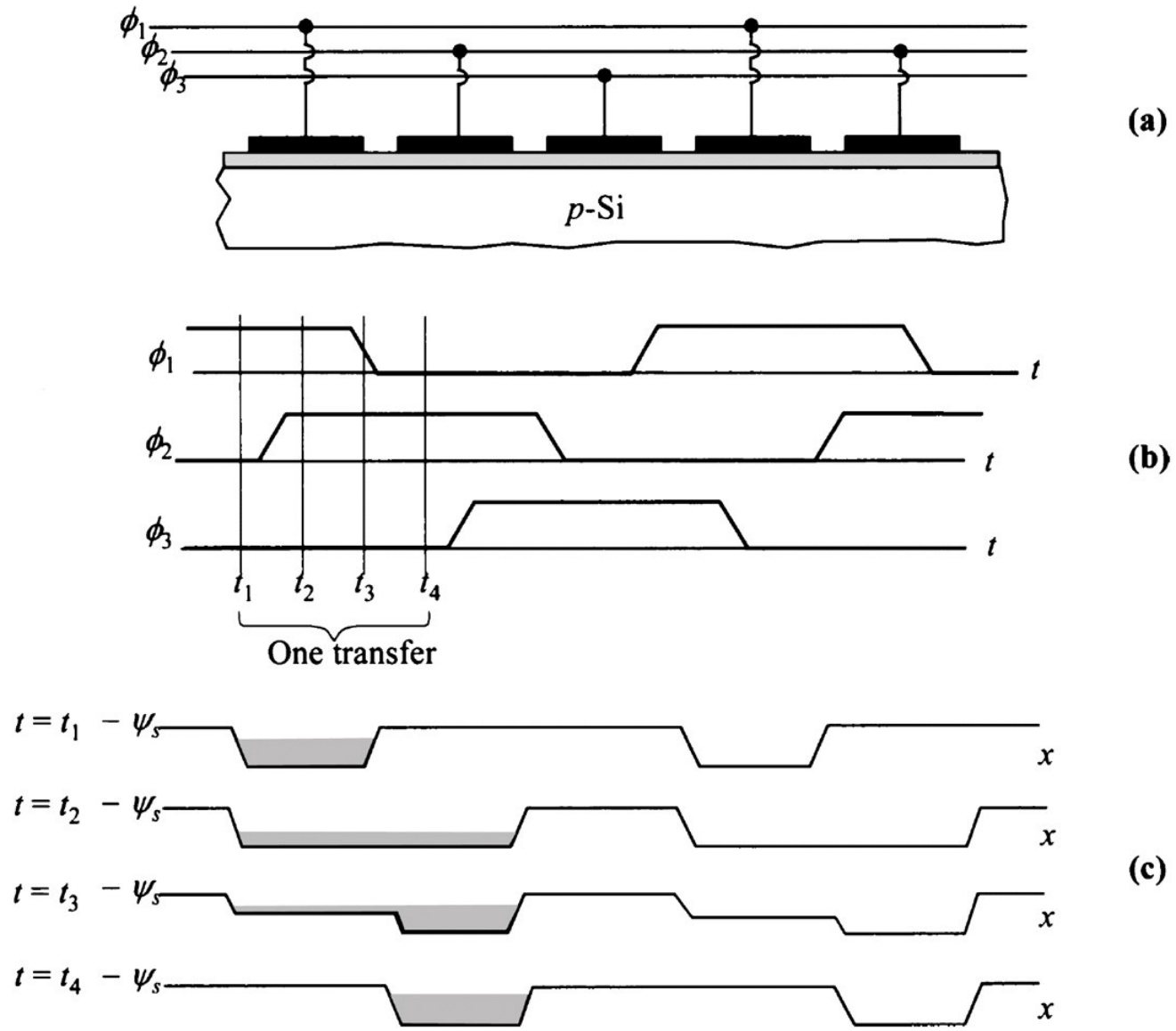


Figure 5.19

CCD charge transfer, (a) three-phase gate bias, (b)clock

Readout mechanisms,

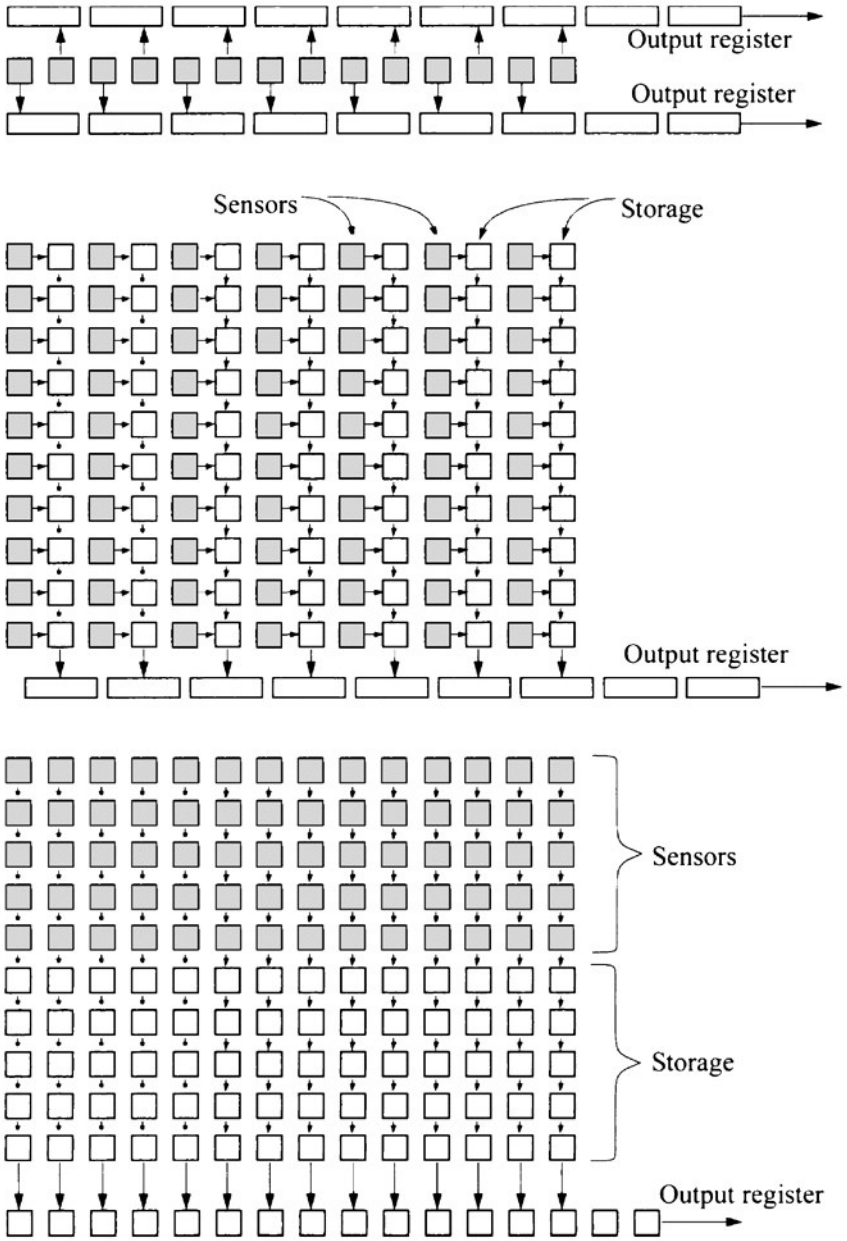
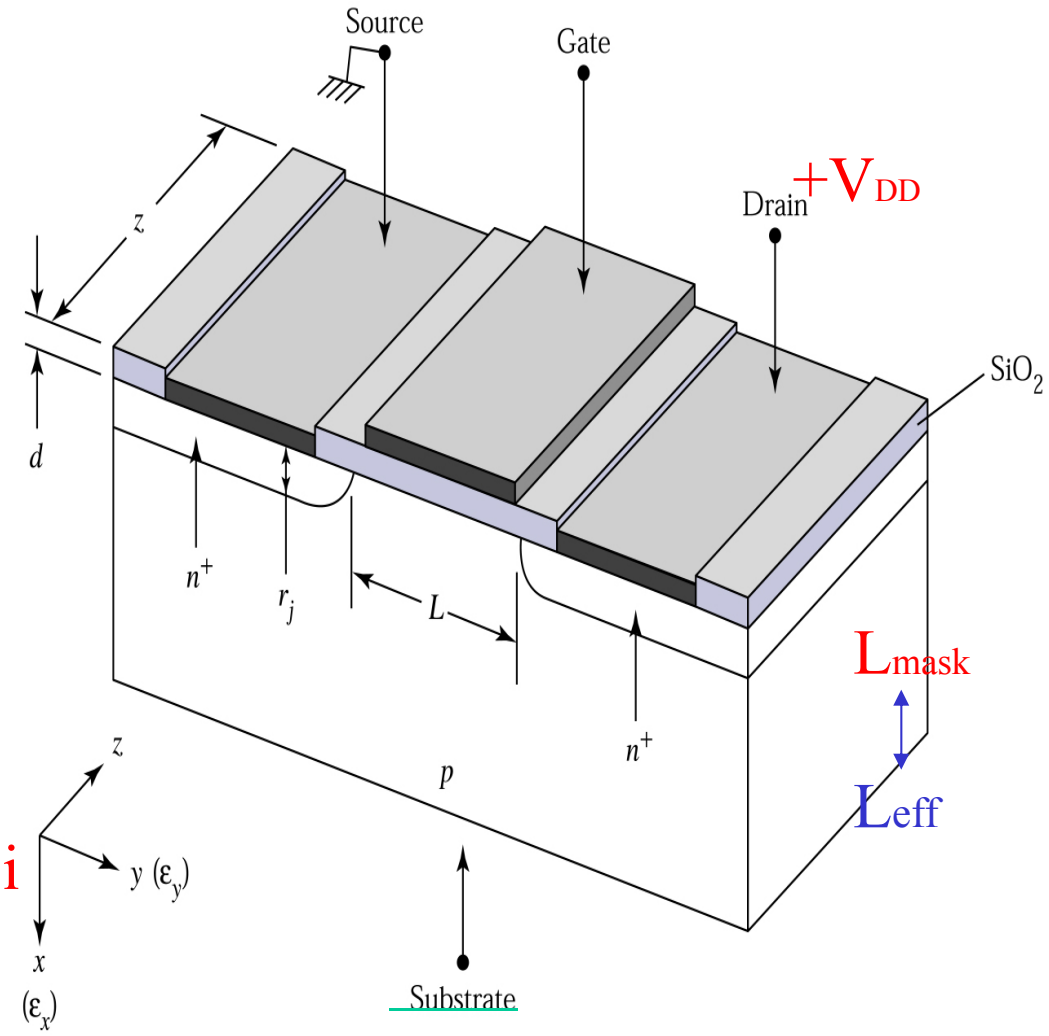


Figure 5.20

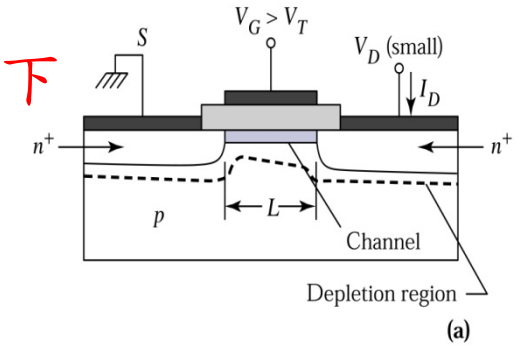
*為4-terminal
*L為D到S之長度
(與Gate無關)
*中間部分,
即為MOS capacitor

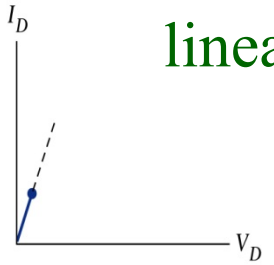


*Gate 為poly-Si,silicide/poly-Si
(n+) (n+)
*S,D為n+/p junction

Figure 5.21. Perspective view of a metal-oxide-semiconductor field-effect transistor (MOSFET).

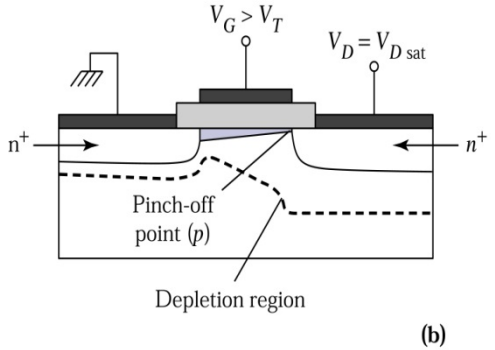
Given,fixed V_G下

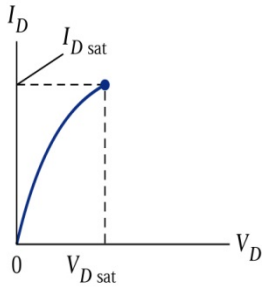


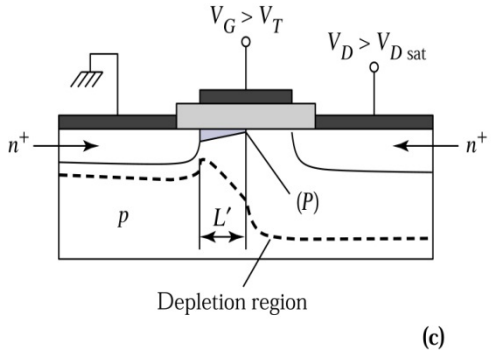


linear

Figure 5.22.
Operations of the MOSFET and output *I-V* characteristics. (*a*) Low drain voltage. (*b*) Onset of saturation. Point *P* indicates the pinch-off point. (*c*) Beyond saturation.

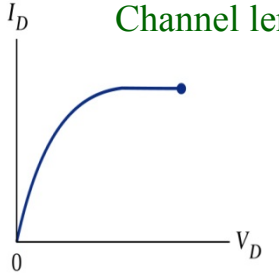






*L'<L

Channel length↓



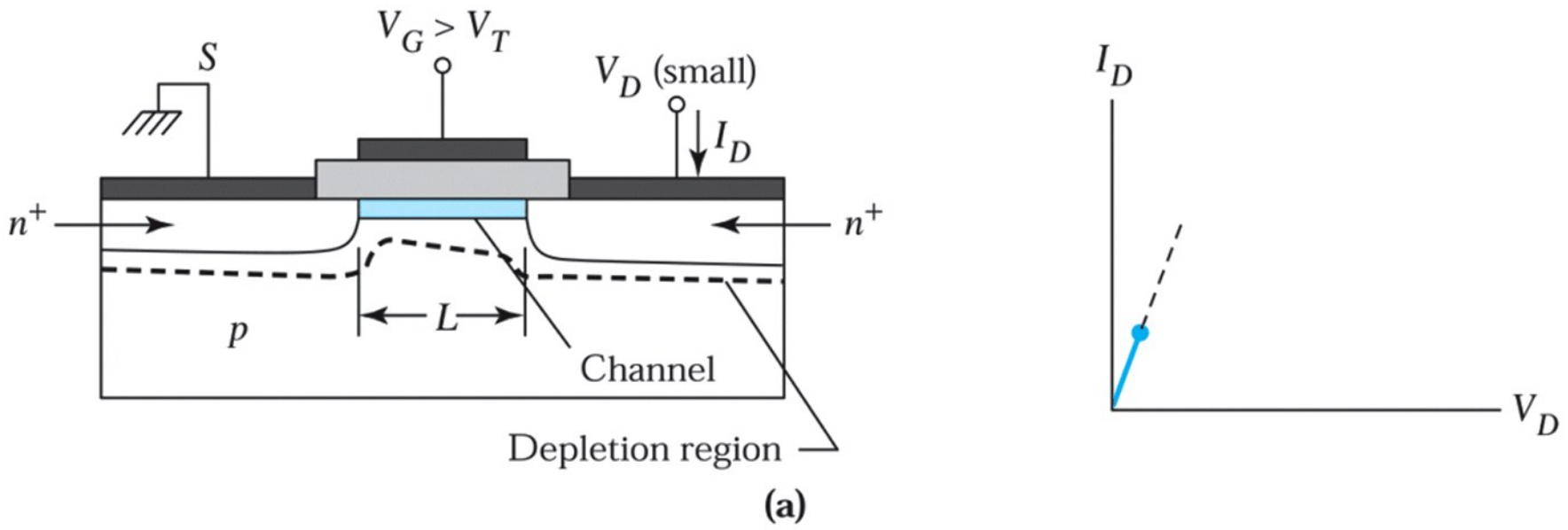


Figure 5.22a

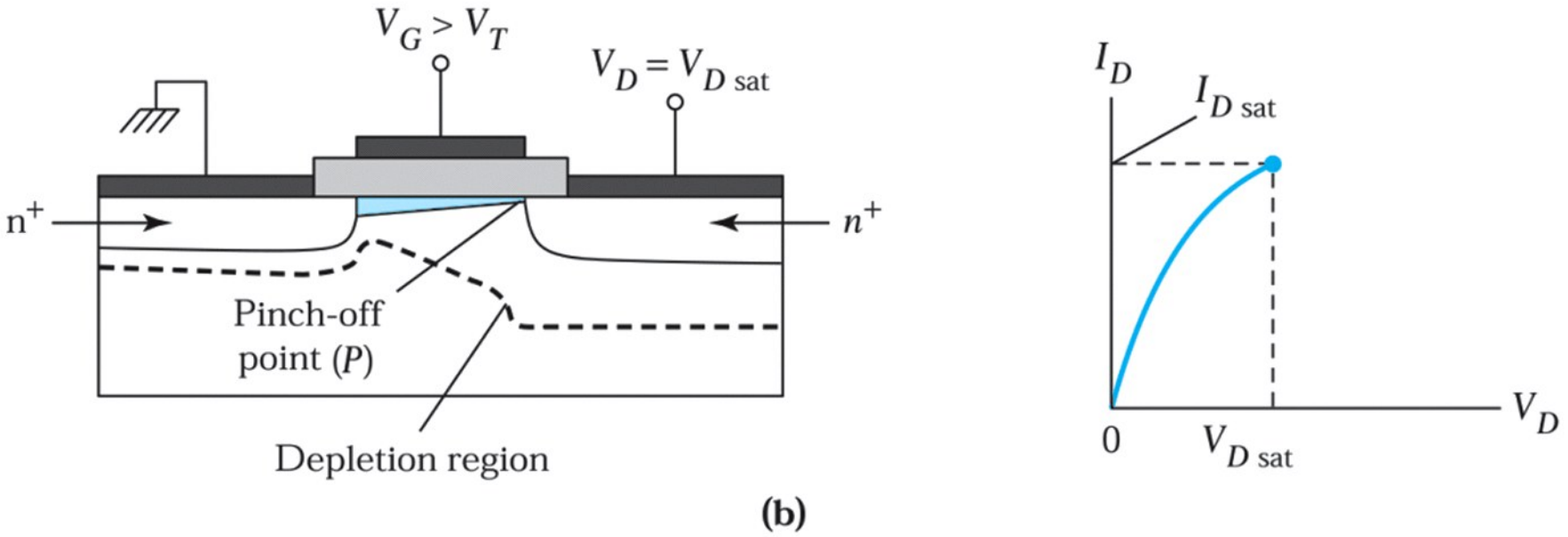


Figure 5.22b

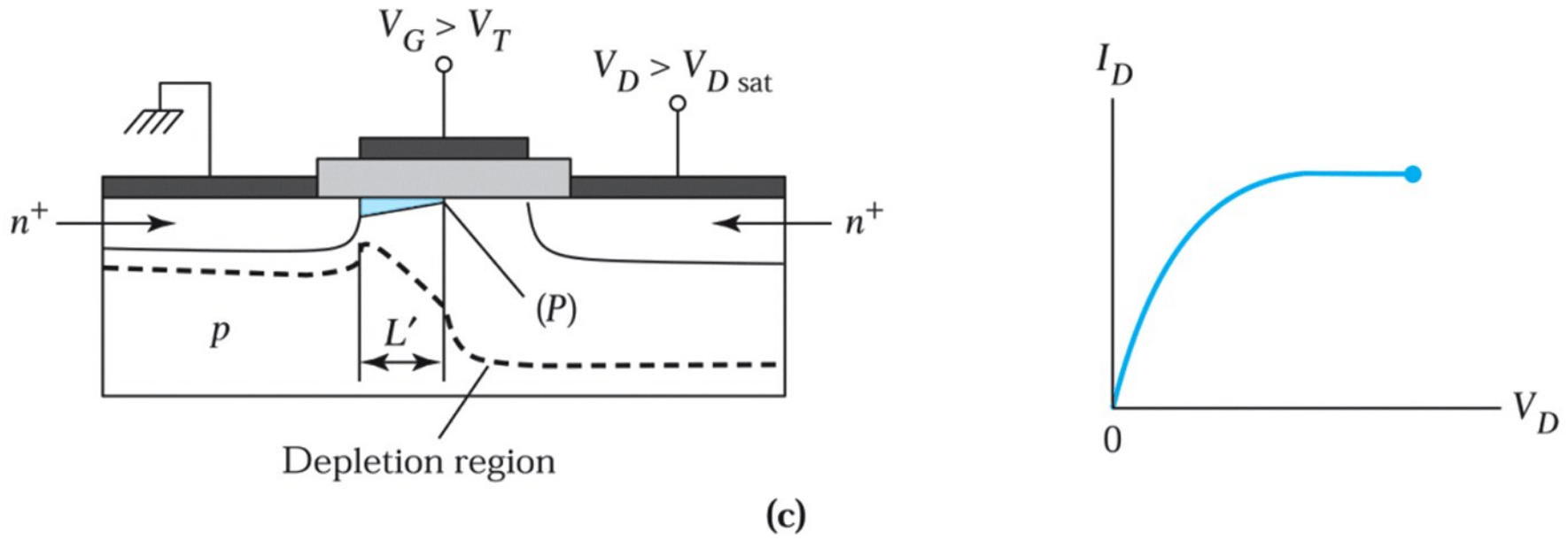


Figure 5.22c

以下推導Io vs VD之general eq.

參考Fig.16

Vo

(-Qs/Co=Vo)

$$Q_s(y) = -[V_G - \psi_s(y)]C_o \qquad (24)$$

感應在半導體內,單位面積電荷

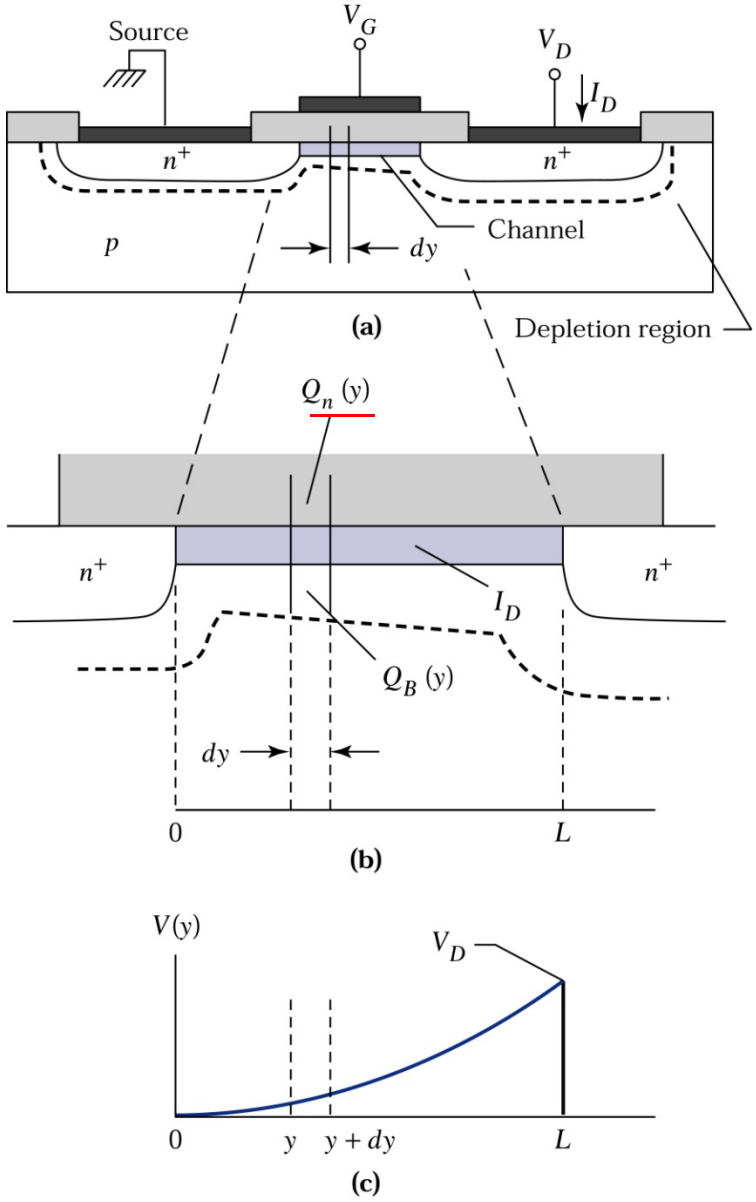
Depletion region

$$Q_n(y) = Q_s(y) - Q_{sc}(y)$$
$$= -[V_G - \psi_s(y)]C_o - Q_{sc}(y). \qquad (25)$$

∵inv. Ψs(y)～2φB+V(y)

$$Q_{sc}(y) = -qN_A W_m \simeq -\sqrt{2\epsilon_s qN_A[V(y) + 2\psi_B]}. \qquad (26)$$

Figure 5.23.
(*a*) MOSFET operated in the linear region. (*b*) Enlarged view of the channel. (*c*) Drain voltage drop along the channel.



$$Q_n(y) \simeq -[V_G - V(y) - 2\psi_B]C_o + \sqrt{2\epsilon_s q N_A [V(y) + 2\psi_B]}. \qquad (27)$$

$$\sigma(x) = qn(x)\mu_n(x). \qquad (28)$$

p.53 (14)

$$g = \frac{Z}{L}\int_0^{x_i} \sigma(x)\,dx = \frac{Z\mu_n}{L}\int_0^{x_i} qn(x)\,dx. \qquad (29)$$

$$g = \frac{Z\mu_n}{L}|Q_n|. \qquad (30)$$

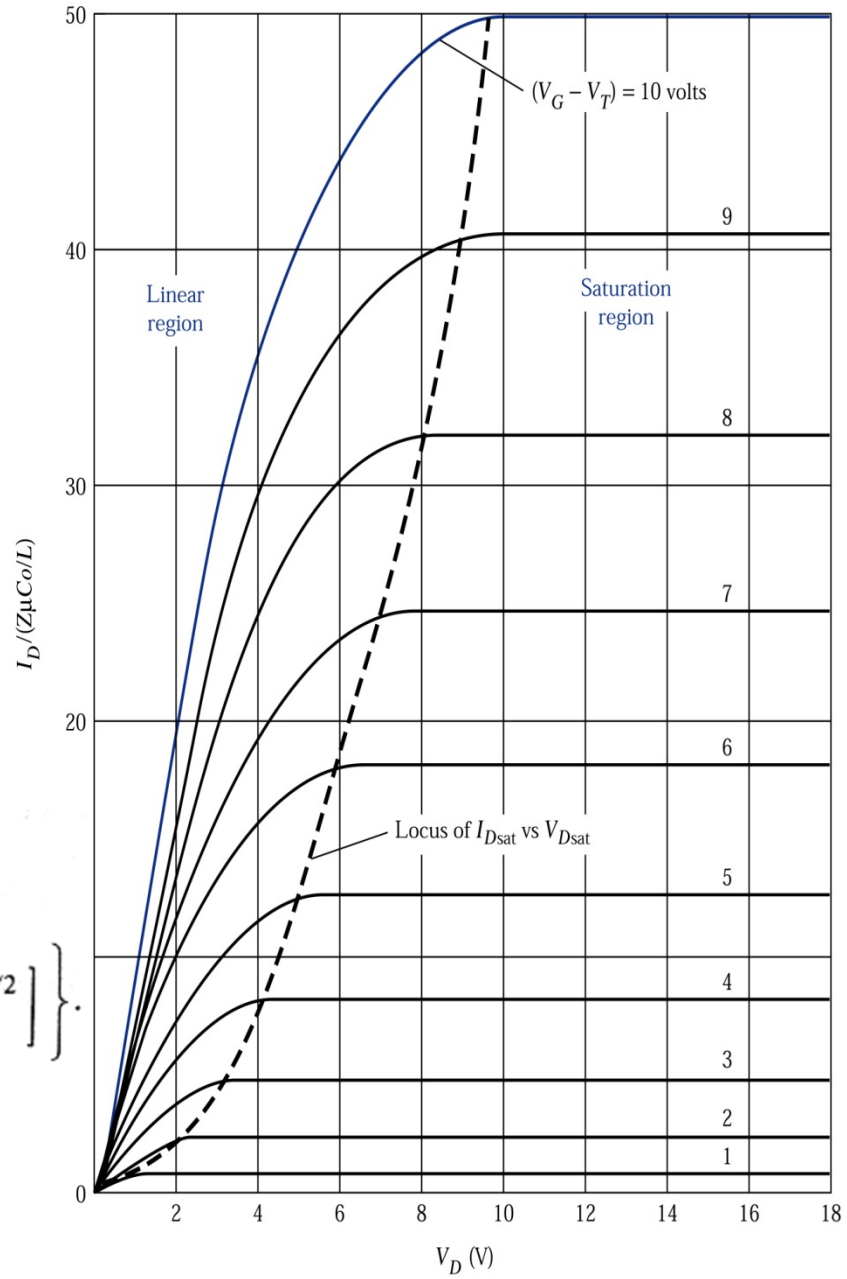
dy/dR= L/(1/g)

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n |Q_n(y)|} \qquad (31)$$

i不變

$$dV = I_D\,dR = \frac{I_D\,dy}{Z\mu_n |Q_n(y)|} \qquad (32)$$

Figure 5.24.
Idealized drain characteristics of a MOSFET. For $V_D \geq V_{Dsat}$, the drain current remains constant.



I_D vs V_D之general eq.

$$I_D \simeq \frac{Z}{L}\mu_n C_o \left\{ \left[V_G - 2\psi_B - \frac{V_D}{2} \right] V_D - \frac{2}{3}\frac{\sqrt{2\epsilon_s q N_A}}{C_o} \left[(V_D + 2\psi_B)^{3/2} - (2\psi_B)^{3/2} \right] \right\}. \quad (33)$$

Linear:

V_D很小時,(33)可化成: $I_D = \frac{Z}{L}\mu_n C_o[(V_G - V_T)V_D - (\frac{1}{2} + \frac{\sqrt{\varepsilon_s q N_A / \Phi_B}}{4C_O})V_D^2]$

$$I_D \simeq \frac{Z}{L}\mu_n C_o(V_G - V_T)V_D \quad \text{for } V_D \ll (V_G - V_T) \qquad (34)$$

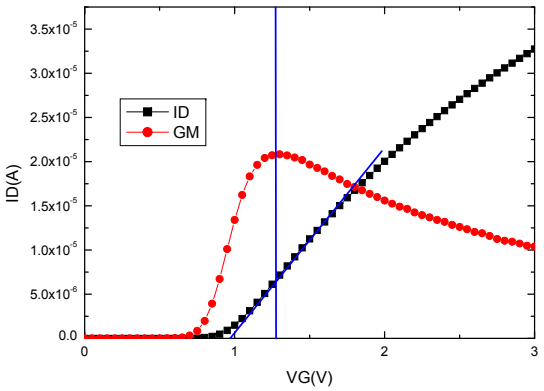
:linear relation/線性區

$$V_T \simeq \frac{\sqrt{2\epsilon_s q N_A (2\psi_B)}}{C_o} + 2\psi_B . \qquad (35)$$

*For small V_D(0.1,0.05),I_D vs V_G 曲線之切線即為V_T

$$g_D \equiv \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G=\text{const}} \simeq \frac{Z}{L}\mu_n C_o(V_G - V_T) \qquad (36)$$

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{const}} \simeq \frac{Z}{L}\mu_n C_o V_D . \qquad (37)$$



Sat.*pinch off ≡$Q_{n(L)}$=0 , 令(27)=0得

$$V_{Dsat} \simeq V_G - 2\psi_B + K^2\left[1 - \sqrt{1 + 2V_G/K^2}\right] \qquad (38)$$

*(38)代入(33)

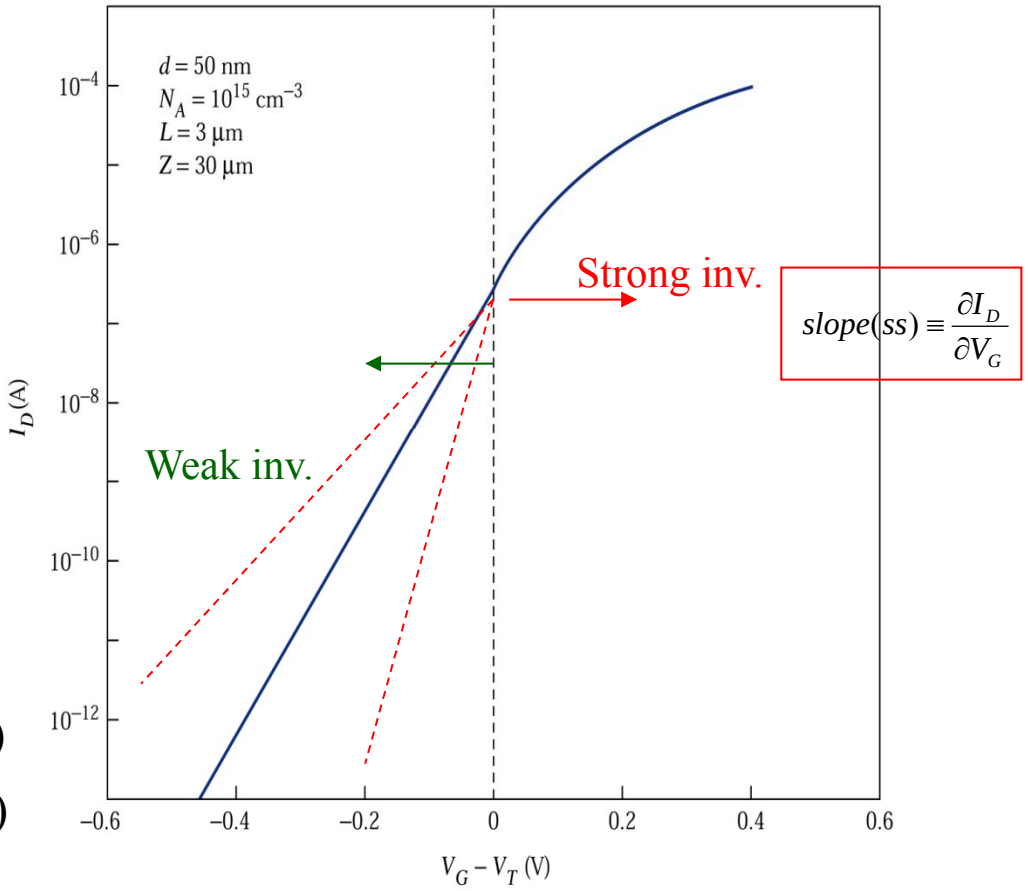
$$I_{D\,sat} \simeq \frac{Z\mu_n\epsilon_{ox}}{2dL}(V_G - V_T)^2 . \qquad (39)$$

$g_{D=0}$

$$g_m \equiv \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D=\text{const}} = \frac{Z\mu_n\epsilon_{ox}}{dL}(V_G - V_T) . \qquad (40)$$

Tox

Figure 5.25. Subthreshold characteristics of a MOSFET.



***MOSFET做為switch時,特別重要**

Subthreshold: surface at weak inversion
Id is dominated by diffusion current

$$I_D = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L)}{L} \qquad (41)$$

***因為尚未strong inv. ,電流以diff.為主**

$$n(0) = n_i e^{q(\psi_s - \psi_B)/kT} \qquad (42a)$$

$$n(L) = n_i e^{q(\psi_s - \psi_B - V_D)/kT} \qquad (42b)$$

$$I_D = \frac{qAD_n n_i e^{-q\psi_B/kT}}{L}(1 - e^{-qV_D/kT})e^{q\psi_s/kT}. \qquad (43)$$

$$I_D \sim e^{q(V_G - V_T)/kT}. \qquad (44)$$

$\Psi_S \approx K(V_G - V_T)$

$\longleftrightarrow$ **Log I_D vs $(V_G - V_T)$為直線**

$\Psi_s \approx K(V_G - V_T)$

請參考 p.446, SM Sze, Physics of Semiconductor Devices (大施敏)

where we have used the relation $D_n = \mu_n kT/q$, and a is given by Eq. 33. The surface potential ψ_s is related to the gate voltage as follows:[18,19]

$$\psi_s = (V_G - V_{FB}) - \frac{a^2}{2\beta}\left\{\left[1 + \frac{4}{a^2}(\beta V_G - \beta V_{FB} - 1)\right]^{1/2} - 1\right\}. \quad (41)$$

$$a \equiv \sqrt{2}(\epsilon_s/L_D)/C_i = 2(\epsilon_s/\epsilon_i)(d/L_D). \quad (33)$$

$$\beta = \frac{KT}{q}$$

18 J. R. Brews, "A Charge-Sheet Model of the MOSFET," *Solid State Electron.*, **21**, 345 (1978).

19 J. R. Brews, "Subthreshold Behavior of Uniformly and Nonuniformly Doped Long-Channel MOSFET," *IEEE Trans. Electron Devices*, **ED-26**, 1282 (1979).

*enhancement mode為主

N

P

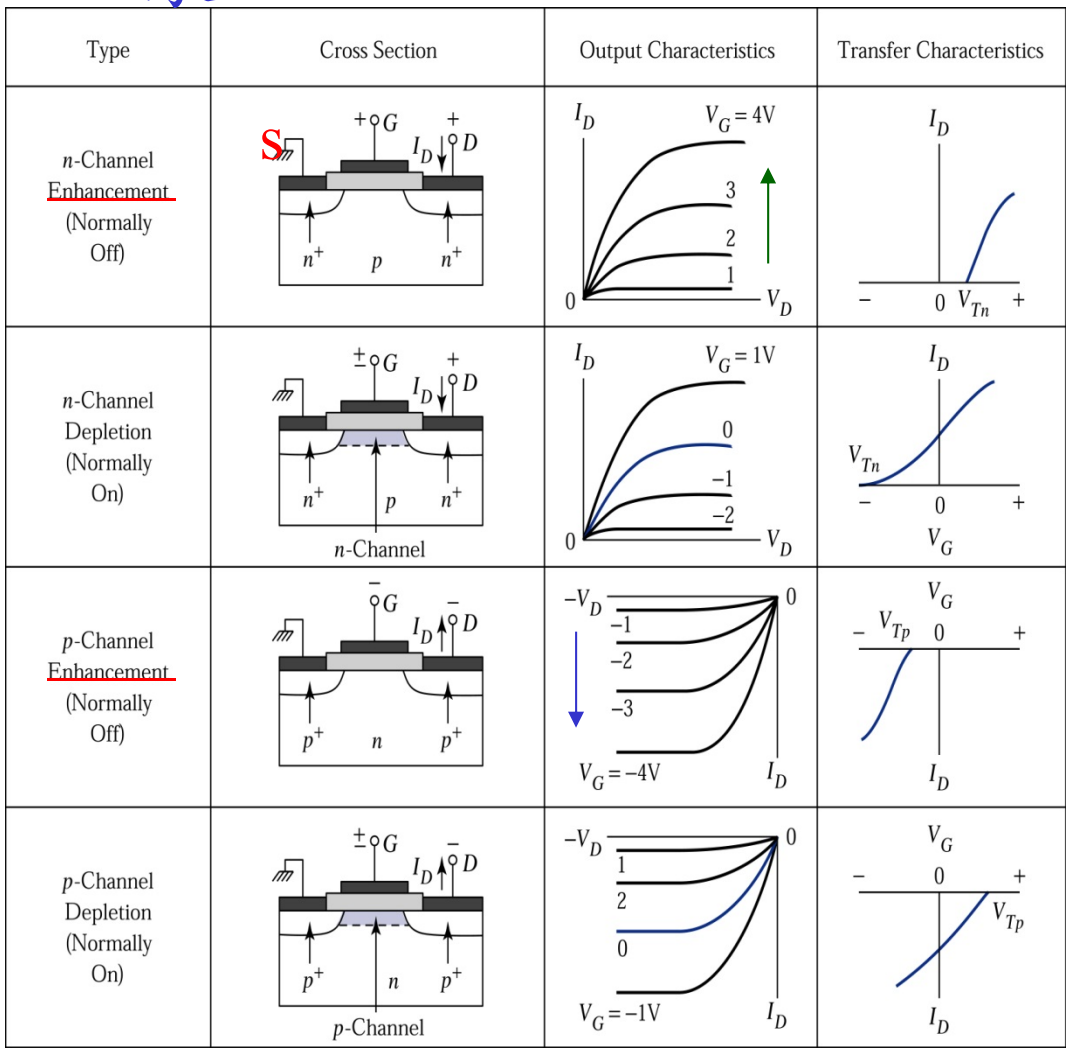


Figure 5.26. Cross section, output, and transfer characteristics of four types of MOSFETs.

Threshold Voltage Control

$$V_T \simeq V_{FB} + 2\psi_B + \frac{\sqrt{2\epsilon_s q N_A (2\psi_B)}}{C_o} \quad (Qn \uparrow + Qsc)$$

$$= \left[\phi_{ms} - \frac{Q_f}{C_o} \right] + 2\psi_B + \frac{\sqrt{4\epsilon_s q N_A \psi_B}}{C_o} \qquad (45)$$

故使用 ion-implant, 改變 Substrate doping,而調V_{T0}

$N_B \uparrow$ 得

- n-sub, $|\Phi ms|$ ↓
- p-sub, $|\Phi ms|$ ↑

($\Phi ms<0$)

得V_T ↑ p-ch ; ↓ n-ch

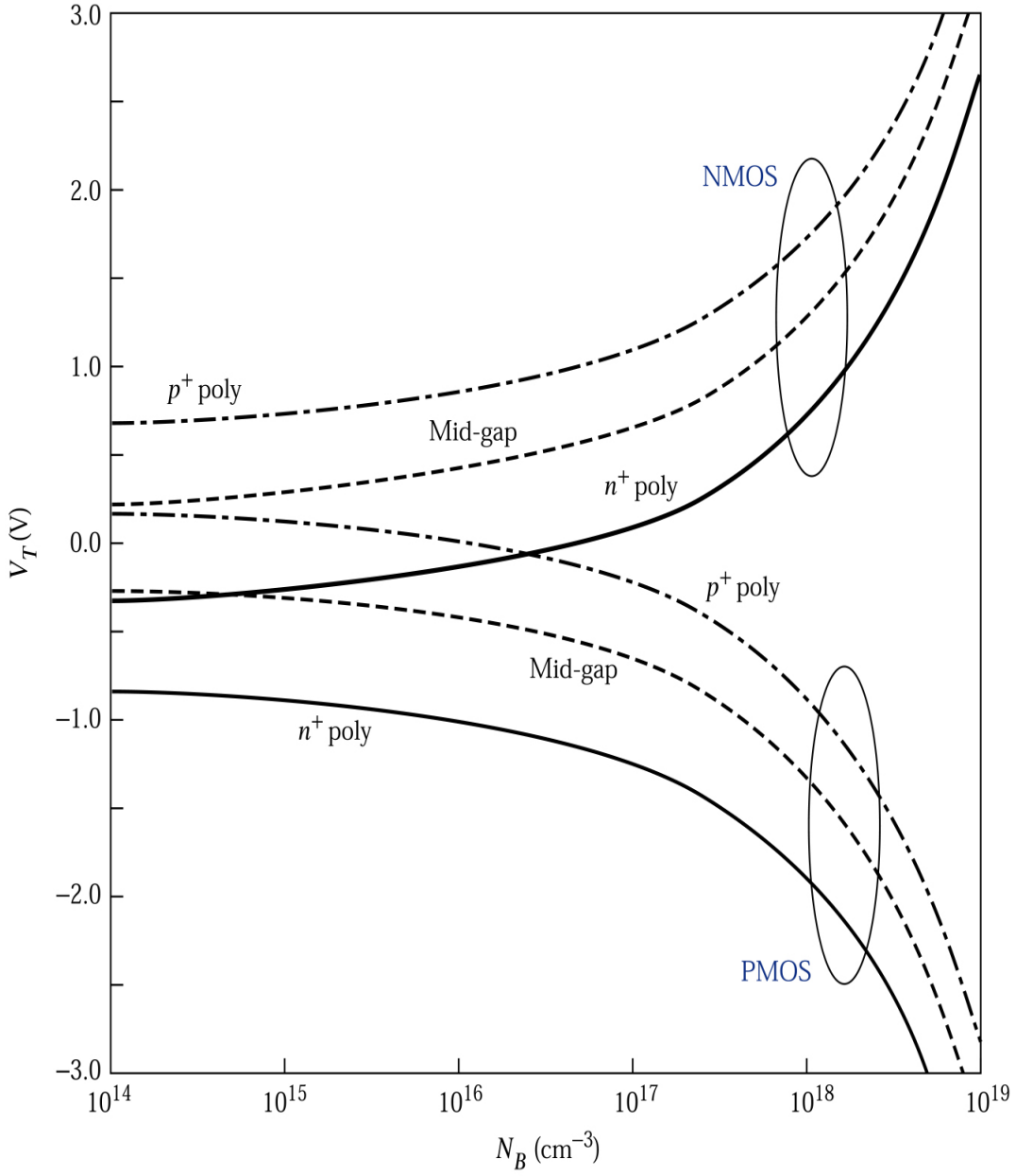
$N_B \uparrow$ 得

$|\Psi_B|$
- n-sub<0
- p-sub>0

得V_T ↓↓ p-ch ; ↑↑ n-ch

$\Psi_B \equiv Ei - E_F$

Figure 5.27.
Calculated threshold voltage of *n*-channel (V_{Tn}) and *p*-channel (V_{Tp}) MOSFETs as a function of impurity concentration, for devices with n^{+-}, p^{+}–polysilicon, and mid-gap work function gates assuming zero fixed charge. The thickness of the gate oxide is 5 nm. NMOS, *n*-channel MOSFET; PMOS, *p*-channel MOSFET.



EXAMPLE 6

For an n-channel n^+-polysilicon-SiO_2-Si MOSFET with $N_A = 10^{17}$ cm^{-3} and $Q_f/q = 5 \times 10^{11}$ cm^{-2}, calculate V_T for a gate oxide of 5 nm. What is the boron ion dose required to increase V_T to 0.6 V? Assume that the implanted acceptors form a sheet of negative charge at the Si-SiO_2 interface.

SOLUTION From the examples in Section 6.1, we have $C_o = 6.9 \times 10^{-7}$ F/cm^2, $2\psi_B = 0.84$ V, $V_{FB} = -1.1$ V. Therefore, from Eq. 45 (with $V_{BS} = 0$),

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_o}$$

$$= -1.1 + 0.84 + \frac{\sqrt{2 \times 11.9 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 10^{17} \times 0.84}}{6.9 \times 10^{-7}}$$

$$= -0.02 \text{ V}.$$

The boron charge causes a flat-band shift of qF_B/C_o. Thus,

$$0.6 = -0.02 + \frac{qF_B}{6.9 \times 10^{-7}},$$

$$F_B = \frac{0.62 \times 6.9 \times 10^{-7}}{1.6 \times 10^{-19}} = 2.67 \times 10^{12} \text{ cm}^{-2}.$$

EXAMPLE 7

For an n-channel field transistor with $N_A = 10^{17}$ cm^{-3} and $Q_f/q = 5 \times 10^{11}$ cm^{-2}, calculate V_T for a gate oxide (i.e., the field oxide) of 500 nm.

SOLUTION $C_o = \varepsilon_{ox} / d = 6.9 \times 10^{-9}$ F/cm^2.

From Exs. 2 and 3, we have $2\psi_B = 0.84$ V, and $V_{FB} = -1.1$ V.

Therefore, from Eq.45 (with $V_{BS} = 0$)

$$V_T = V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_o}$$

$$= -1.1 + 0.84 + \frac{\sqrt{2 \times 11.9 \times 8.85 \times 10^{-14} \times 1.6 \times 10^{-19} \times 10^{17} \times 0.84}}{6.9 \times 10^{-9}}$$

$$= 24.12 \text{ V}.$$

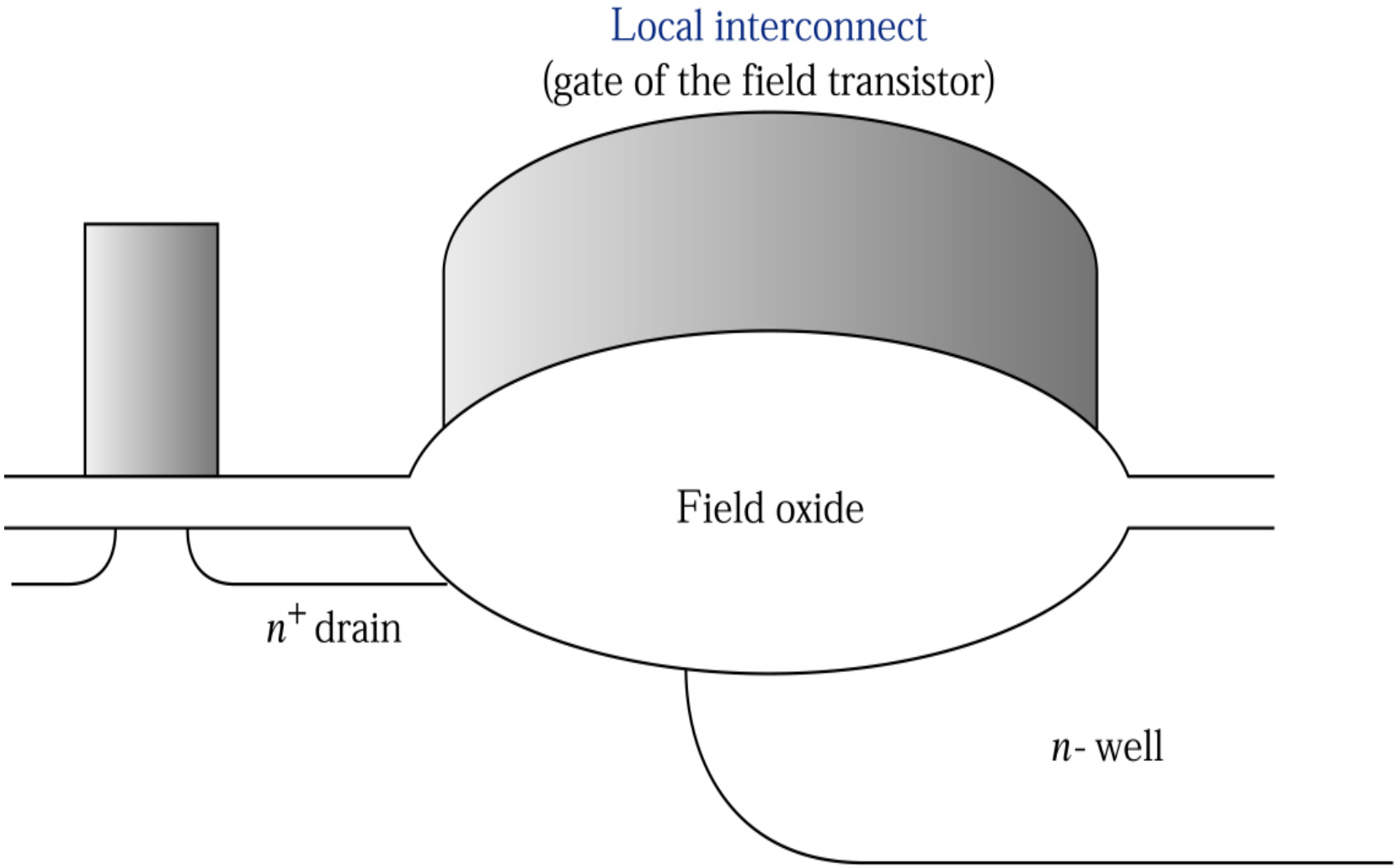


Figure 5.28. Cross section of a parasitic field transistor in an *n*-well structure.

若 Substrate 加反向偏壓 V_{BS}

$$Q_B' = -\sqrt{2q\epsilon_s N_A(2\psi_B + V_{BS})}.$$

Space charge

$$\Delta V_T = \frac{\sqrt{2q\epsilon_s N_A}}{C_o}(\sqrt{2\psi_B + V_{BS}} - \sqrt{2\psi_B}). \quad (46)$$

$\begin{cases} V_{BS} < 0, V_T \text{ 增加}. \\ V_{BS} > 0, V_T \text{ 減少}. \end{cases}$

以 V_{BS} 調 V_T,即 $|V_{BS}| \uparrow \longrightarrow V_T \uparrow$

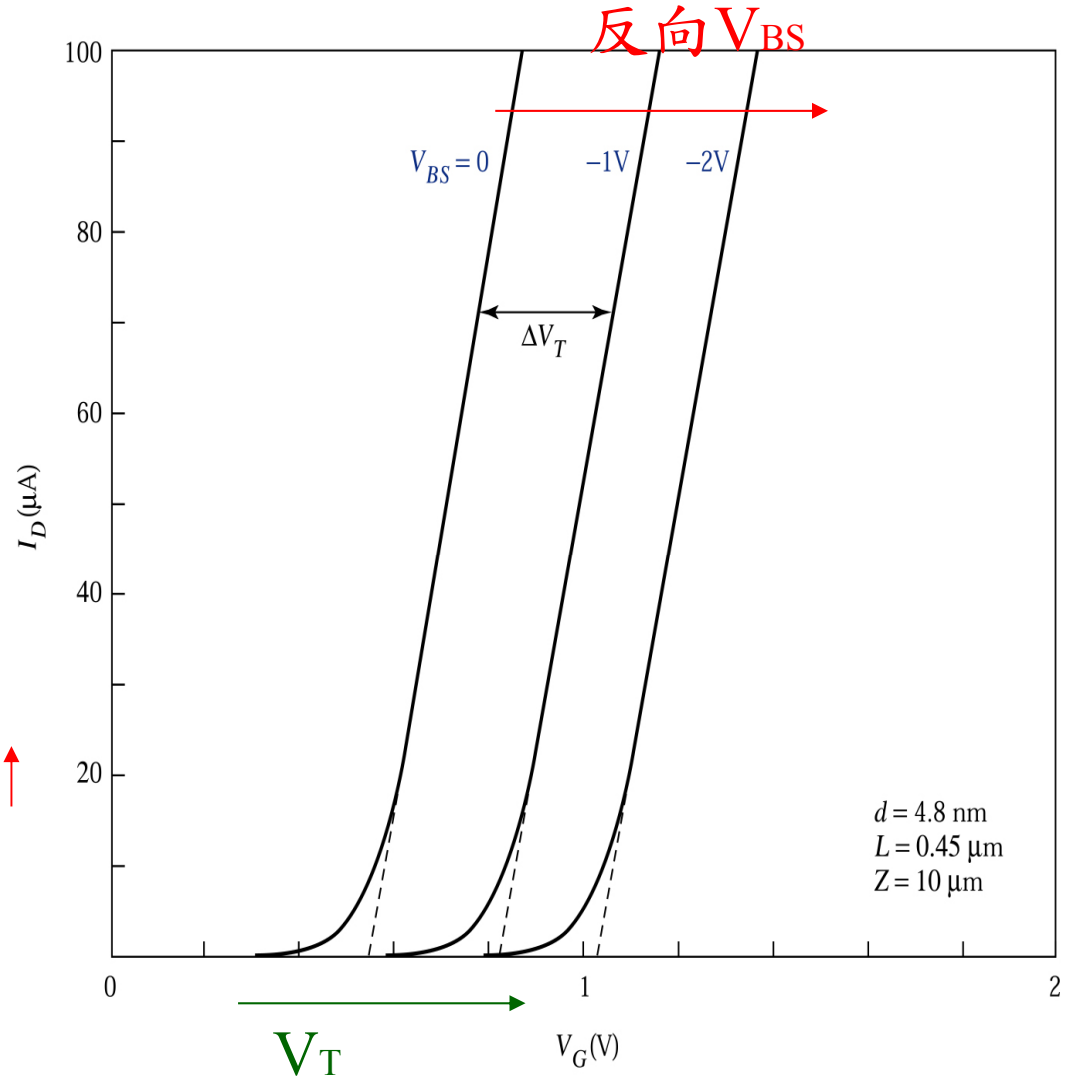
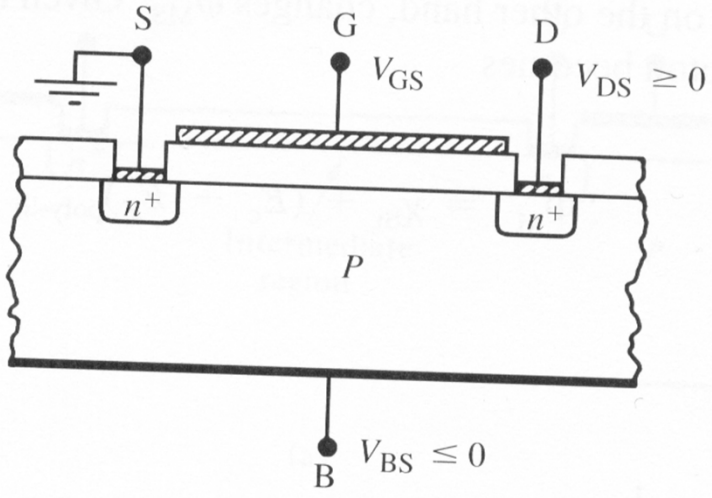
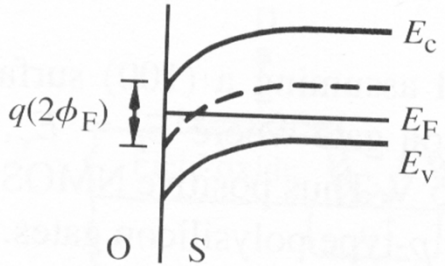


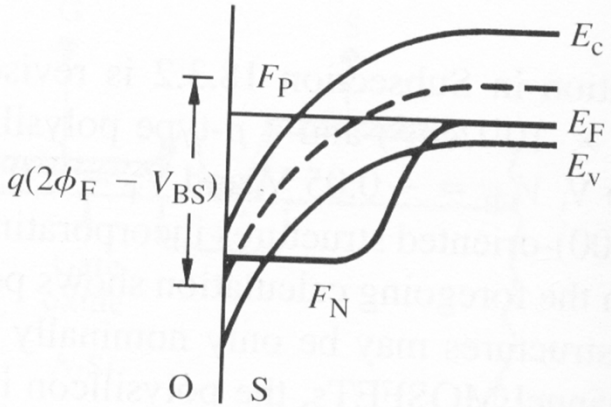
Figure 5.29. Threshold voltage adjustment using substrate bias.


S
G
D
V_{GS}
$V_{DS} \geq 0$
n^+
n^+
P
B
$V_{BS} \leq 0$

(a)


E_c
$q(2\phi_F)$
E_F
E_v
O
S

(b)


E_c
F_P
E_F
E_v
$q(2\phi_F - V_{BS})$
F_N
O
S

(c)