Semiconductor Devices

THIRD EDITION

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Chapter 4

Bipolar Transistors and Related Devices

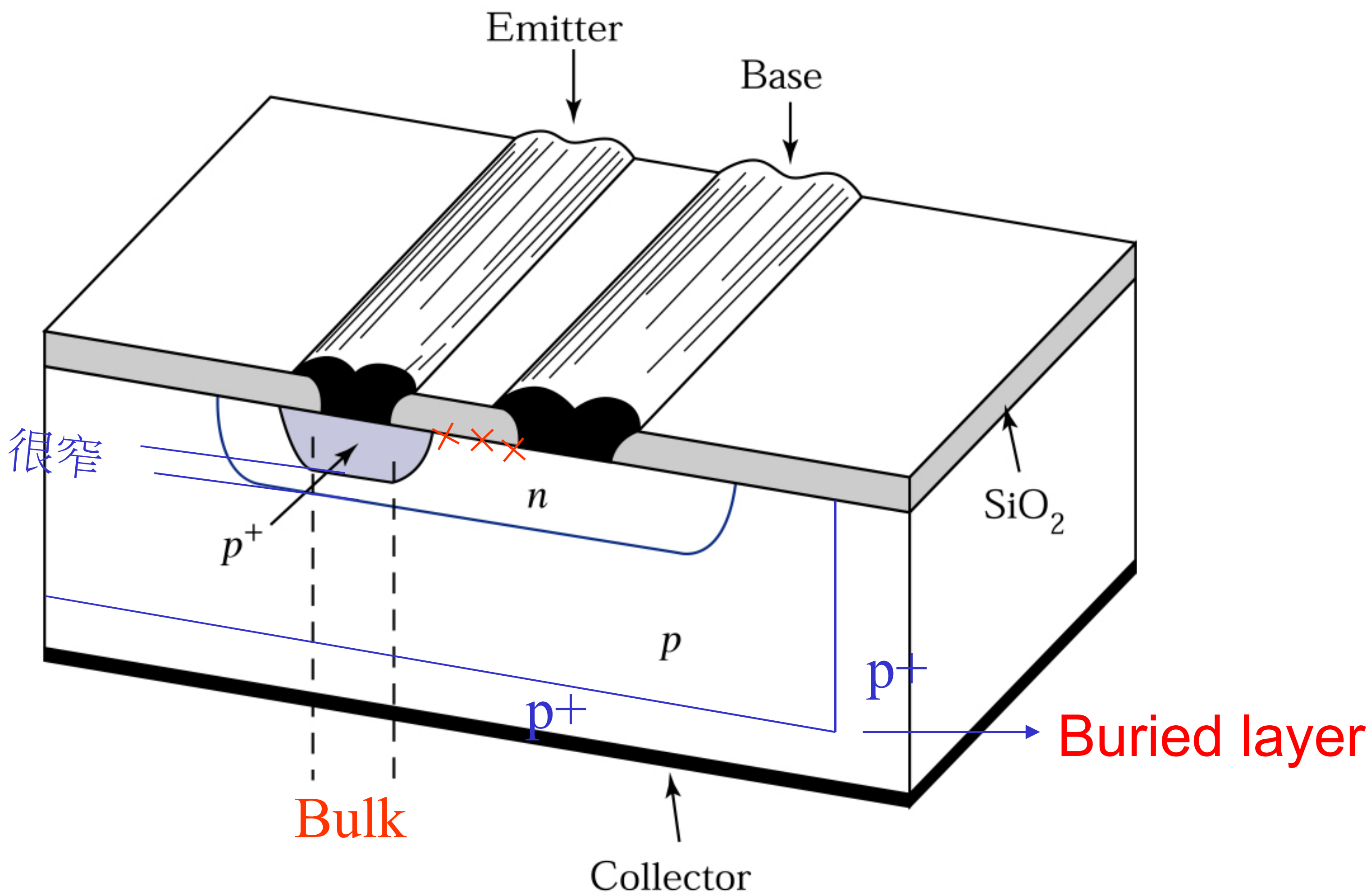
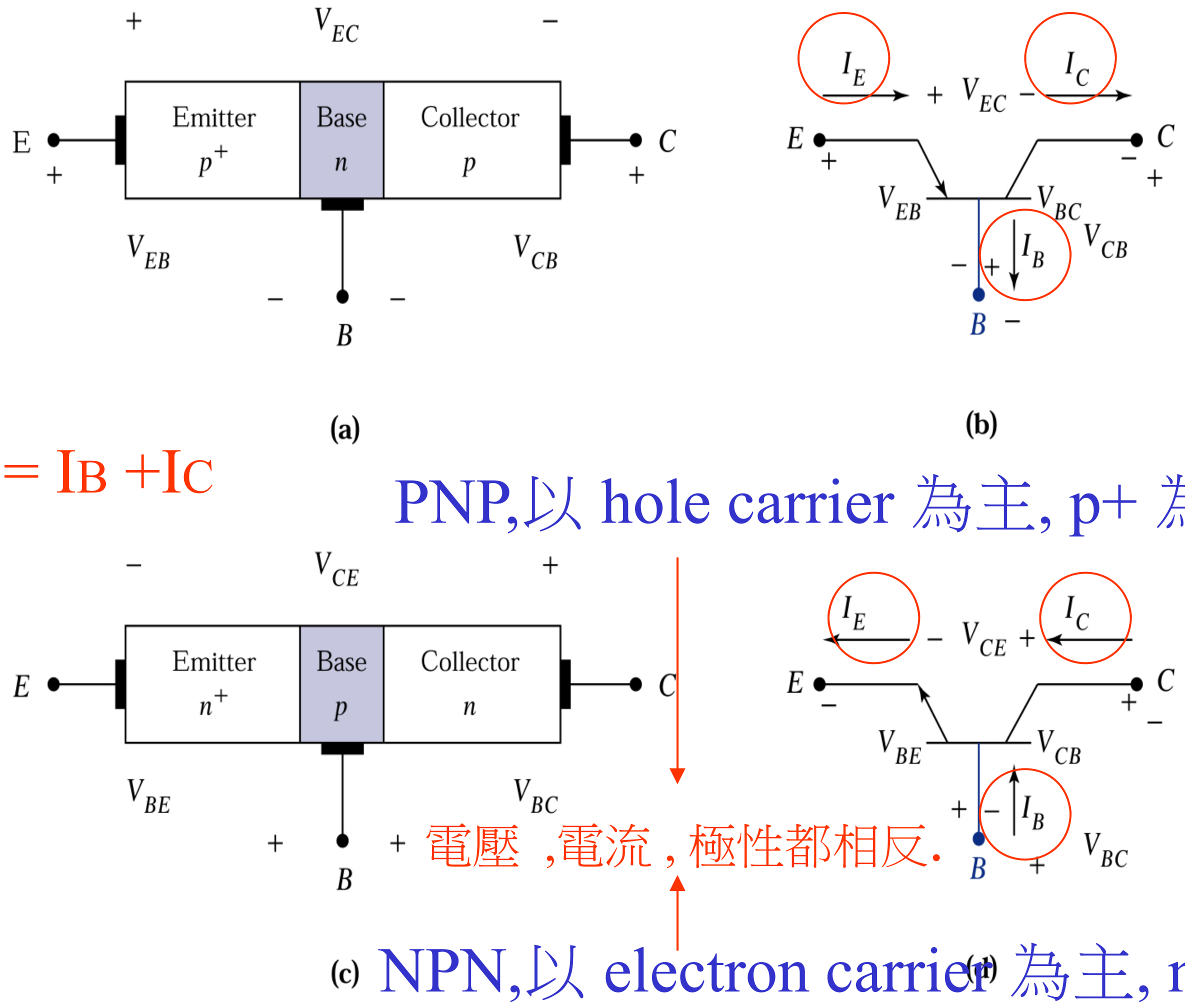


Figure 4.1. Perspective view of a silicon *p*-*n*-*p* bipolar transistor.



$I_E = I_B + I_C$

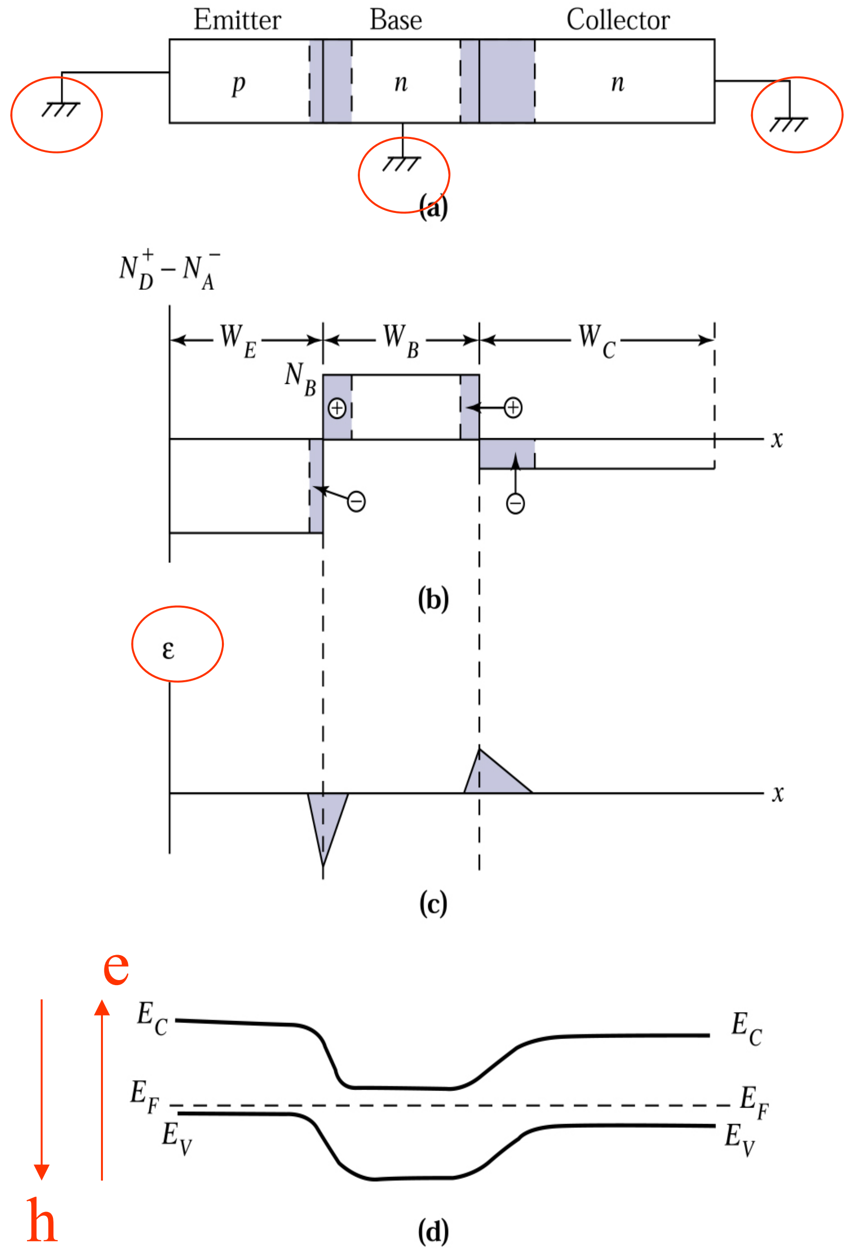
PNP,以 hole carrier 為主, p+ 為 emitter

電壓 ,電流 , 極性都相反.

NPN,以 electron carrier 為主, n+ 為 emitter

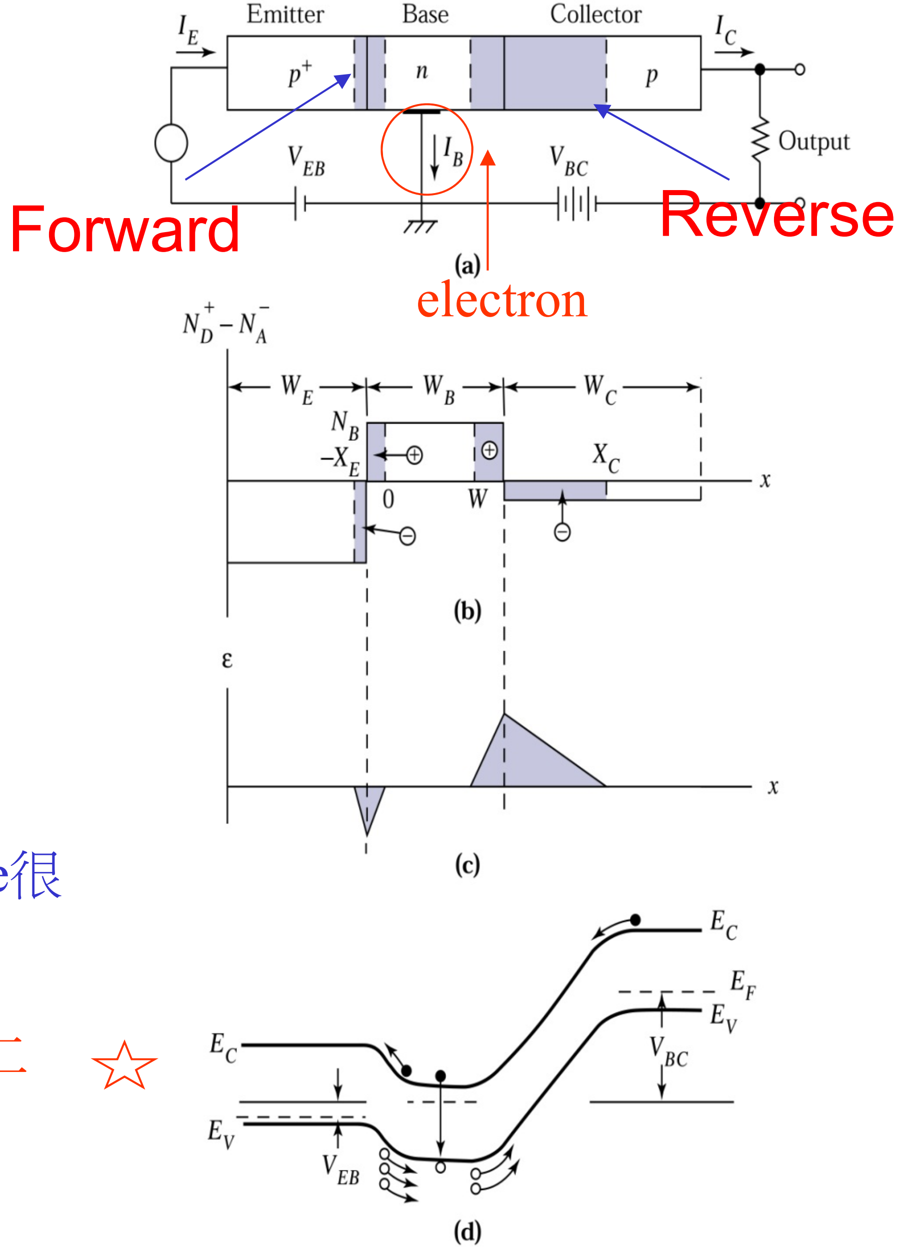
Figure 4.2. (*a*) Idealized one-dimensional schematic of a *p-n-p* bipolar transistor and (*b*) its circuit symbol. (*c*) Idealized one-dimensional schematic of an *n-p-n* bipolar transistor and (*d*) its circuit symbol.

Figure 4.3. (*a*) A *p-n-p* transistor with all leads grounded (at thermal equilibrium). (*b*) Doping profile of a transistor with abrupt impurity distributions. (*c*) Electric-field profile. (*d*) Energy band diagram at thermal equilibrium.



熱平衡,無電流,EF是平的 ☆

Figure 4.4.
(*a*) The transistor shown in Fig. 3 under the **active** mode of operation.[3] (*b*) Doping profiles and the depletion regions under biasing conditions. (*c*) Electric-field profile. (*d*) Energy band diagram.



➢Hole 越過EB junction 後,若 Base很窄,則會大部分被C收集.

➢Base 很寬就不是Transistor,所以二個背對背之Diode不等於Transistor. ☆

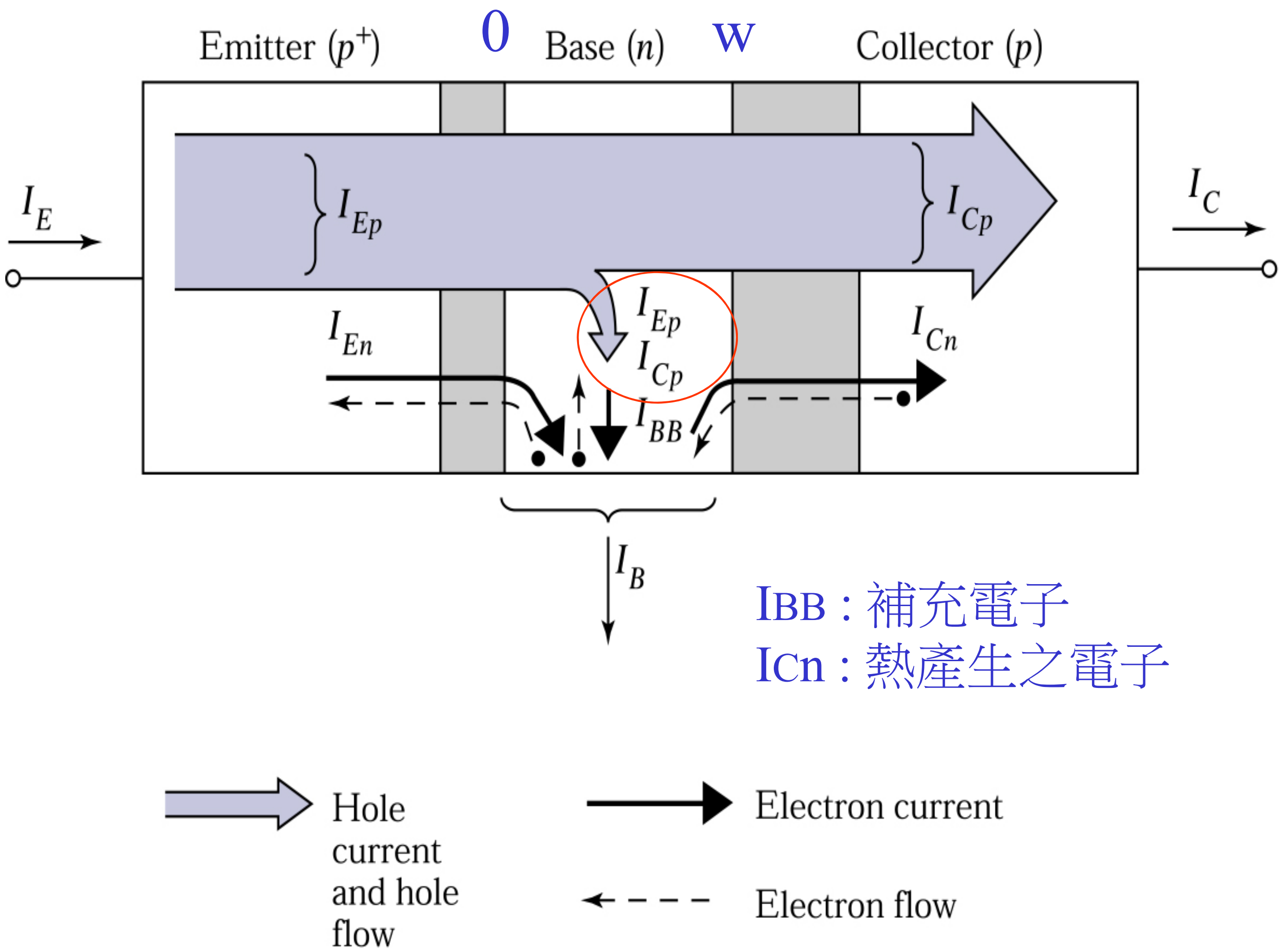


Figure 4.5. Various current components in a *p-n-p* transistor under active mode of operation. The electron flow is in the opposite direction to the electron current.

I_{En} :B到E之電子流,越小越好(p+很濃,heterojunction)

$$I_E = I_{Ep} + I_{En}, \quad (1)$$

$$I_C = I_{Cp} + I_{Cn}, \quad (2)$$

$$I_B = I_E - I_C = I_{En} + (I_{Ep} - I_{Cp}) - I_{Cn}. \quad (3)$$

Common-base current gain :

CB : Ri小,Ro=Rc大,
Current follower.

$$\alpha_0 \equiv \frac{I_{Cp}}{I_E}. \longrightarrow 1 \quad (4)$$

$$\alpha_0 = \frac{I_{Cp}}{I_{Ep} + I_{En}} = \left(\frac{I_{Ep}}{I_{Ep} + I_{En}}\right)\left(\frac{I_{Cp}}{I_{Ep}}\right). \quad (5)$$

➢Emitter efficiency

$$\gamma \equiv \frac{I_{Ep}}{I_E} = \frac{I_{Ep}}{I_{Ep} + I_{En}}. \quad (6)$$

(I_{En} ↓)

➢Base transport factor

$$\alpha_T \equiv \frac{I_{Cp}}{I_{Ep}}. \quad (7)$$

(I_{BB} ↓, W_B ↓, N_B ↓)

$$\alpha_0 = \gamma \alpha_T. \quad (8)$$

CB current gain = (emmitter eff)*(base transport factor)

$$I_C = I_{Cp} + I_{Cn} = \alpha_T I_{Ep} + I_{Cn} = \gamma\alpha_T\left(\frac{I_{Ep}}{\gamma}\right) + I_{Cn} = \alpha_0 I_E + I_{Cn}, \qquad (9)$$

令$I_{Cn} = I_{CB0}$

$$\boxed{I_C = \alpha_0 I_E + I_{CBO}.} \qquad (10)$$

指EB open

Common base

1. The device has uniform doping in each region.
2. The hole drift current in the base region as well as the collector saturation current is negligible.
3. There is low-level injection.
4. There are no generation-combination currents in the depletion regions.
5. There are no series resistances in the device.

Active mode

Continuity eq. for E=0 (Chap 3 eq.(61))

$$D_p\left(\frac{d^2 p_n}{dx^2}\right) - \frac{p_n - p_{no}}{\tau_p} = 0, \qquad (11)$$

分解為:

$$p_n(x) = p_n + C_1 e^{x/L_p} + C_2 e^{-x/L_p}, \quad (12)$$

B.C.

$$p_n(0) = p_{no}\, e^{qV_{EB}/kT} \quad \text{EB forward} \quad (13a)$$

$$p_n(W) = 0, \quad \text{BC reverse} \quad (13b)$$

Ref. Fig. 4.6 (後面)

Substituting Eq. 13 into the general solution expressed in Eq. 12 yields

$$p_n(x) = p_{no}(e^{qV_{EB}/kT} - 1)\left[\frac{\sinh\left(\frac{W-x}{L_p}\right)}{\sinh\left(\frac{W}{L_p}\right)}\right] + p_{no}\left[1 - \frac{\sinh\left(\frac{x}{L_p}\right)}{\sinh\left(\frac{W}{L_p}\right)}\right] \qquad (14)$$

If W/Lp<<1

$$p_n(x) = p_{no}\, e^{qV_{EB}/kT}\left(1 - \frac{x}{W}\right) = \underline{p_n(0)\left(1 - \frac{x}{W}\right)} \,. \qquad (15)$$

linear

B.C

$$n_E(x = -x_E) = n_{EO}\, e^{qV_{EB}/kT} \quad (16)$$

$$n_C(x = x_C) = n_{CO}\, e^{-q|V_{CB}|} = 0, \quad (17)$$

$$n_E(x) = n_{EO} + n_{EO}\left(e^{qV_{EB}/kT} - 1\right) e^{\frac{x+x_E}{L_E}} \qquad x \le -x_E, \quad (18)$$

$$n_C(x) = n_{CO} - n_{CO}\, e^{-\frac{x-x_C}{L_C}} \qquad x \ge x_C \;. \quad (19)$$

W/Lp<<1

$$I_{Ep} = A\left(-qD_p \frac{dp_n}{dx}\bigg|_{x=0}\right) \cong \frac{qAD_p p_{no}}{W} e^{qV_{EB}/kT} . \quad (20)$$

$$I_{Cp} = A\left(-qD_p \frac{dp_n}{dx}\bigg|_{x=W}\right)$$

$$\cong \frac{qAD_p p_{no}}{W} e^{qV_{EB}/kT} . \quad (21)$$

越小越好

$$I_{En} = A\left(-qD_E \frac{dn_E}{dx}\bigg|_{x=-x_E}\right) = \frac{qAD_E n_{EO}}{L_E}\left(e^{qV_{EB}/kT} - 1\right), \quad (22)$$

$$I_{Cn} = A\left(-qD_C \frac{dn_C}{dx}\bigg|_{x=x_C}\right) = \frac{qAD_C n_{CO}}{L_C}, \quad (23)$$

$$I_E = a_{11}\left(e^{qV_{EB}/kT} - 1\right) + a_{12}$$ $=I_{EP}+I_{En}$ (24)

$$I_C = a_{21}\left(e^{qV_{EB}/kT} - 1\right) + a_{22},$$ $=I_{cP}+I_{cn}$ (27)

又a12=a21

$$I_B = \left(a_{11} - a_{21}\right)\left(e^{qV_{EB}/kT} - 1\right) + \left(a_{12} - a_{22}\right).$$ (30)

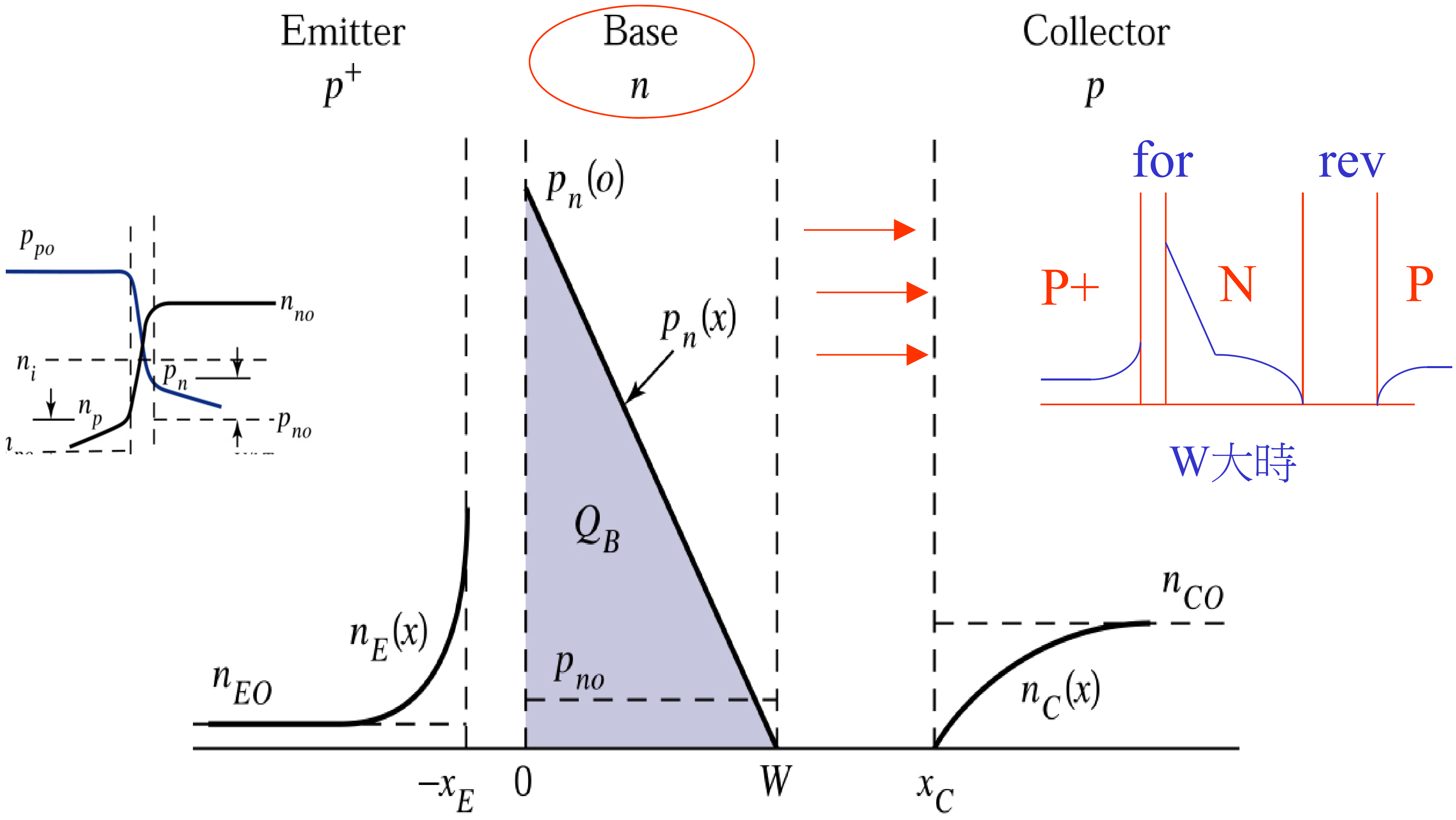


Figure 4.6. Minority carrier distribution in various regions of a *p-n-p* transistor under the active mode of operation.

Summary :

1. I_B, I_C 受V影響,正比exp(qV/kT), continuity eq.
2. I_C,I_E 可由邊界之少數載子梯度表示 .
3. IB=IE-IC

Emitter eff.

$$\gamma \equiv \frac{I_{Ep}}{I_{Ep}+I_{En}} \cong \frac{\frac{D_p p_{no}}{W}}{\frac{D_p p_{no}}{W}+\frac{D_E n_{EO}}{L_E}} = \frac{1}{1+\frac{D_E}{D_p}\frac{n_{EO}}{p_{no}}\frac{W}{L_E}} \qquad (31)$$

($I_{Ep}+I_{En}$ = IE)

☆ $$\gamma = \frac{1}{1+\frac{D_E}{D_p}\cdot\frac{N_B}{N_E}\cdot\frac{W}{L_E}}, \qquad (31a)$$

➢ 欲使γ →1

1. NB/NE ↓
2. W ↓

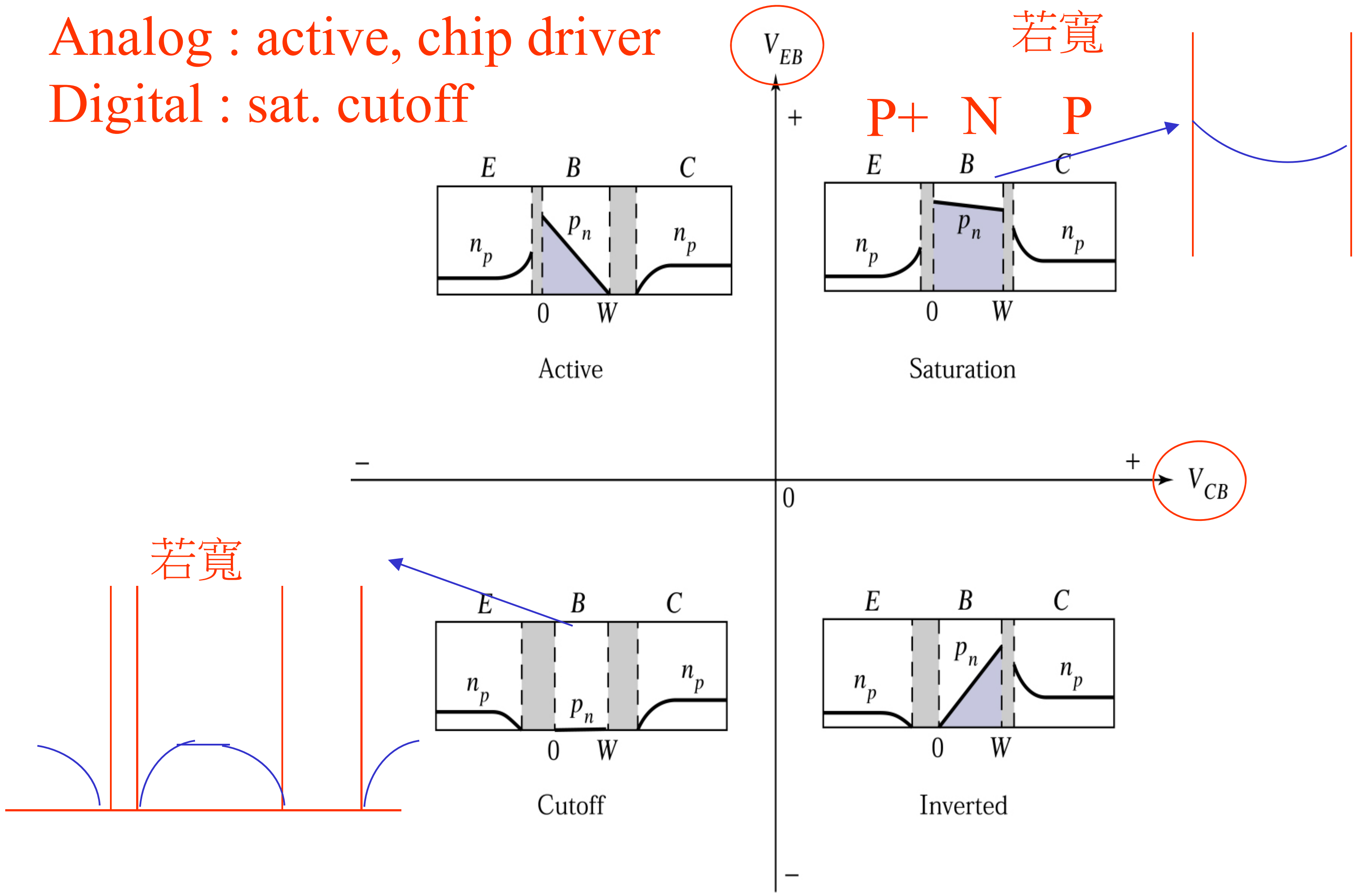


Figure 4.7. Junction polarities and minority carrier distributions of a *p-n-p* transistor under four modes of operation.

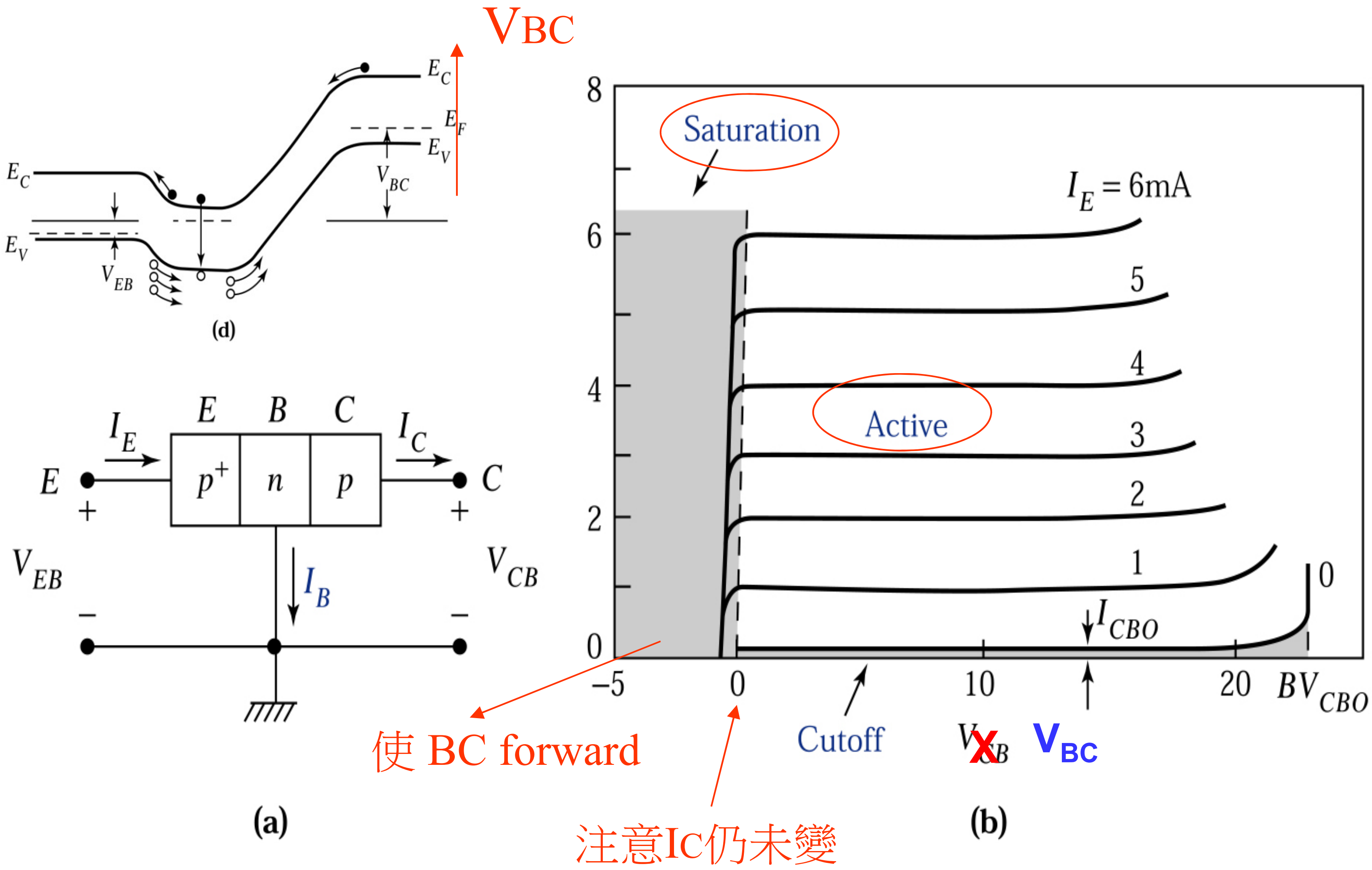


Figure 4.8. (*a*) Common-base configuration of a *p-n-p* transistor. (*b*) Its output current-voltage characteristics.

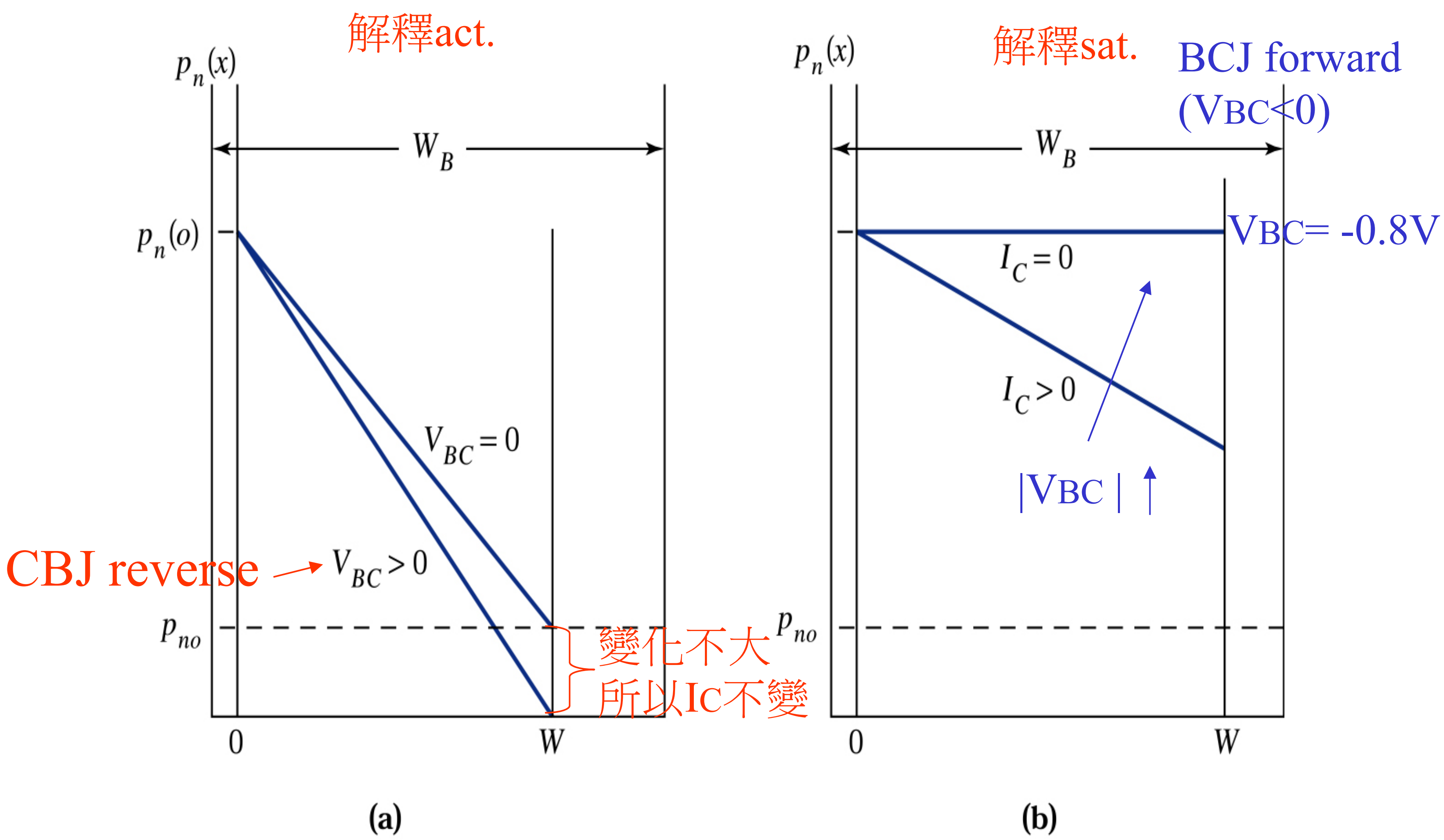


Figure 4.9. Minority carrier distributions in the base region of a *p-n-p* transistor. (*a*) Active mode for $V_{BC} = 0$ and $V_{BC} > 0$. (*b*) Saturation mode with both junctions forward biased.

Base Width Modulation

★ CE才是最常用的(A_I很大)　　　　* $\alpha_0 = \gamma * \alpha_T$

$$\begin{cases} I_C = \alpha_0 (\underbrace{I_B + I_C}_{I_E}) + I_{CBO} \\ I_C = \dfrac{\alpha_0}{1-\alpha_0} I_B + \dfrac{I_{CBO}}{1-\alpha_0} \end{cases}$$

★ common-emitter current gain

$$\beta_0 \equiv \frac{\Delta I_C}{\Delta I_B} = \frac{\alpha_0}{1-\alpha_0} \tag{35}$$

$$I_{CEO} \equiv \frac{I_{CBO}}{(1-\alpha_0)} \tag{36}$$

→ 無I_B之I_C大小

$I_{CEO} \sim \beta_0 * I_{CBO}$

$$I_C = \beta_0 I_B + I_{CEO} \tag{37}$$

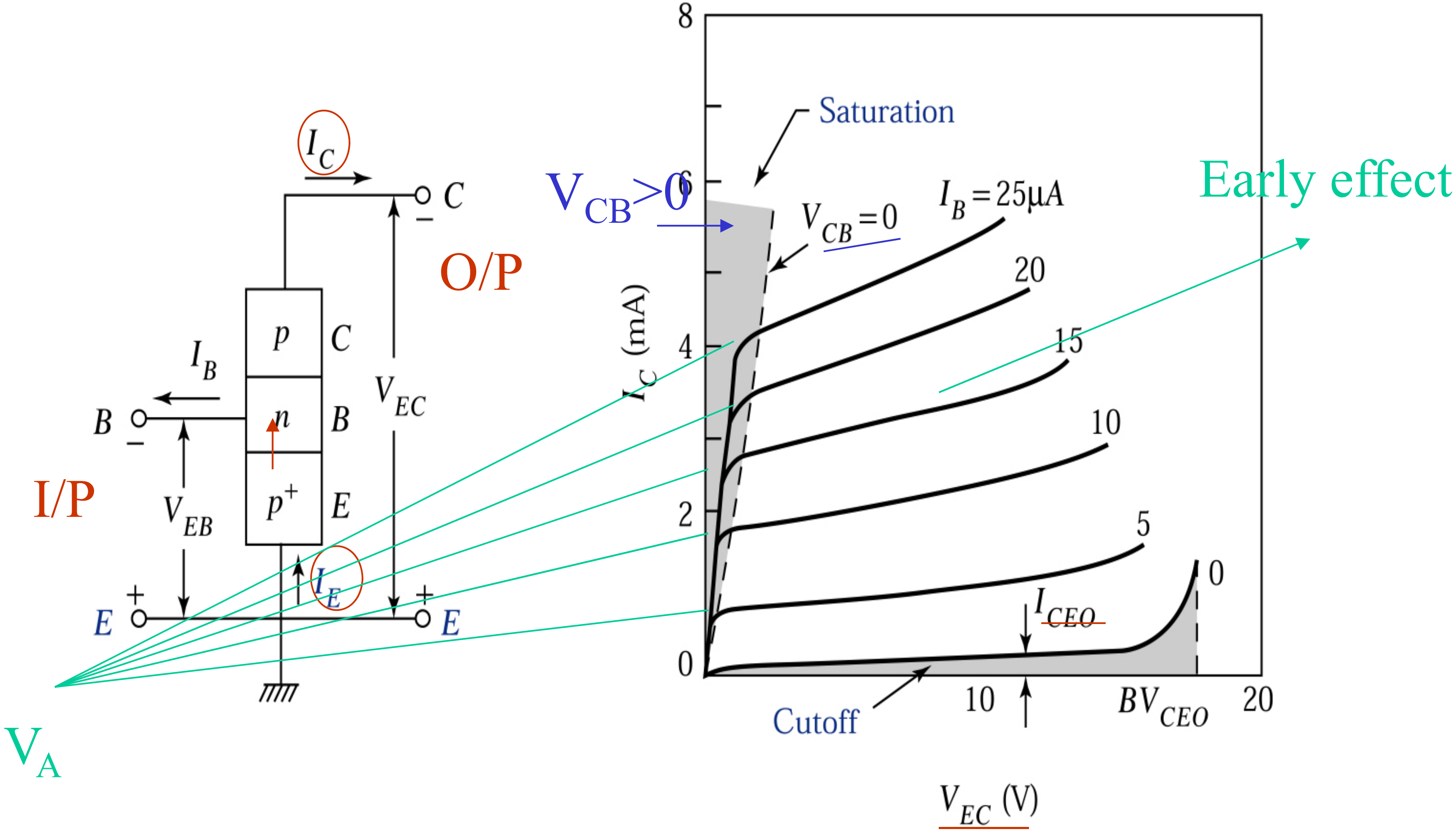


Figure 4.10. (*a*) Common-emitter configuration of a *p-n-p* transistor. (*b*) Its output current-voltage characteristics.

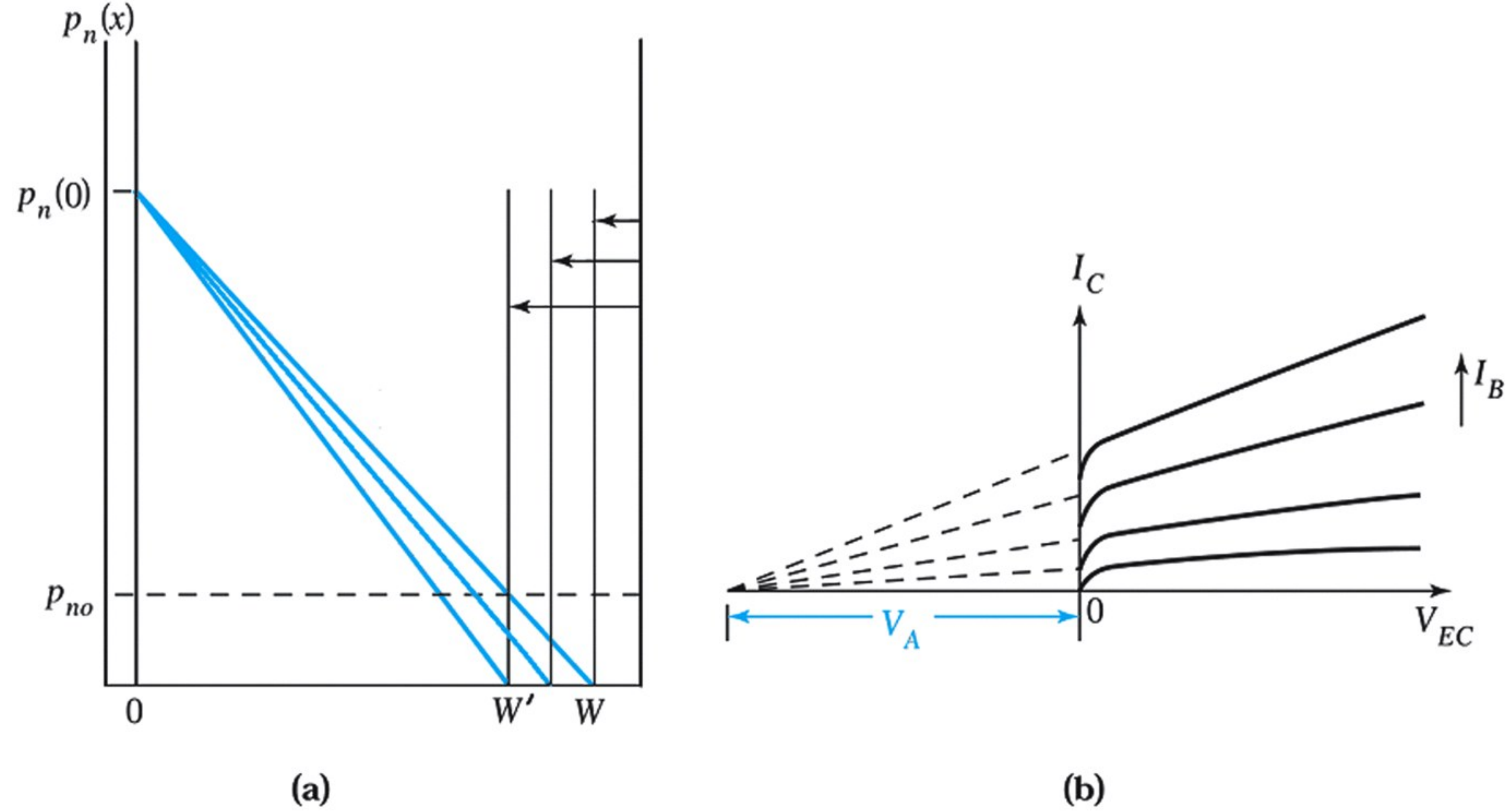


Figure 4.11

Figure 4.11. Schematic diagram of the Early effect and Early voltage V_A. The collector currents for different base currents meet at $-V_A$.

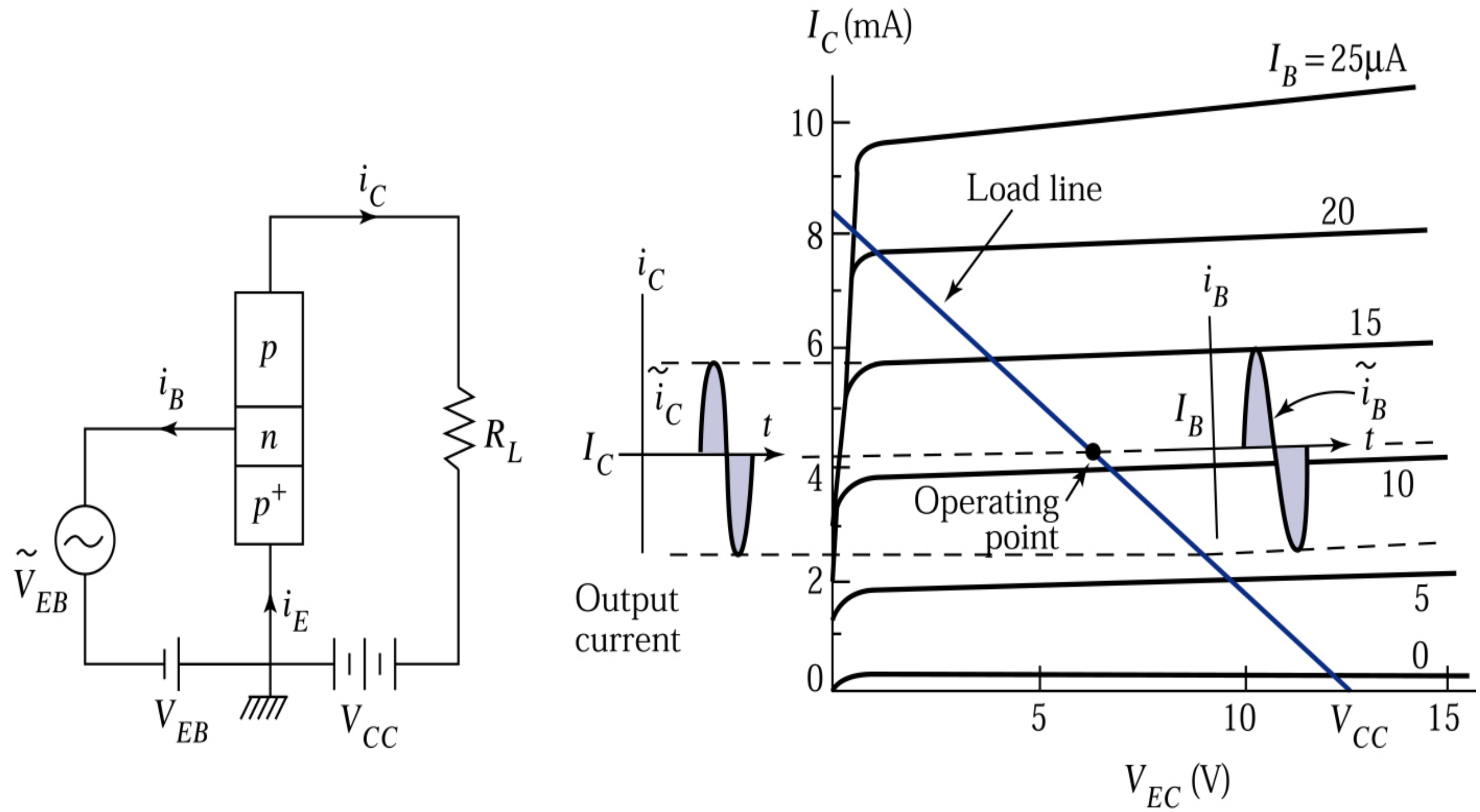
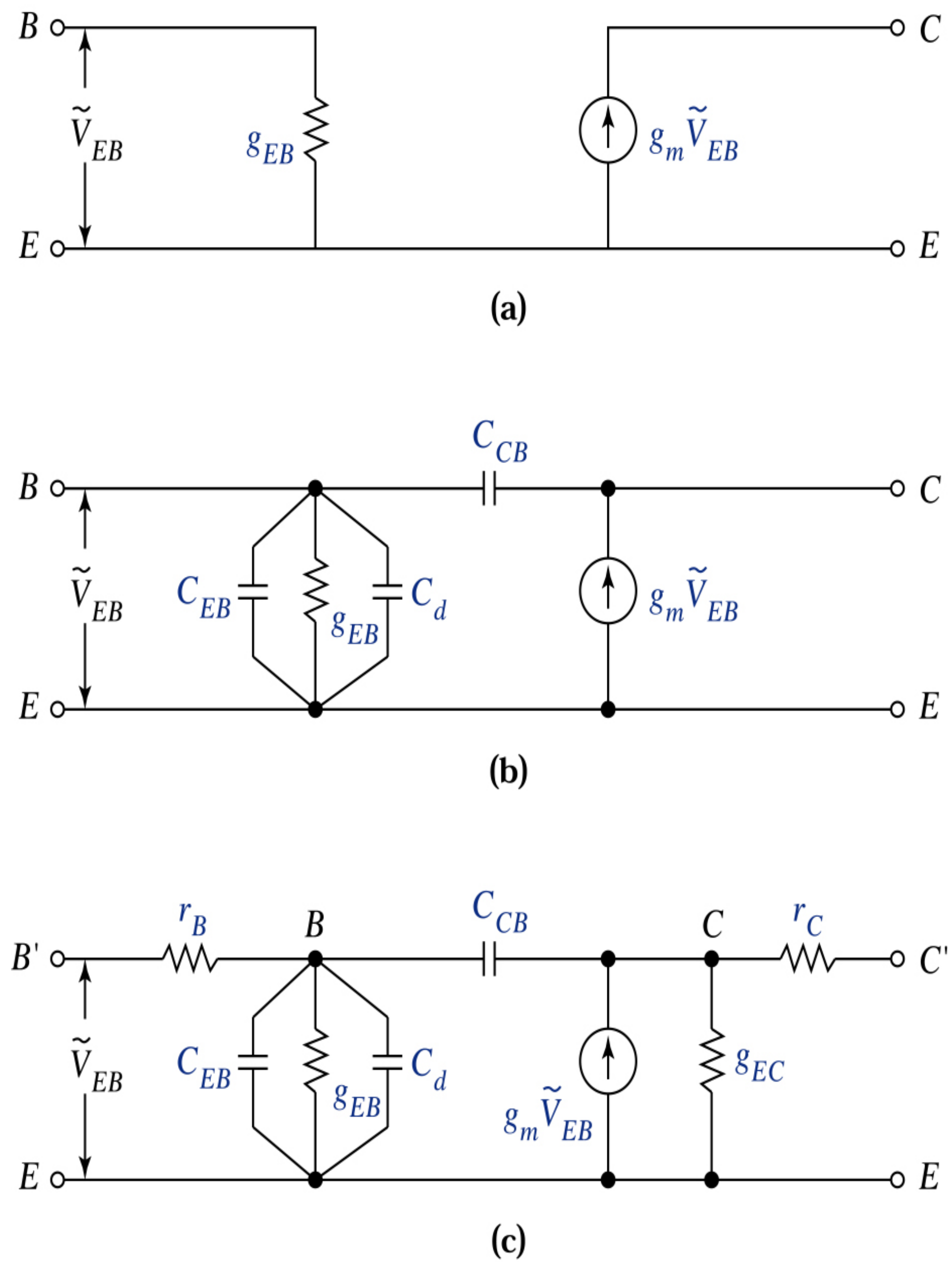
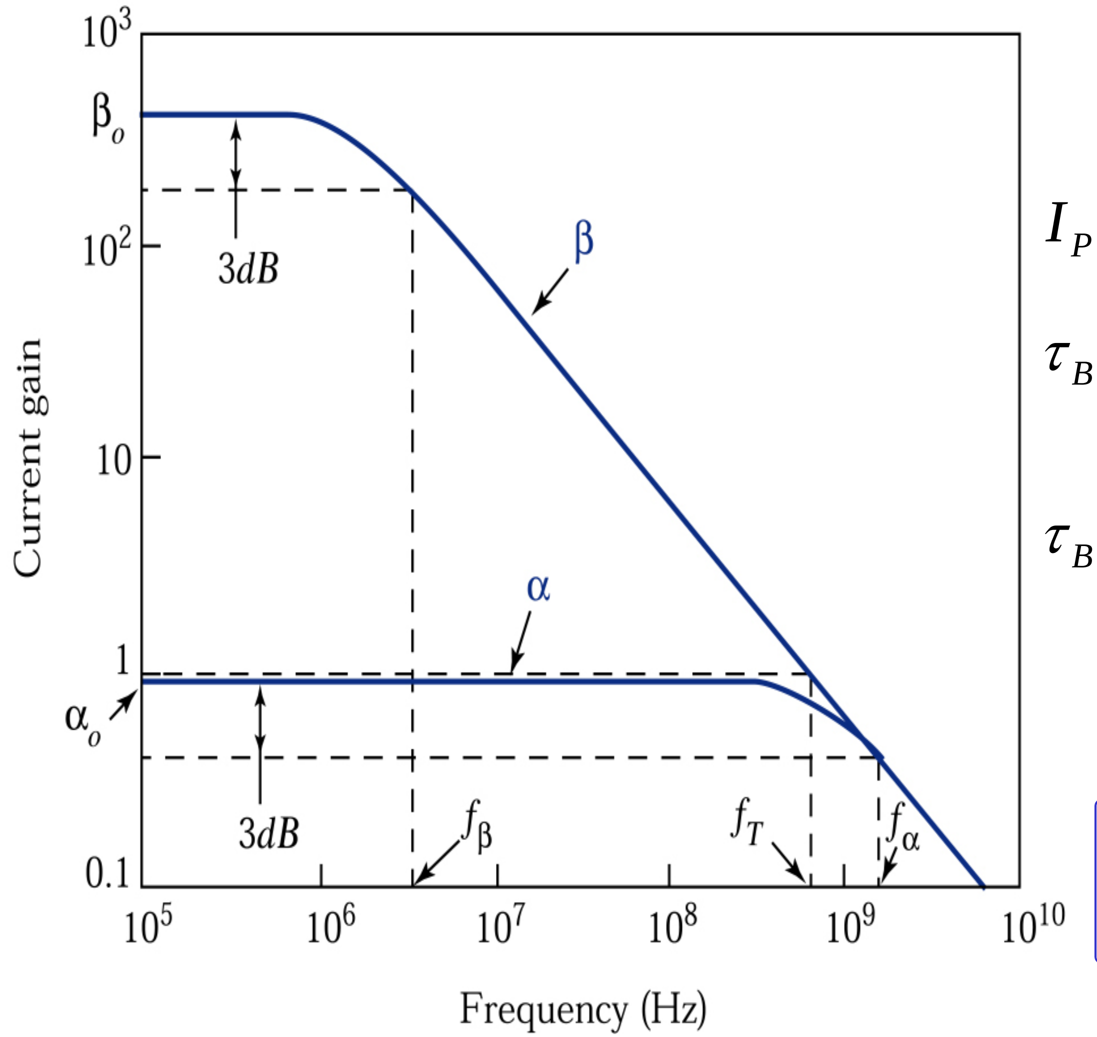


Figure 4-12. (*a*) Bipolar transistor connected in the common-emitter configuration. (*b*) Small-signal operation of the transistor circuit.

Figure 4.13.
(*a*) Basic transistor equivalent circuit. (*b*) Basic circuit with the addition of depletion and diffusion capacitances.
(*c*) Basic circuit with the addition of resistance and conductance.





速度　分佈

$$I_P = qv(x)p(x)A \qquad (42)$$

$$\tau_B = \int_0^W \frac{dx}{v(x)} = \int_0^W \frac{qp(x)A}{I_P}dx \qquad (43)$$

$$\tau_B = \frac{W^2}{2D_P} \qquad (44)$$

(基極傳導時間影響freq. response)

W ↓

D ↑ (用electron 之Dn~3Dp 即多為npn BJT)

Figure 4.14. Current gain as a function of operating frequency.

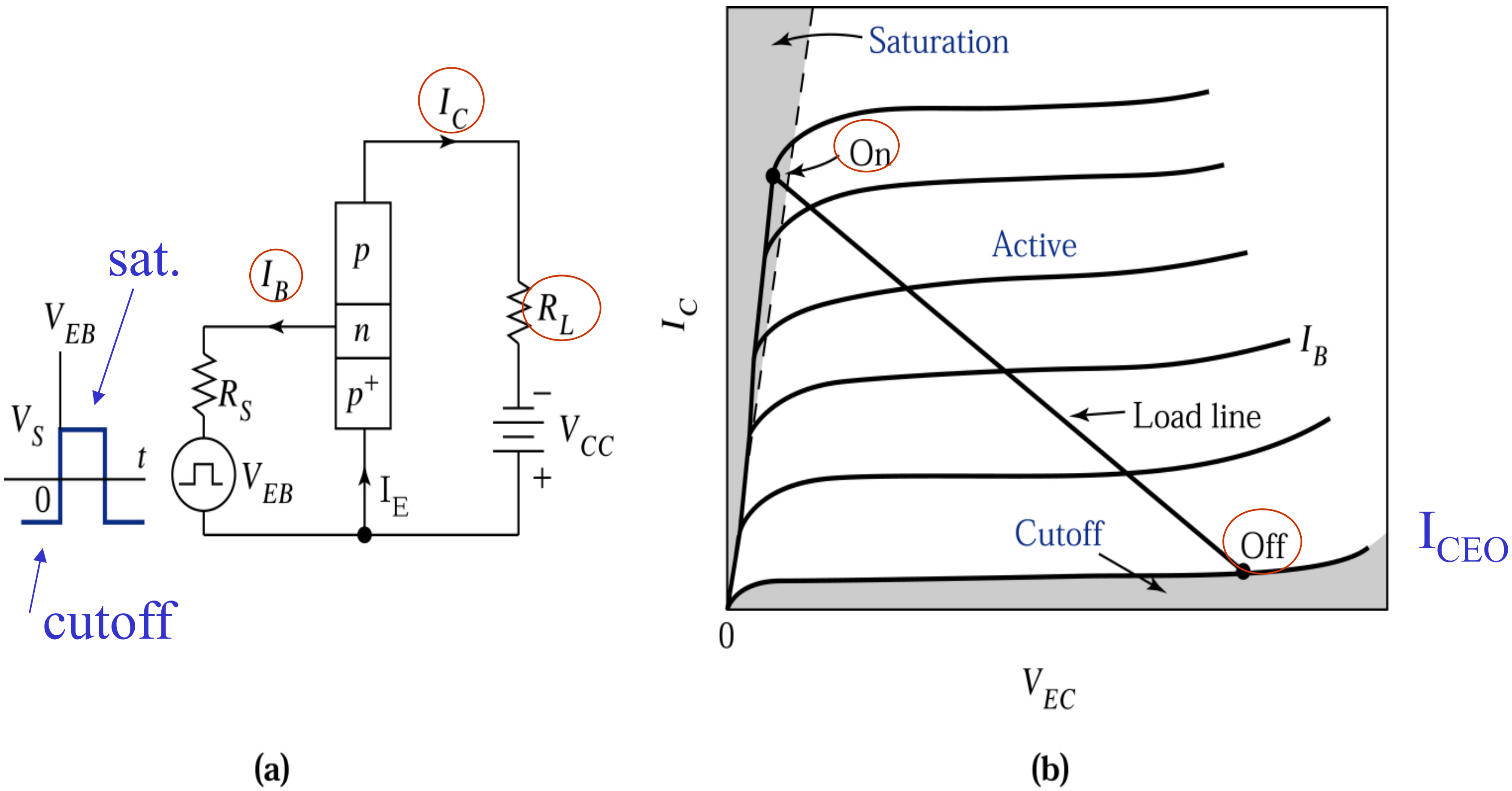
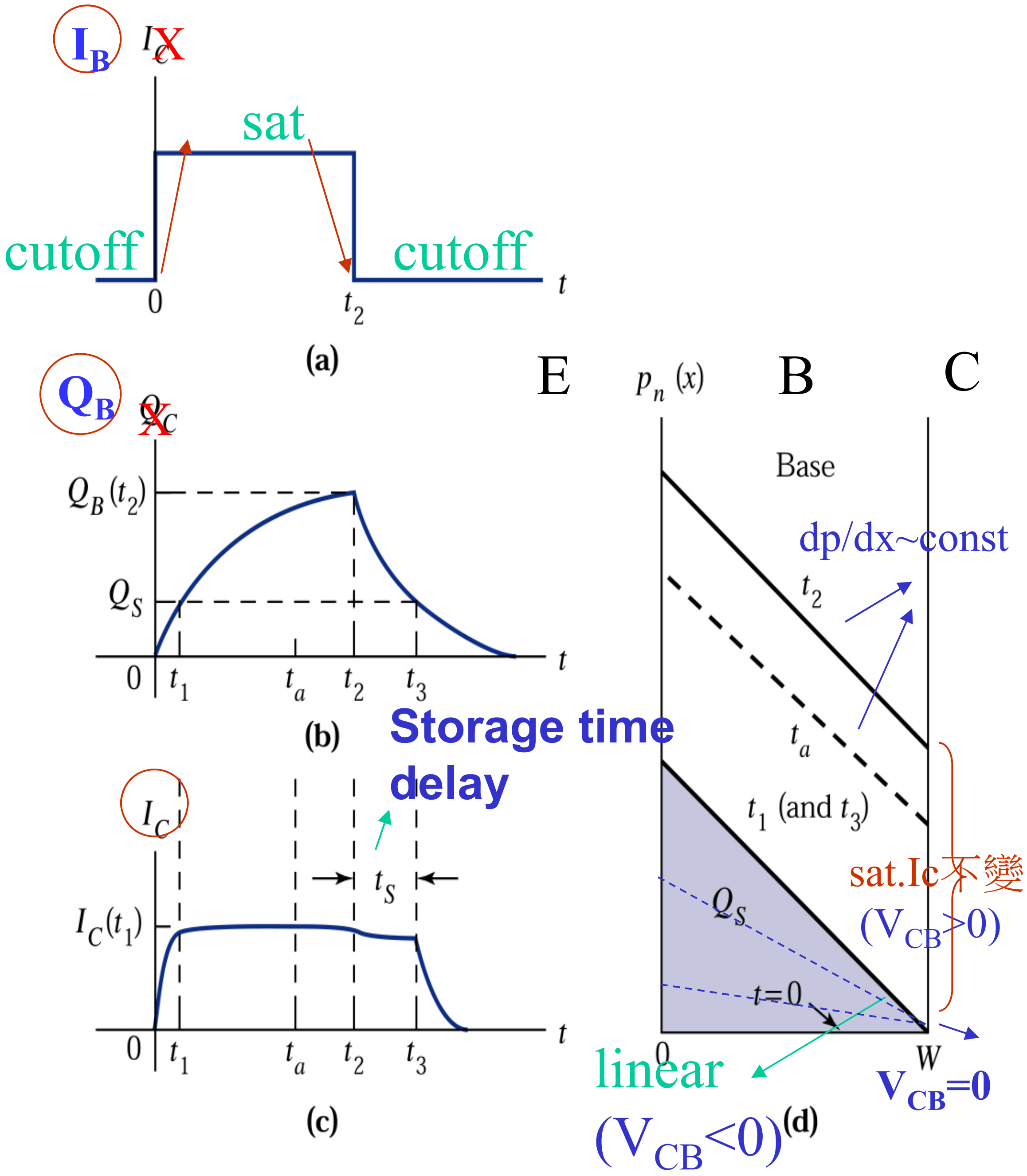


Figure 4.15. (*a*) Schematic of a transistor switching circuit. (*b*) Switching operation from cutoff to saturation.

Figure 4.16. Transistor switching characteristics (*a*) Input base current pulse. (*b*) Variations of the base-stored charge with time. (*c*) Variation of the collector current with time. (*d*) Minority-carrier distributions in the base at different times.



Nonideal Effects

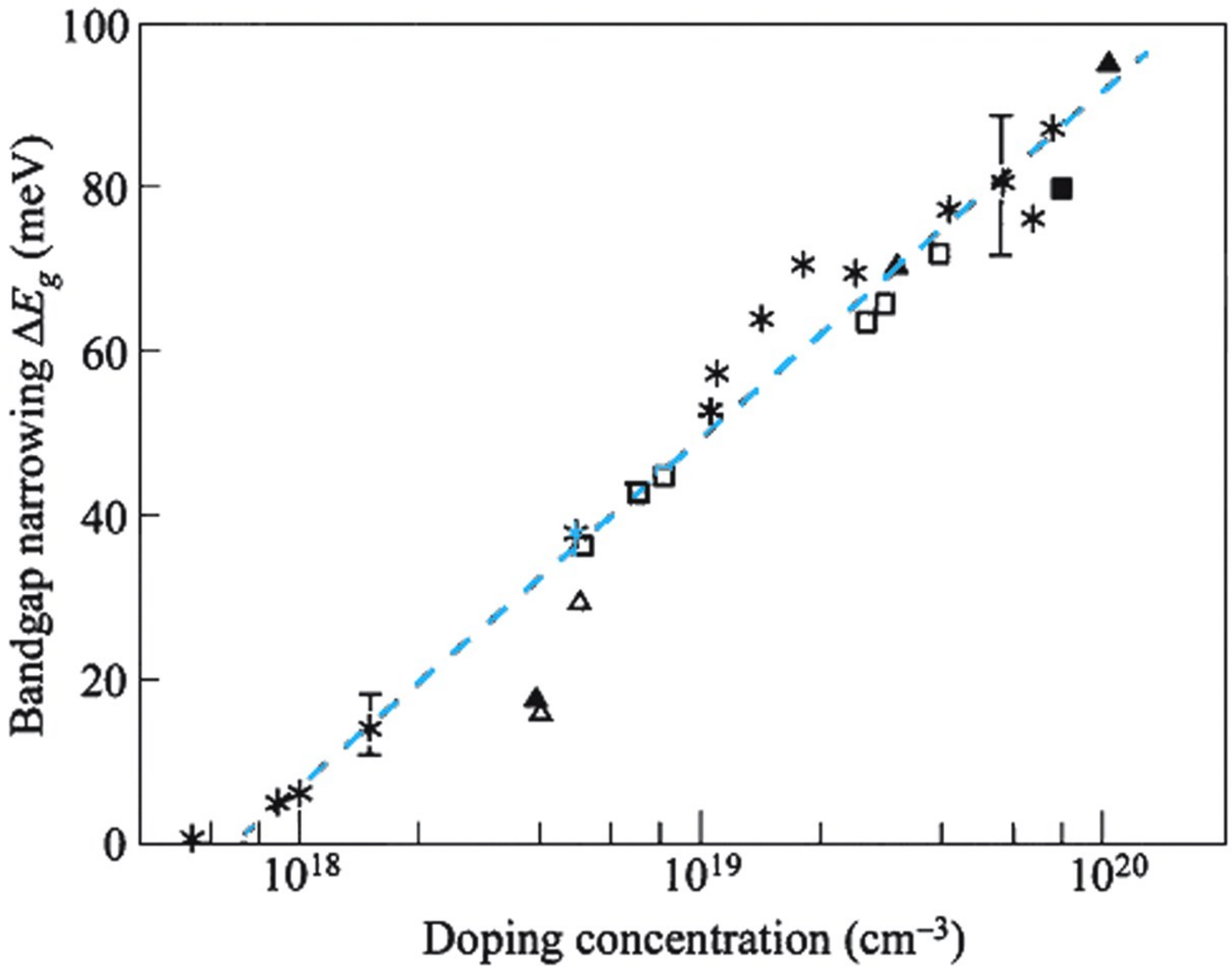


Figure 4.17

When N_E is very high, Eg is lowered, β is reduced

Nonideal Effects

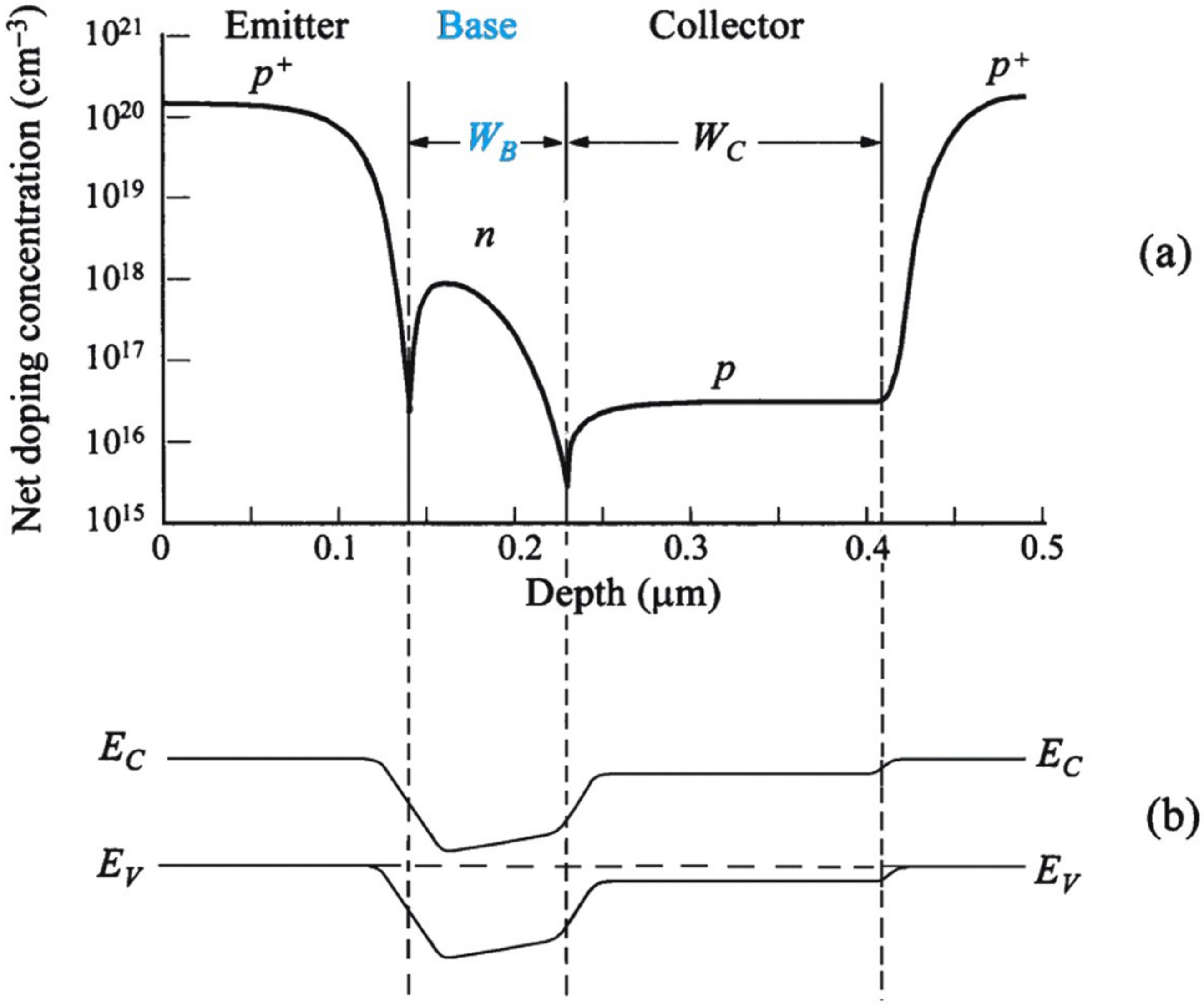


Figure 4.18

Nonideal Effects

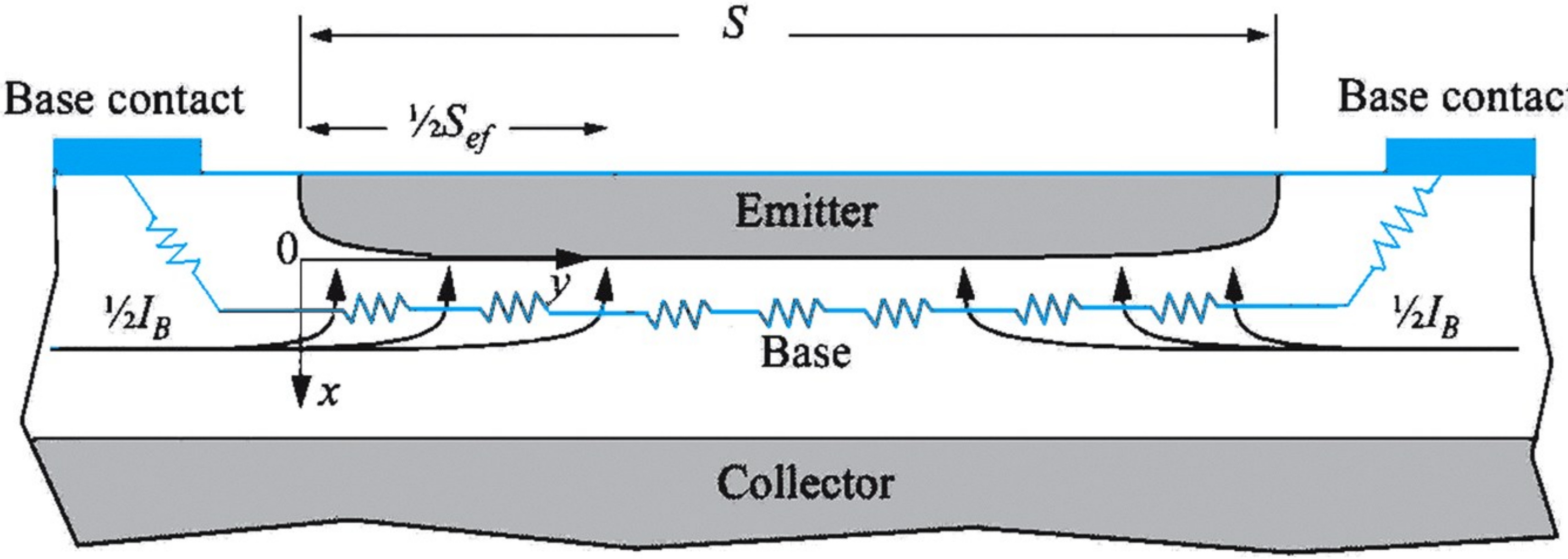
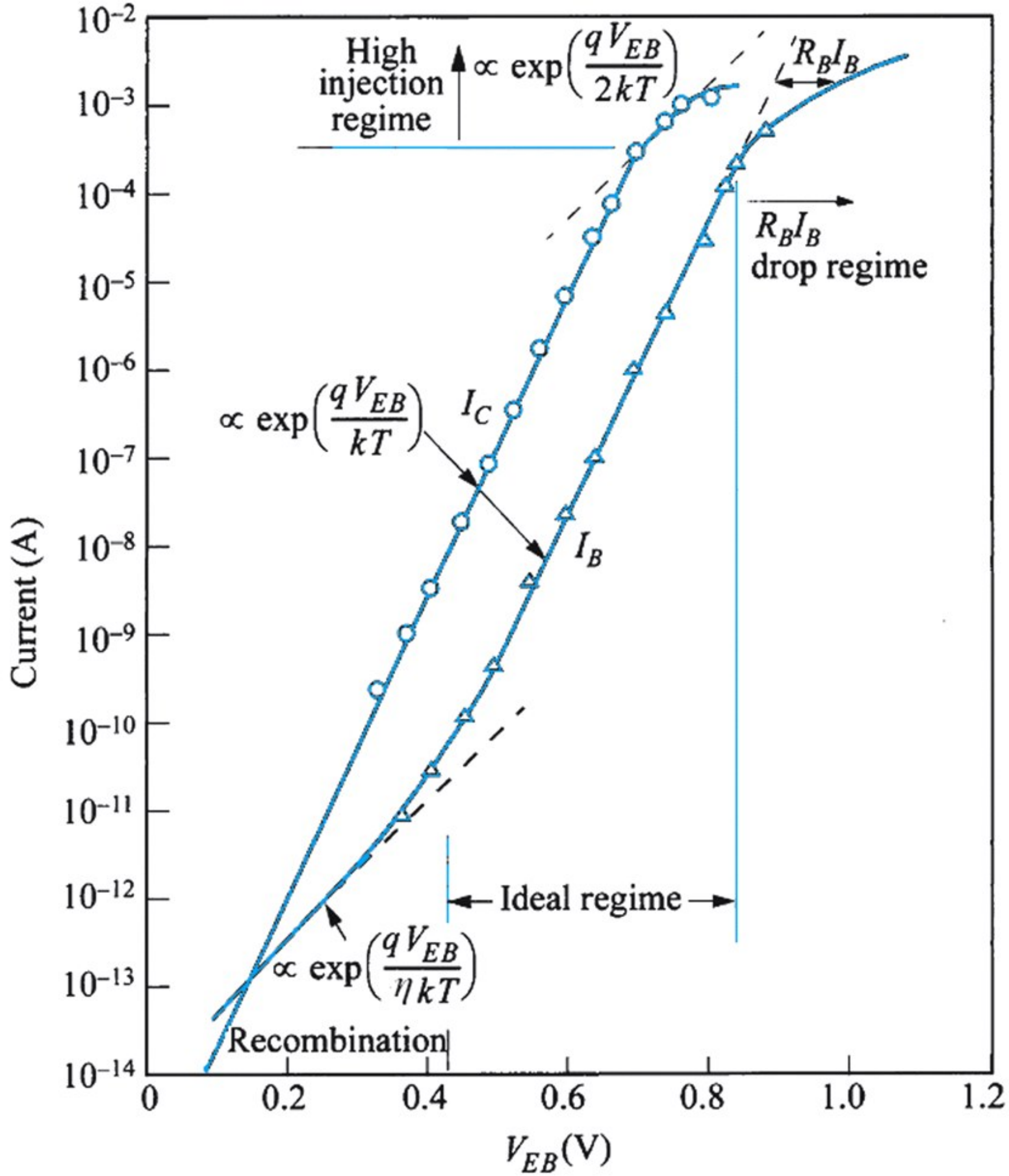


Figure 4.19

Current crowding



最重要的BJT電特性圖

Figure 4.20a

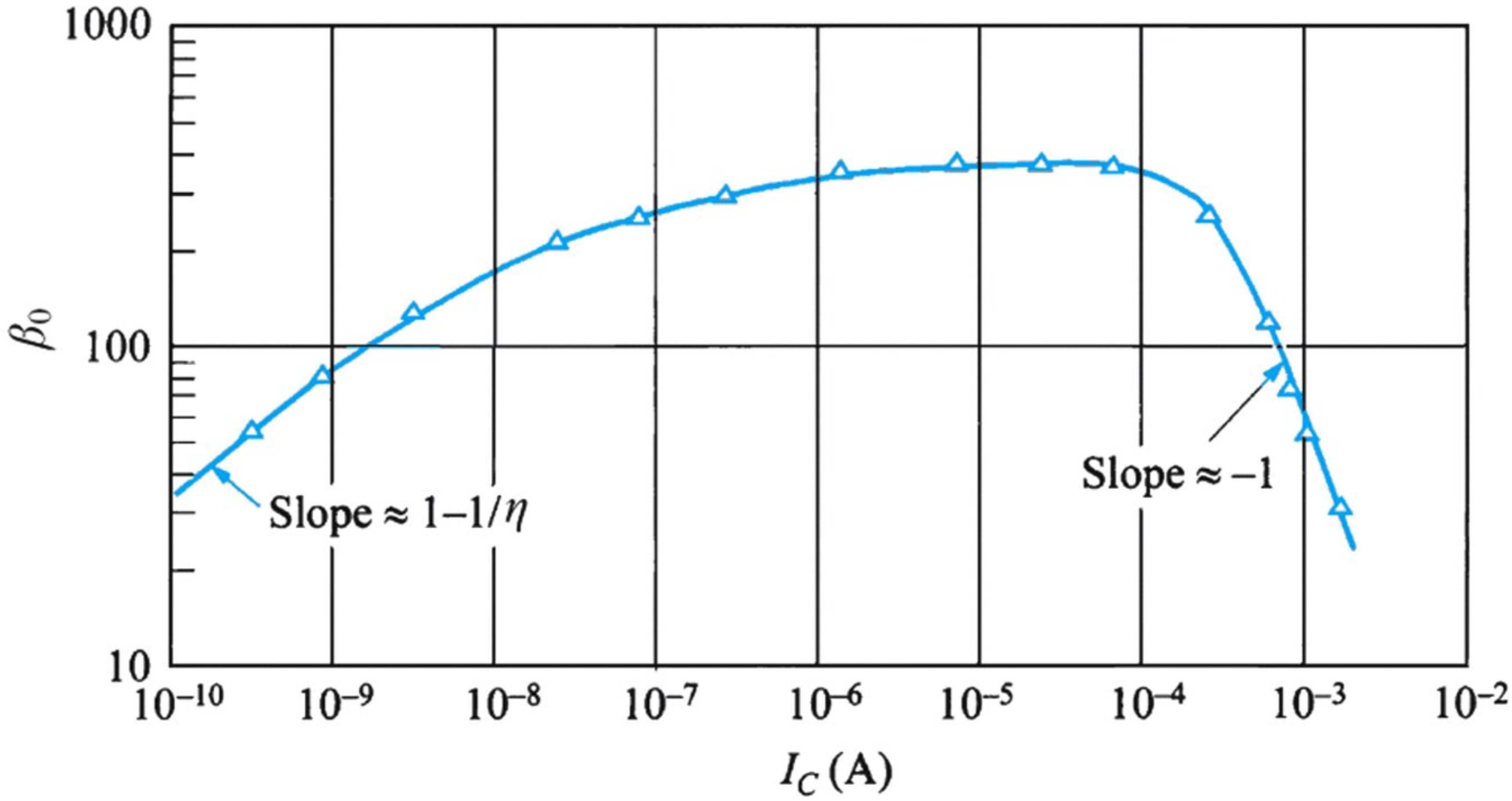

1000
100
10
β_0
10^{-10}
10^{-9}
10^{-8}
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}
I_C (A)
Slope ≈ 1–1/η
Slope ≈ –1

Figure 4.20b

I_{En} majority,

I_{Ep} 抑制，增加 γ

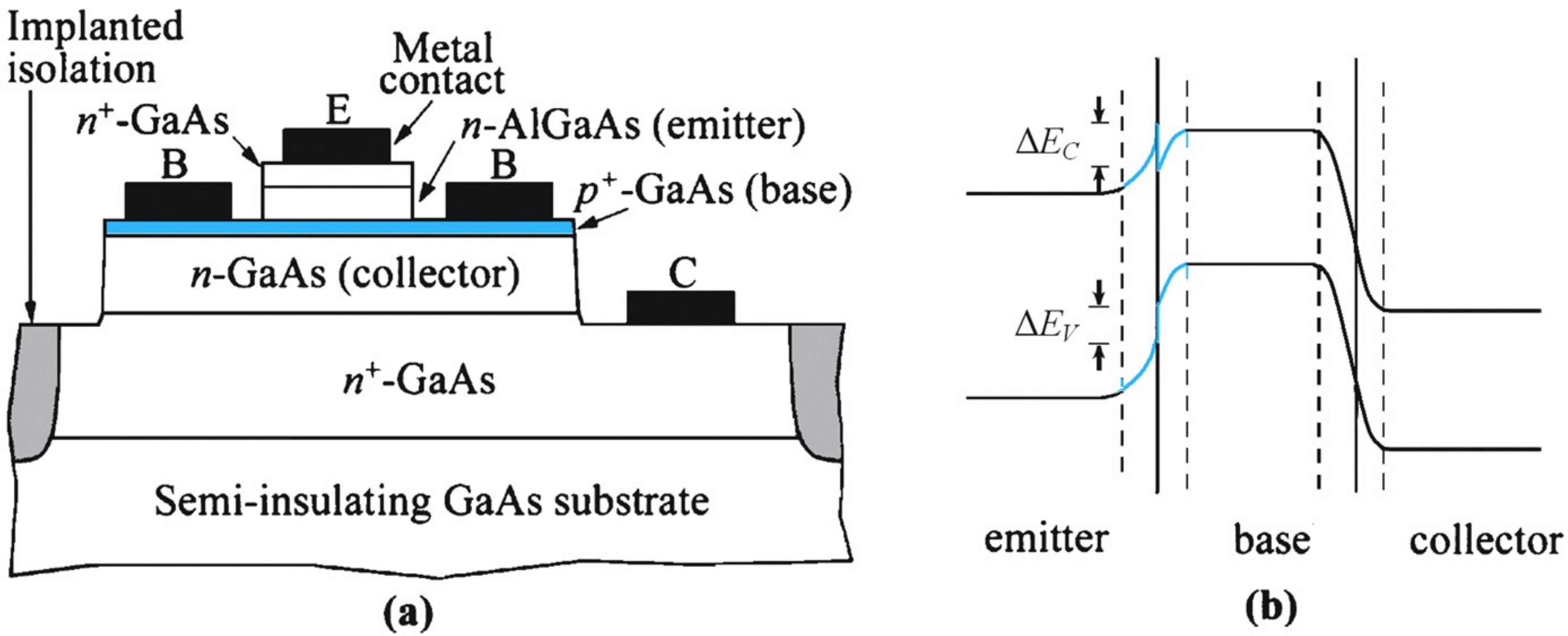


Figure 4.21

Figure 4.21. (*a*) Schematic cross section of an *n-p-n* heterojunction bipolar transistor **(HBT)** structure. (*b*) Energy band diagram of a HBT operated under **active mode**.

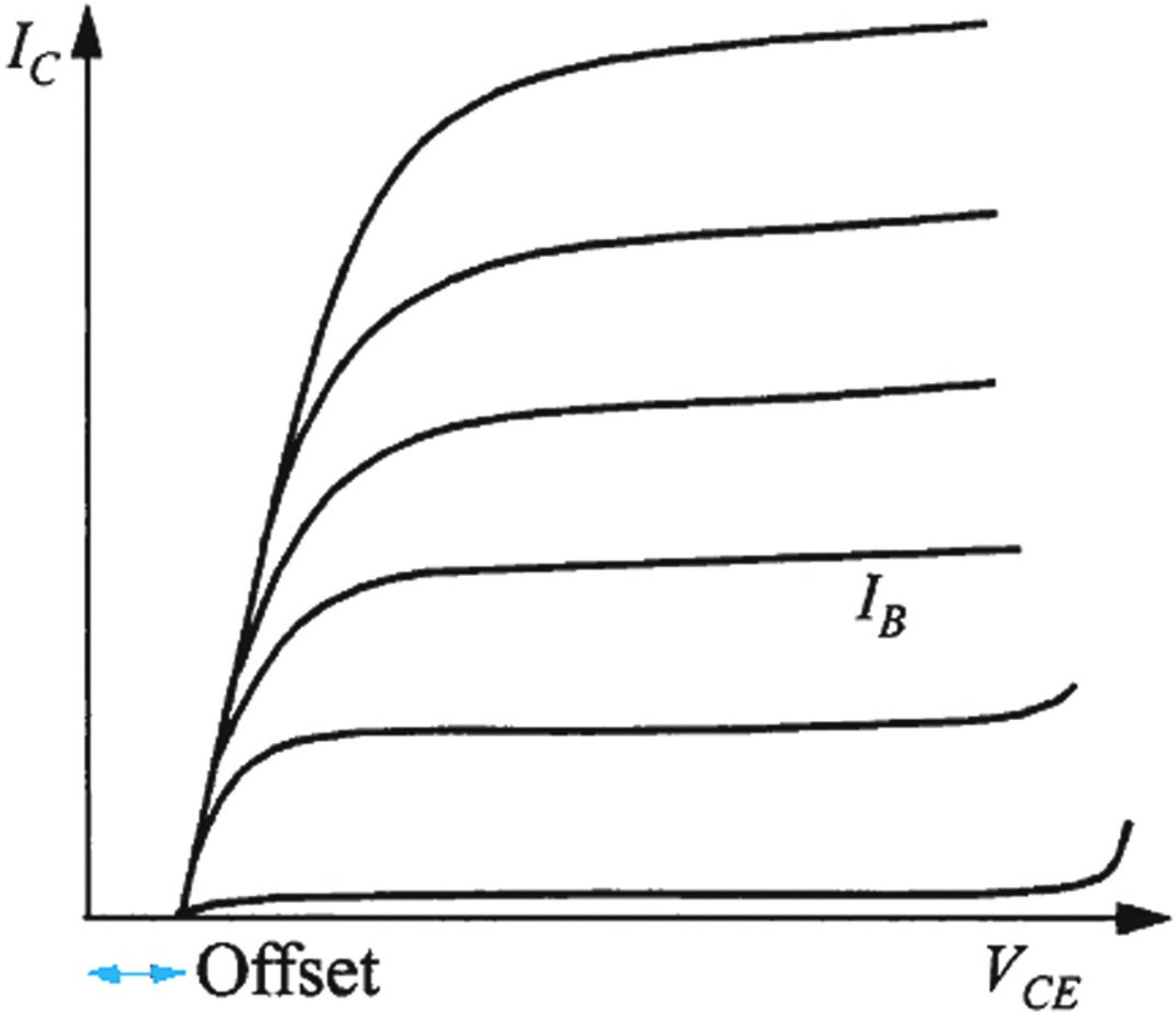
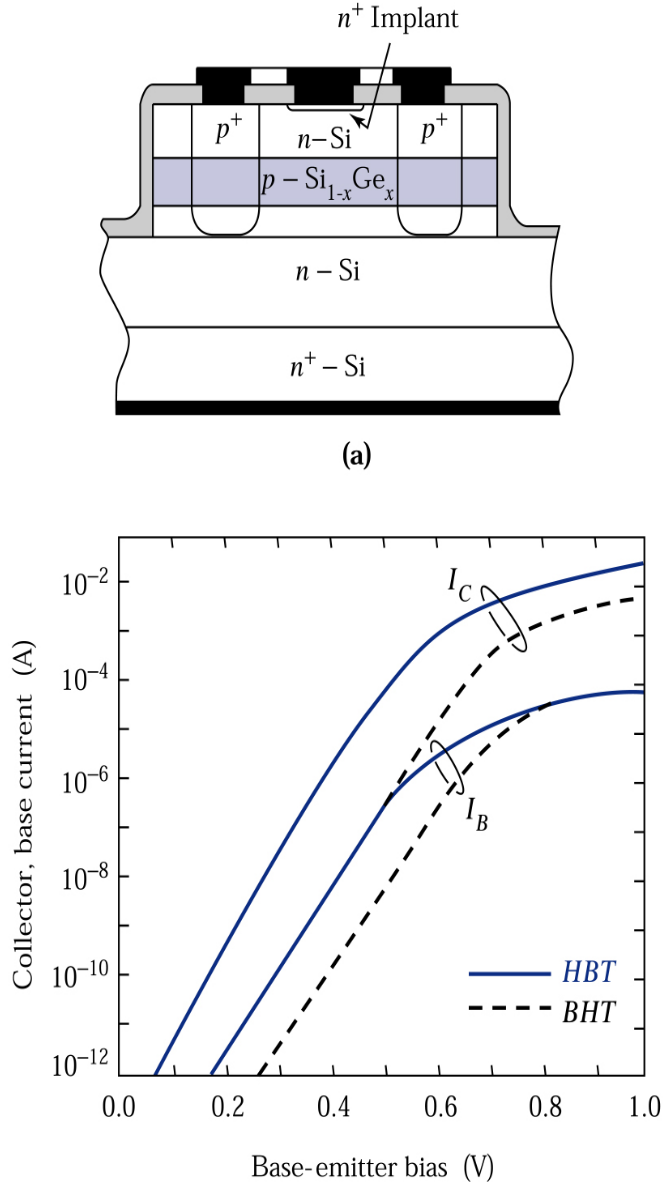


Figure 4.22

A drawback of HBT, comes from Ec barrier at EB junction

Figure
(a) Device structure of an n-p-n **Si/SiGe/Si HBT**.
(b) Collector and base current versus V_{EB} for a HBT and bipolar junction transistor (BJT).

Compatible with Si standard technology



(a)
(b)

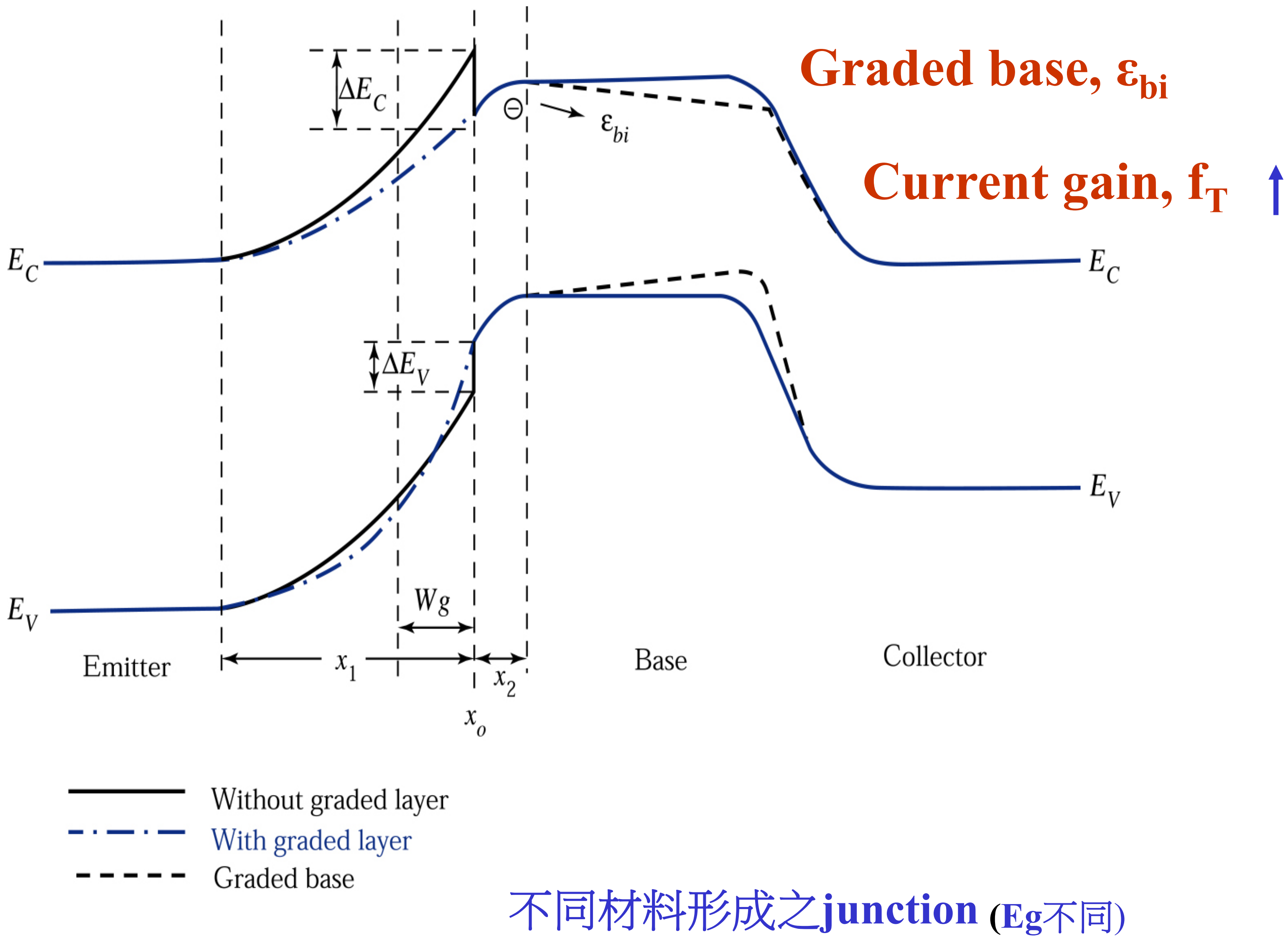
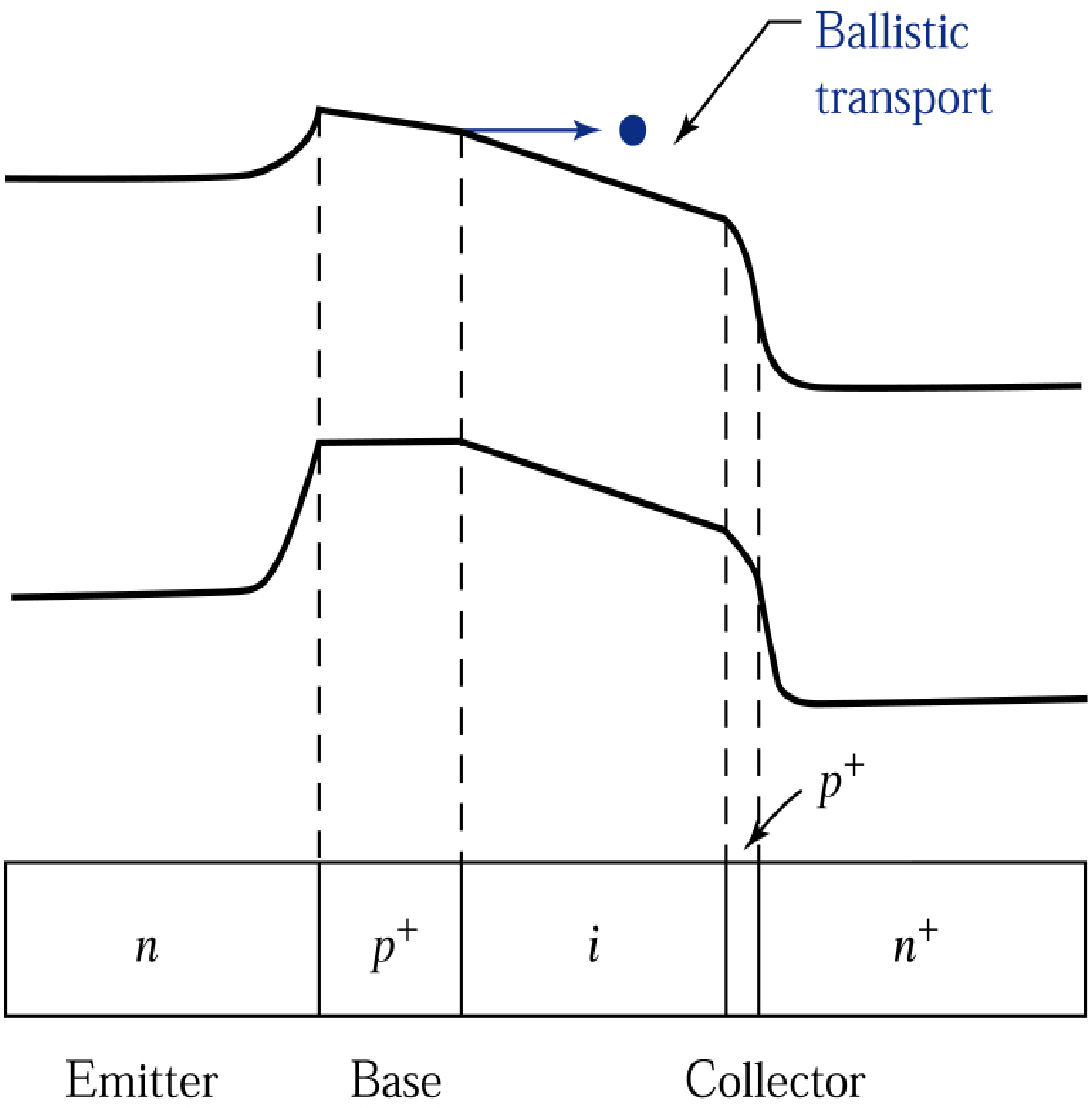
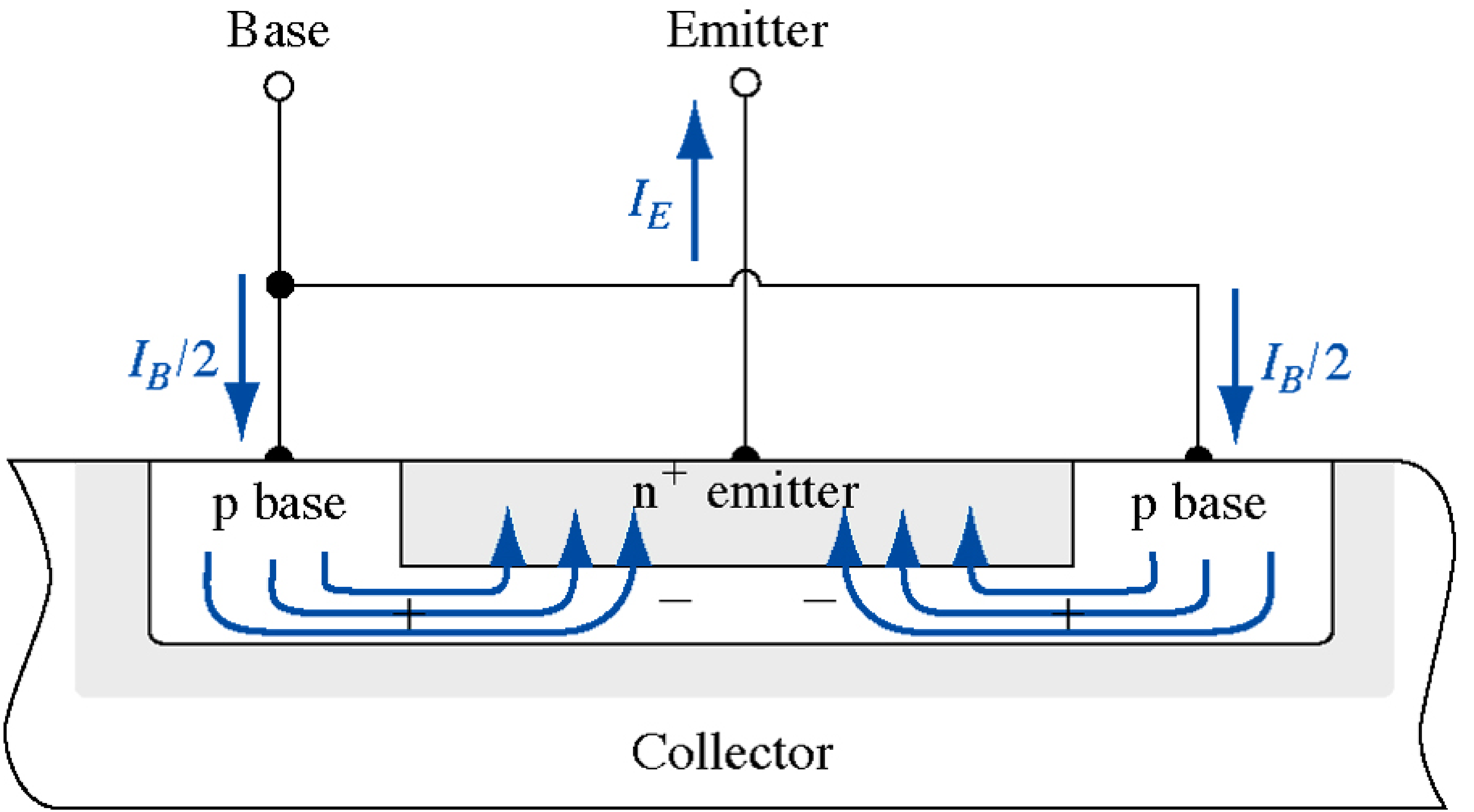
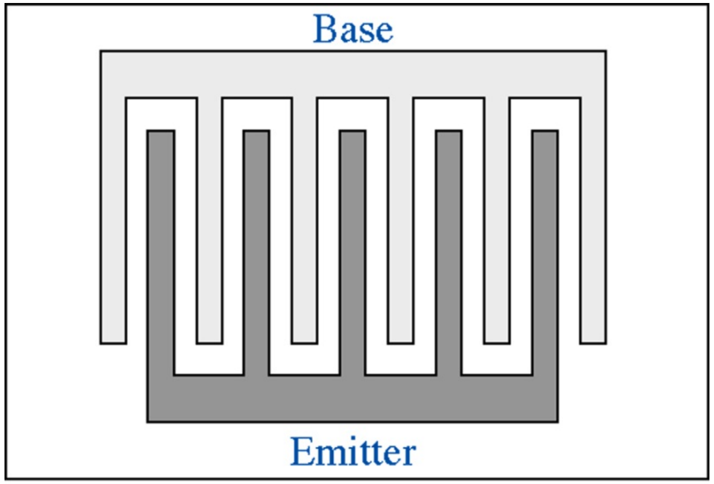


Figure 4.23. Energy band diagrams for a heterojunction bipolar transistor with and without graded layer in the junction, and with and without a graded-base layer.

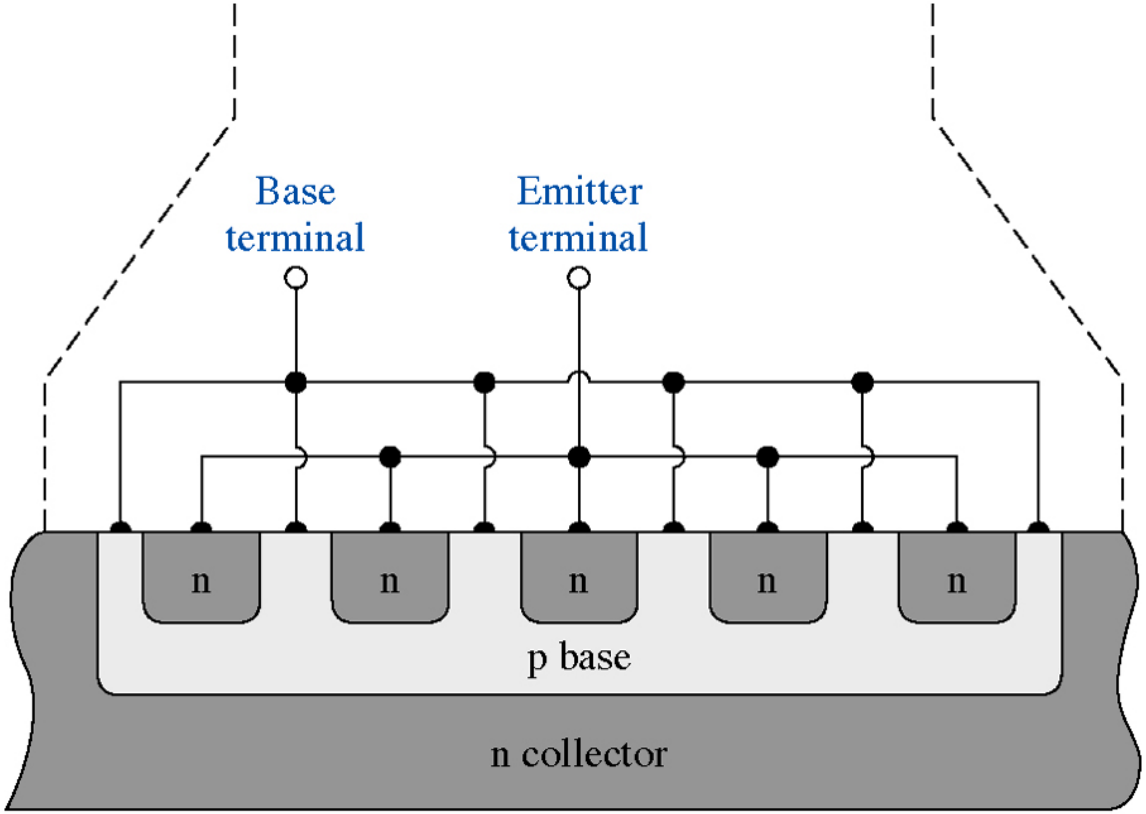
Figure 4.24.
Energy band diagram for the ballistic collector transistor (BCT).[9]




Base
Emitter
I_E
$I_B/2$
$I_B/2$
p base
n^+ emitter
p base
+
−
−
+
Collector


Base
Emitter

(a)

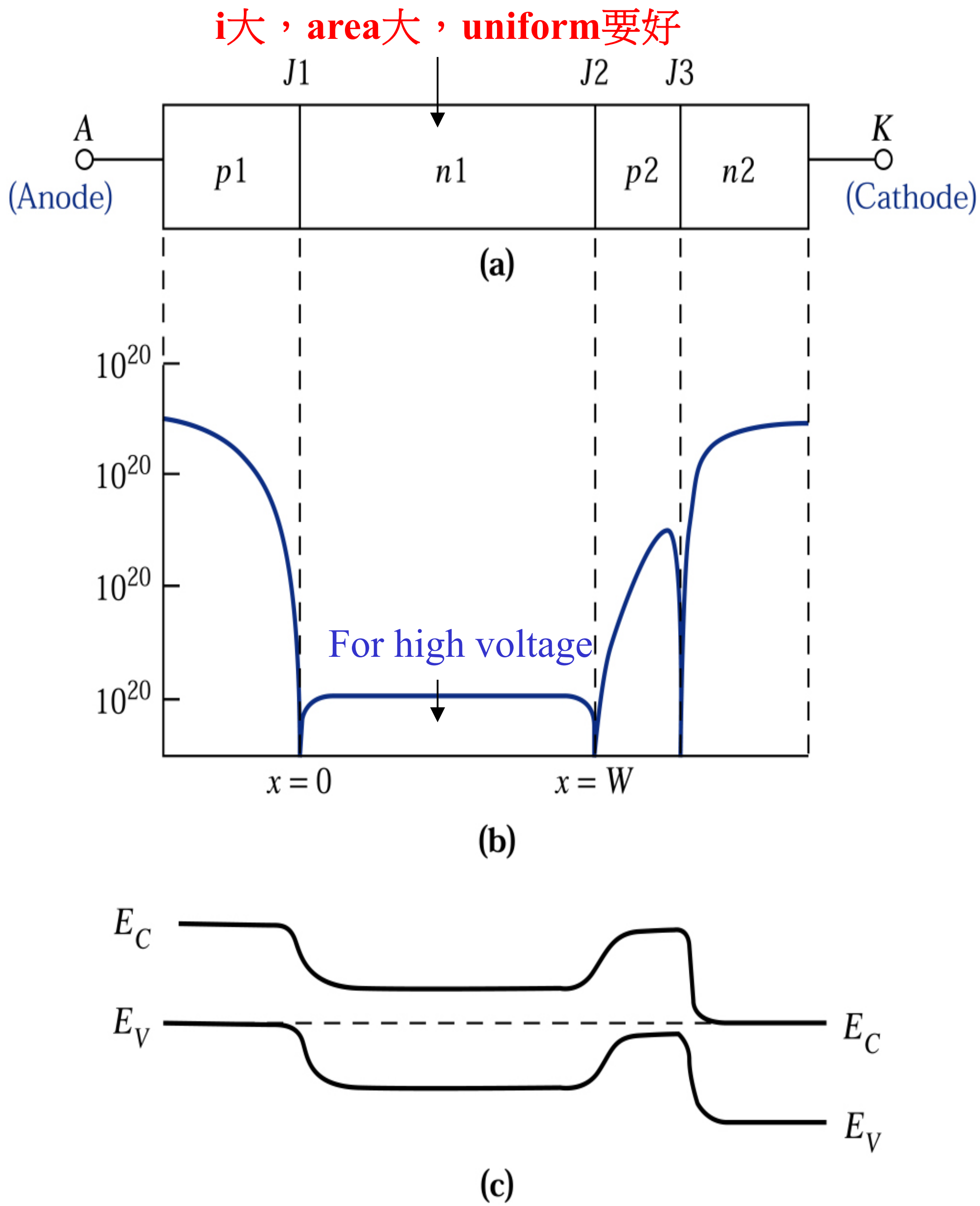

Base terminal
Emitter terminal
n
n
n
n
n
p base
n collector

(b)

Thyristor

(high power，voltage switch)

Figure 4.25.
(*a*) Four-layer *p-n-p-n* diode. (*b*) Typical doping profile of a thyristor. (*c*) Energy band diagram of a thyristor in thermal equilibrium.



n1為bulk

(NTD wafer)

P1，P2為一起dope

n2為high dope

(P2<P1)

*CMOS 之 latch-up

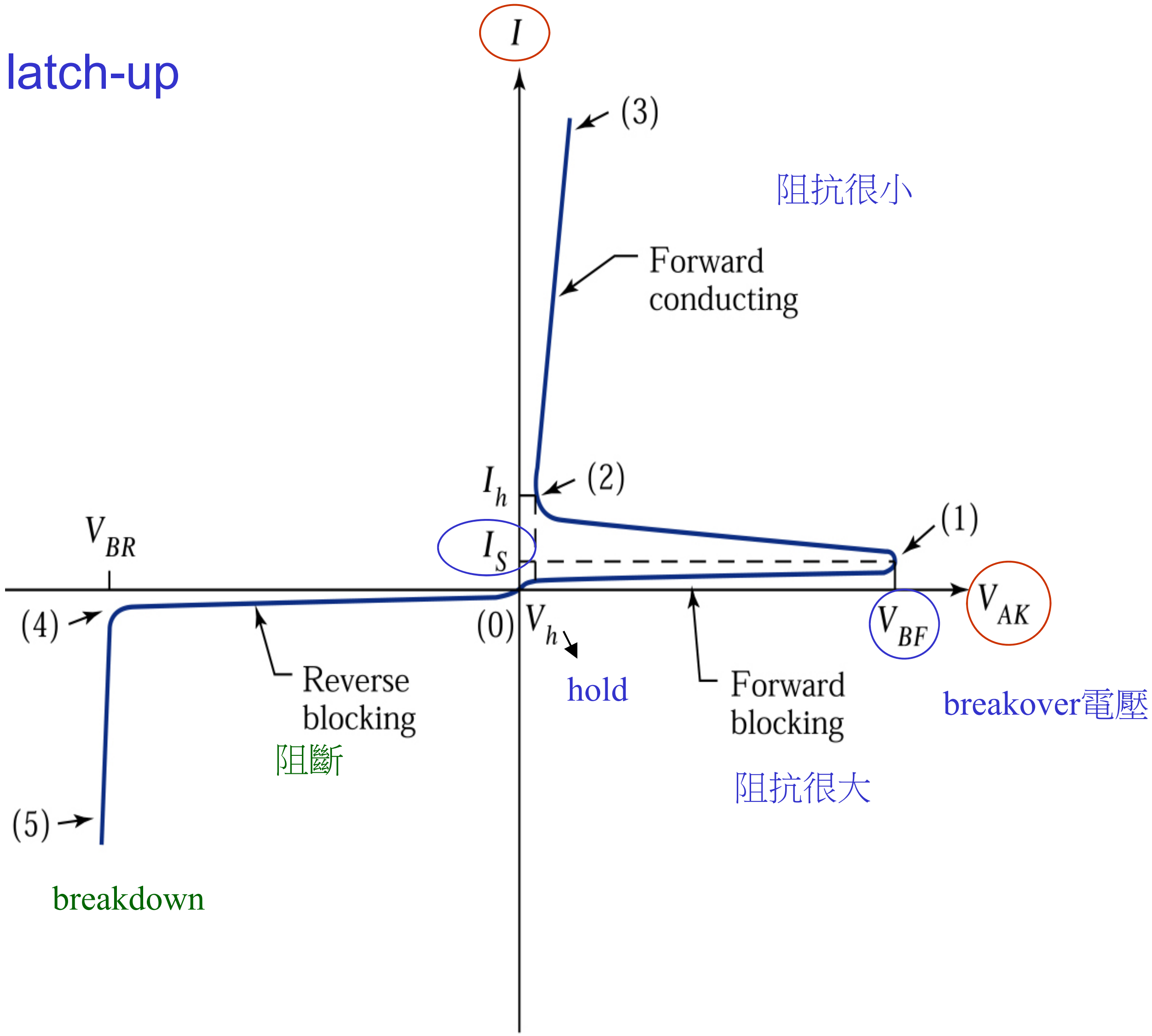


Figure 4.26. Current-voltage characteristics of a *p-n-p-n* diode.

Q1:PNP

Q2:NPN

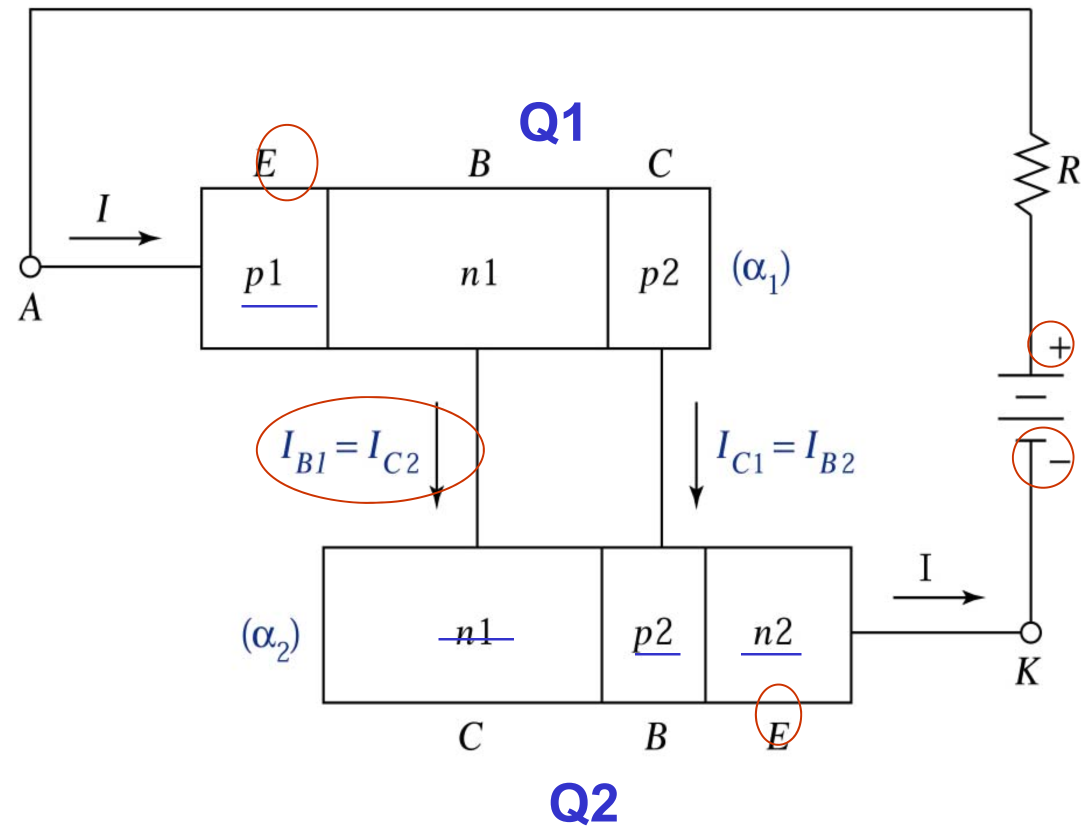


Figure 4.27. Two-transistor representation of a thyristor.[2]

Q1: $I_{B1} = I_{E1} - I_{C1} = (1-\alpha_1)I_{E1} - I_1 (\because I_{C1} = \alpha_1 I_{E1} + I_{CBO})$

$$= (1-\alpha_1)I - I_1$$

I_1 為 Q_1 之 I_{CBO}

Q2: $I_{C2} = \alpha_2 I_{E2} + I_2 = \alpha_2 I + I_2$

I_2 為 Q_2 之 I_{CBO}

令 $I_{B1} = I_{C2}$

$$(1-\alpha_1)I - I_1 = \alpha_2 I + I_2$$

$$I = \frac{I_1 + I_2}{1-(\alpha_1+\alpha_2)}$$

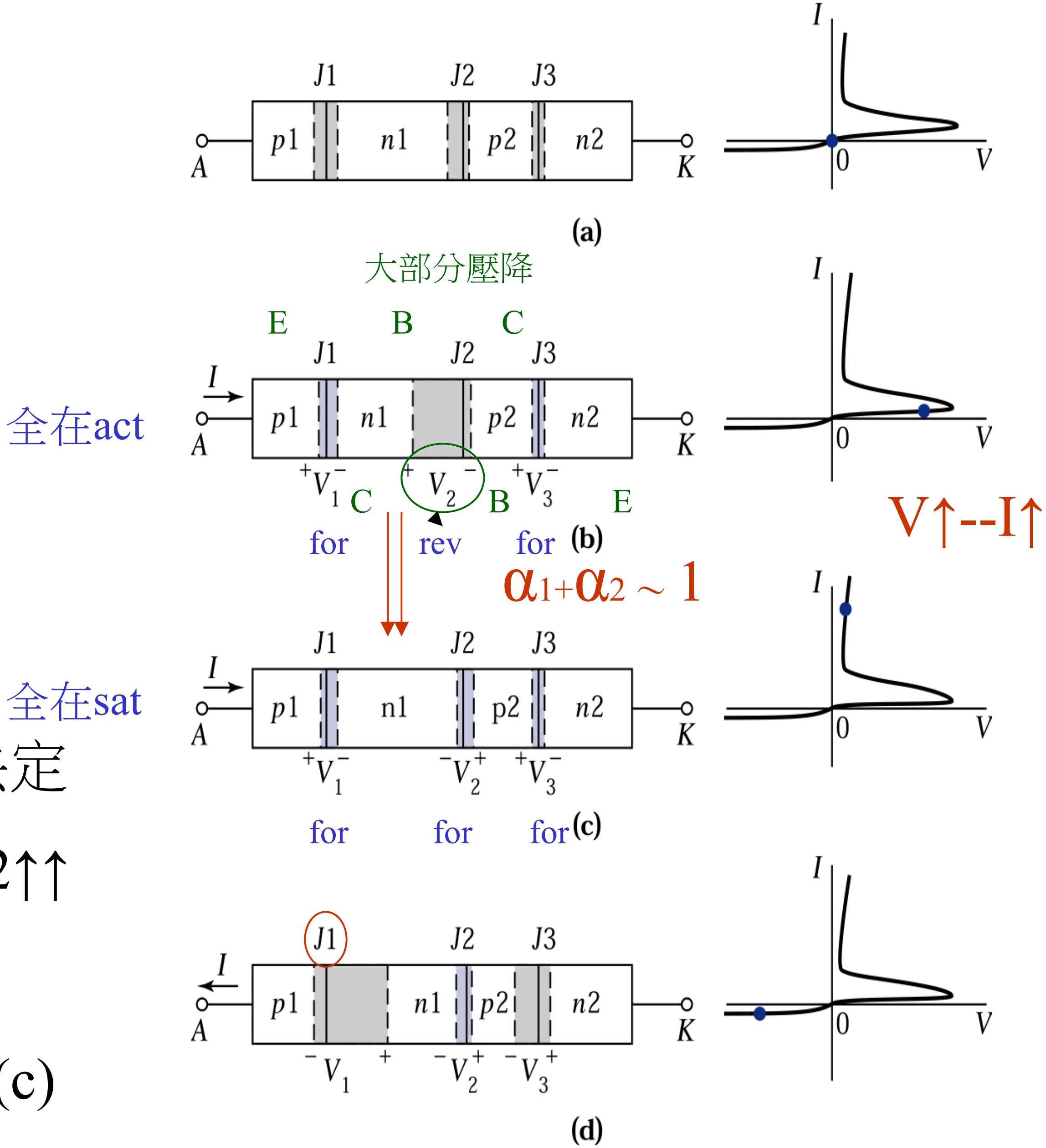
→ I_{CBO}之和

⇒ V_{AK} ↑，I ↑ ⟺ α_1 ↑，α_2 ↑

I 不大時，α_1，$\alpha_2 << 1$

$\alpha_1 + \alpha_2 \sim 1$時，break over

Figure 4.28. Depletion layer widths and voltage drops of a thyristor operated under (*a*) equilibrium, (*b*) forward blocking, (*c*) forward conducting, and (*d*) reverse blocking.



(d) Breakdown 由J_1決定

(b)若在P2加入Ig，α2↑↑

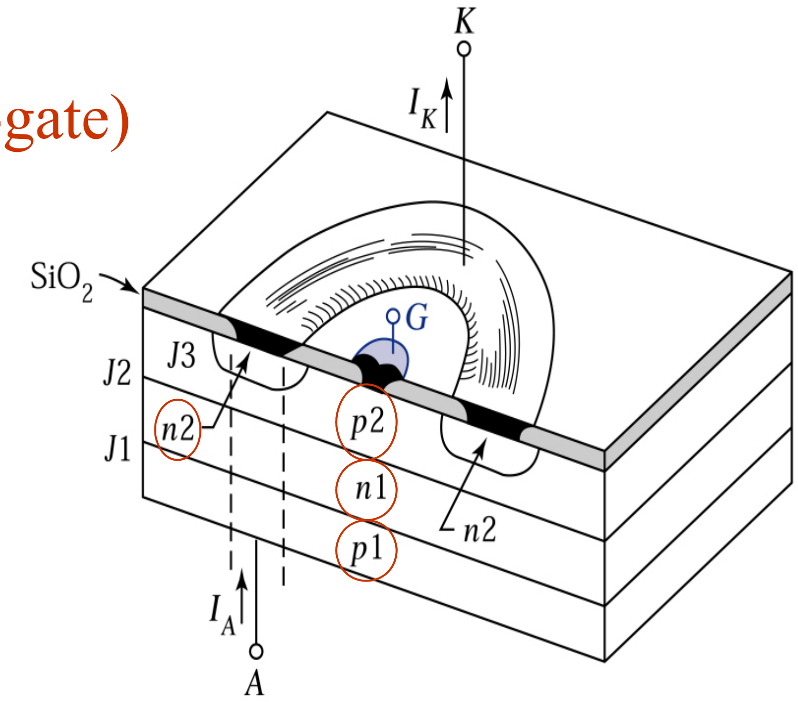
（→ α1+α2 ～ 1）

則能在小V進入(c)

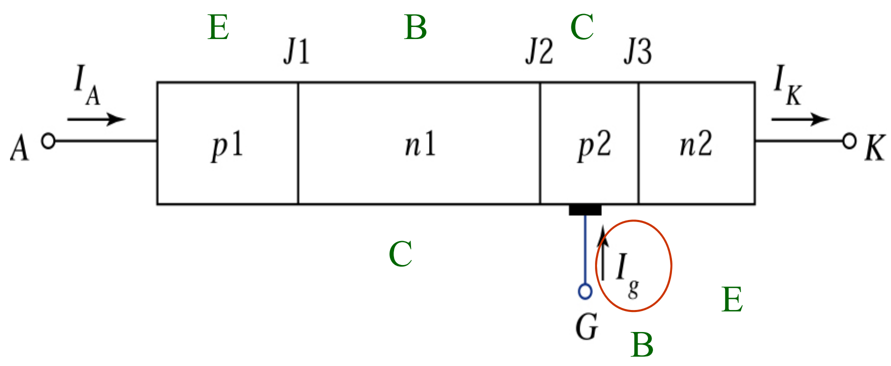
以Ig控制thyristor

SCR:矽控整流器(即在PNPN加-gate)

Figure 4.29.
(*a*) Schematic of a planar three-terminal thyristor.
(*b*) One-dimensional cross section of the planar thyristor.



(a)



(b)

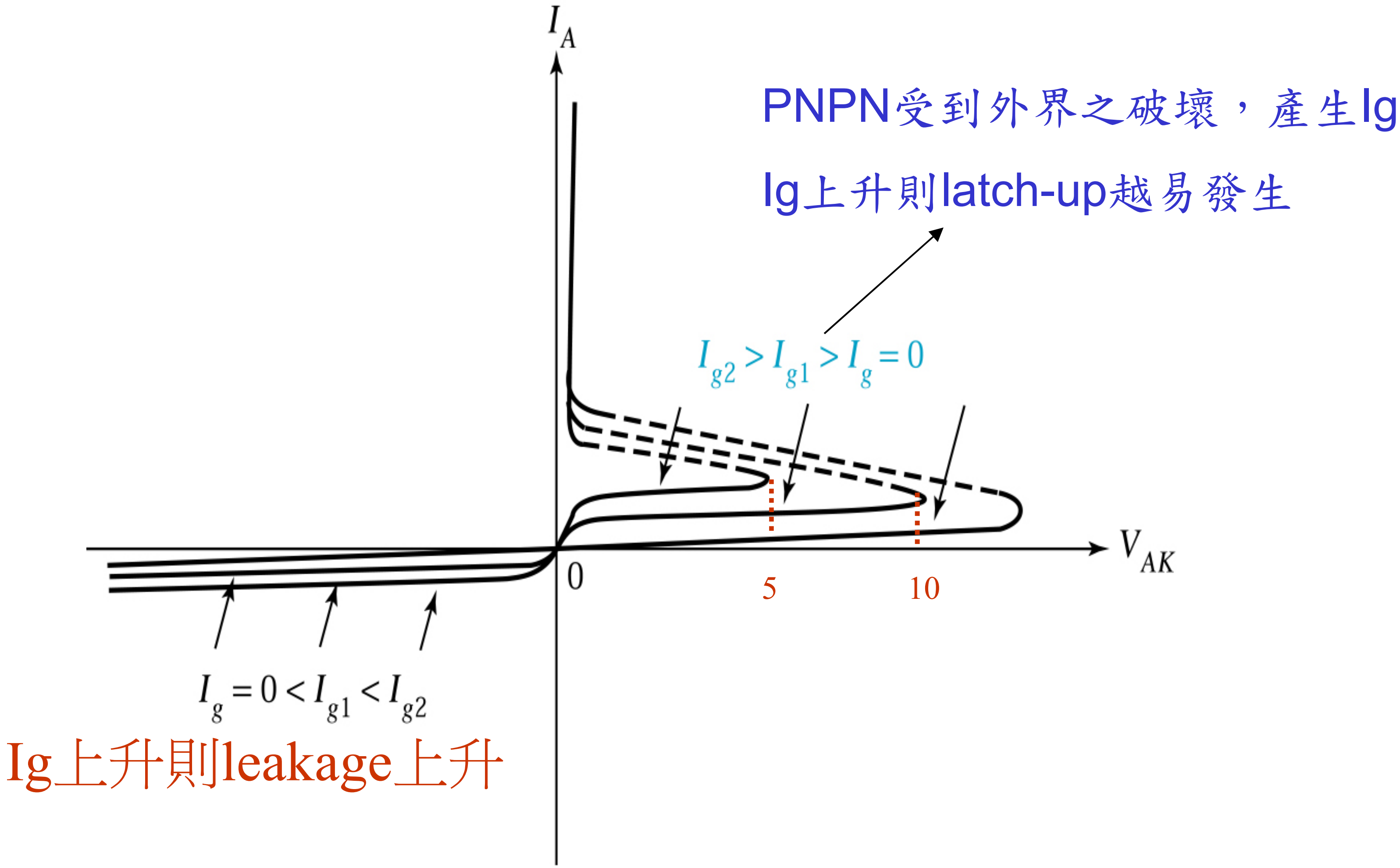


Figure 4.30. Affect of gate current on current-voltage characteristics of a thyristor.

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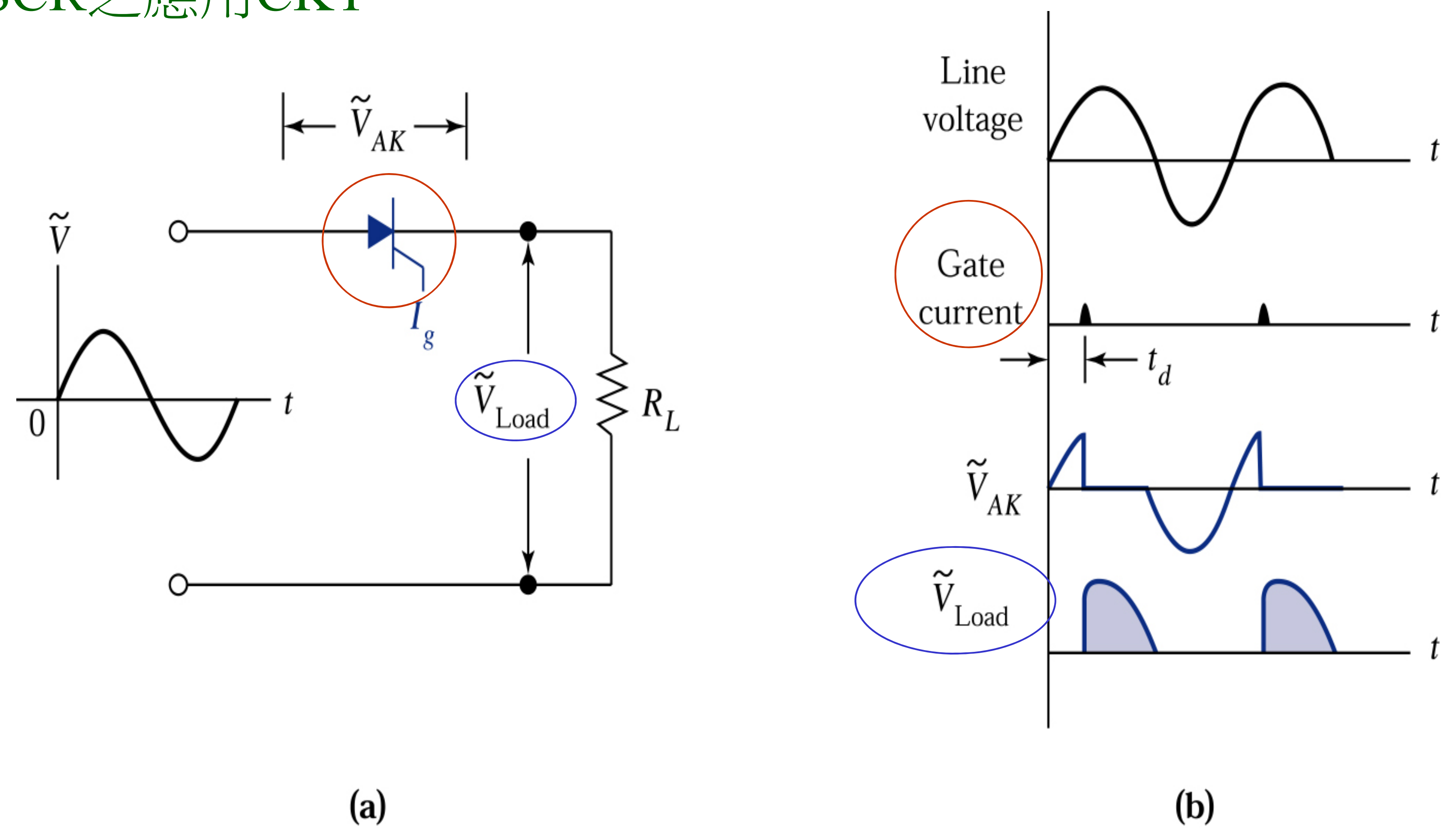
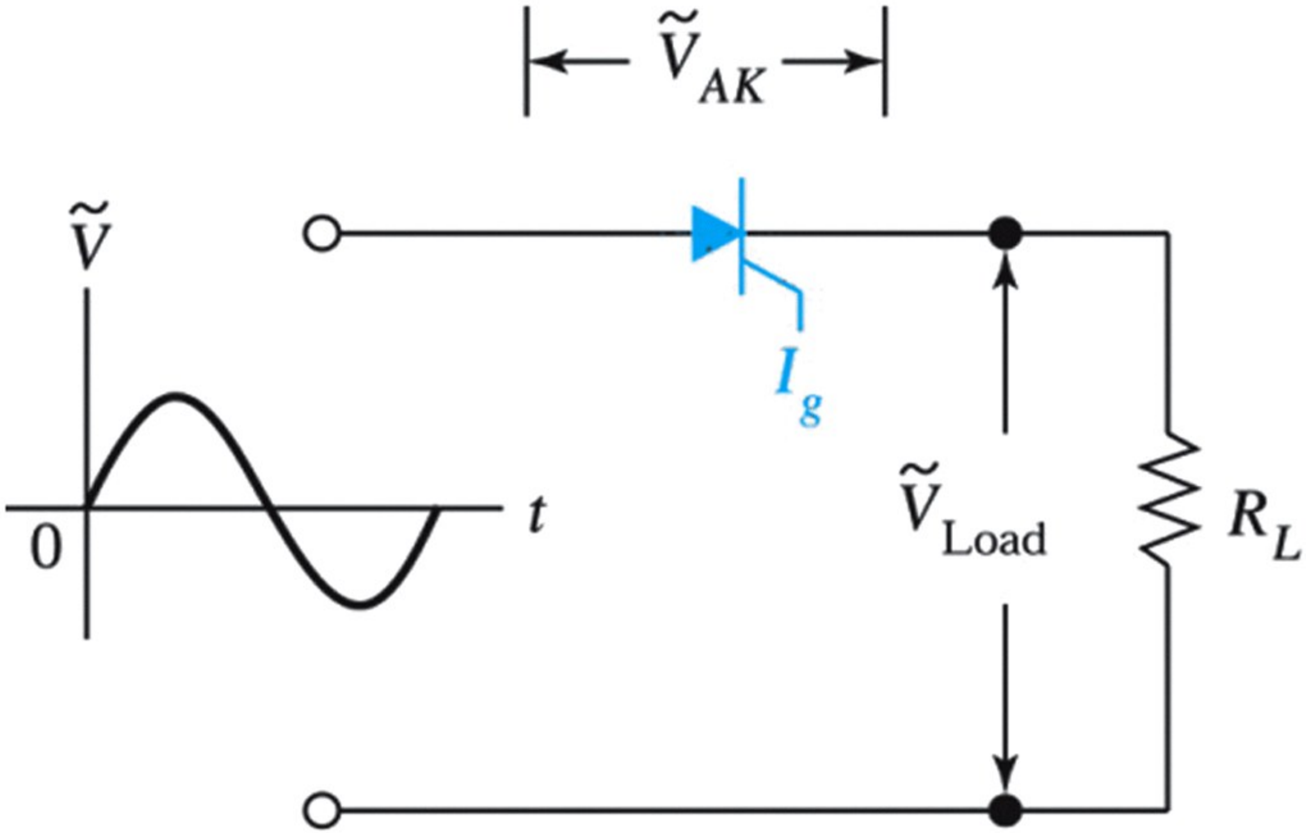


Figure 4.31. (*a*) Schematic circuit for a thyristor application. (*b*) Wave forms of voltages and gate current.



(a)

Figure 4.31a

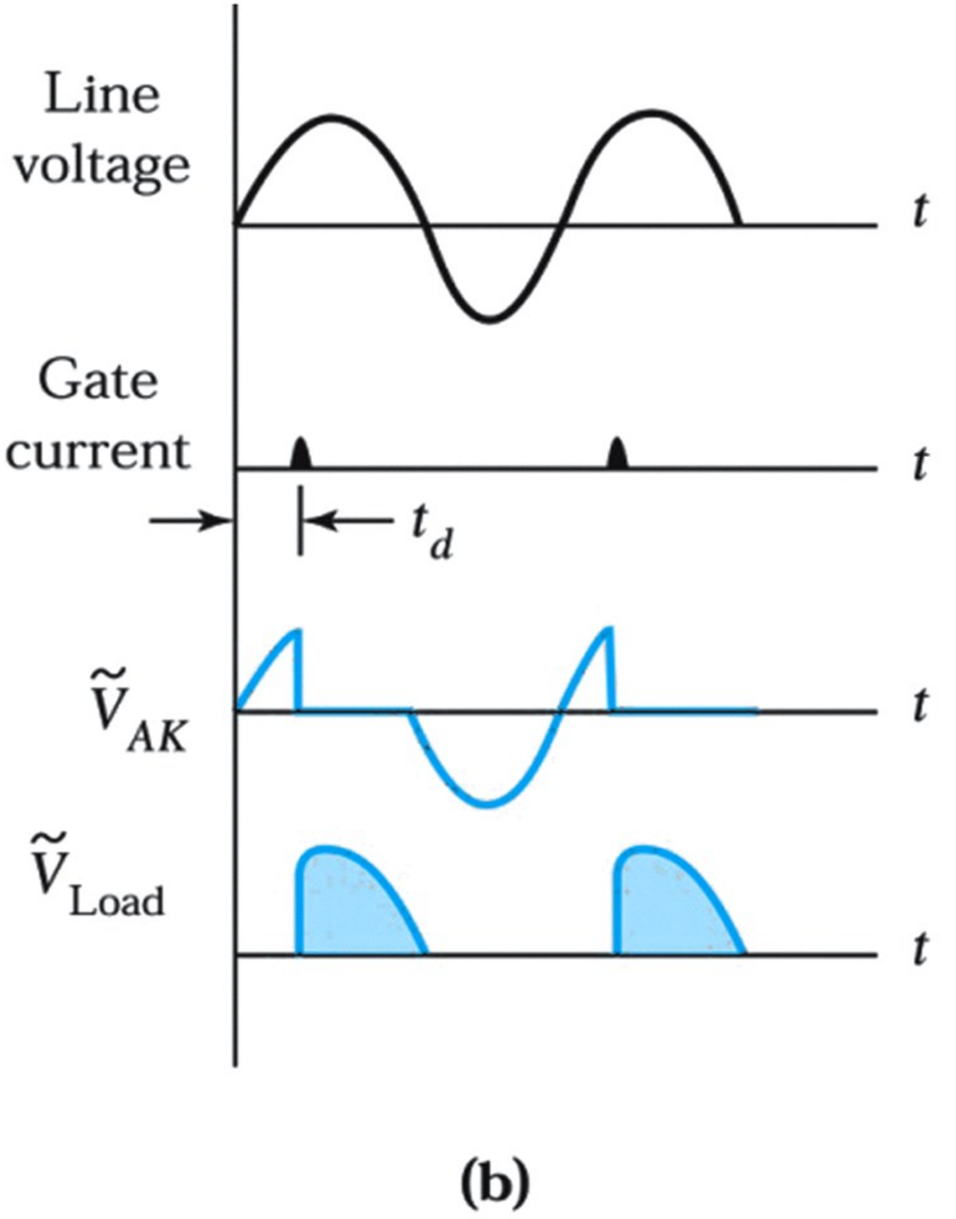

Line
voltage
t
Gate
current
t
t_d
$\tilde{V}_{AK}$
t
$\tilde{V}_{\text{Load}}$
t
(b)

Figure 4.31b

Figure 4.32.
(*a*) Two reverse-connected *p-n-p-n* diodes. (*b*) Integration of the diodes into a single two-terminal diode ac switch (diac). (*c*) Current-voltage characteristics of a diac.

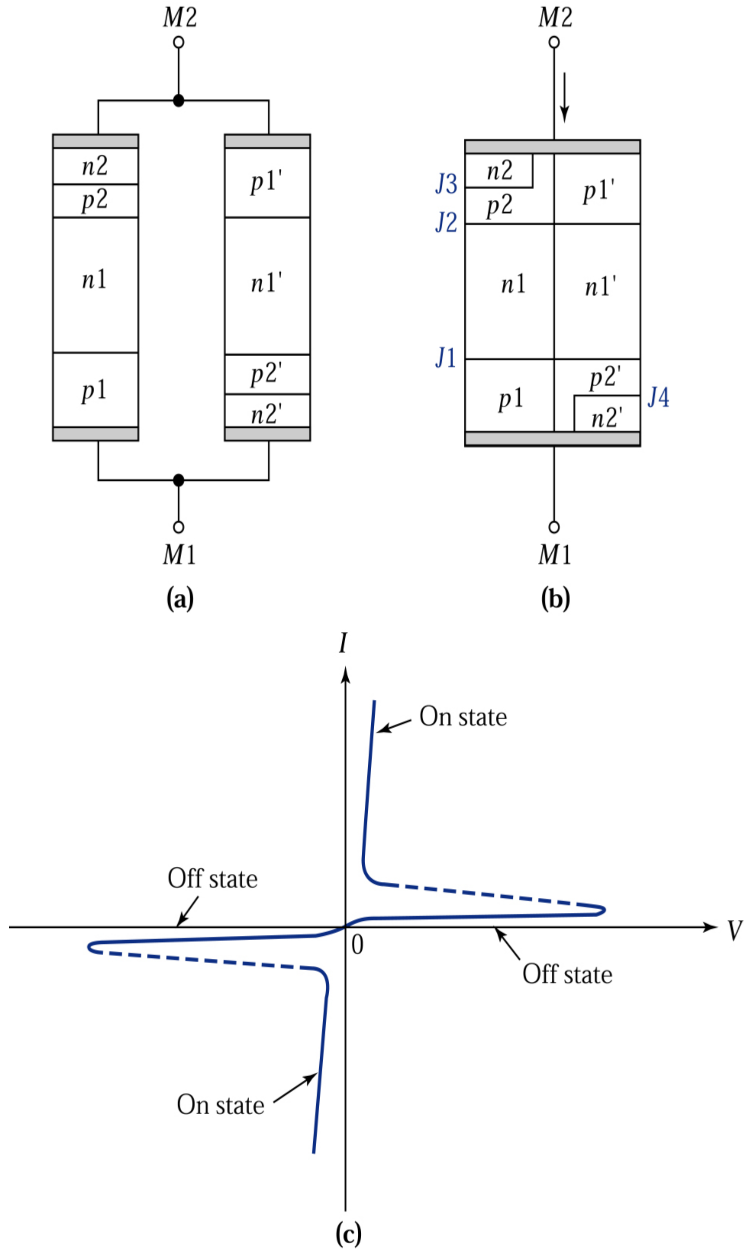


Figure 4.33.
Cross section of a triode ac switch, a six-layer structure having five *p*–*n* junctions.

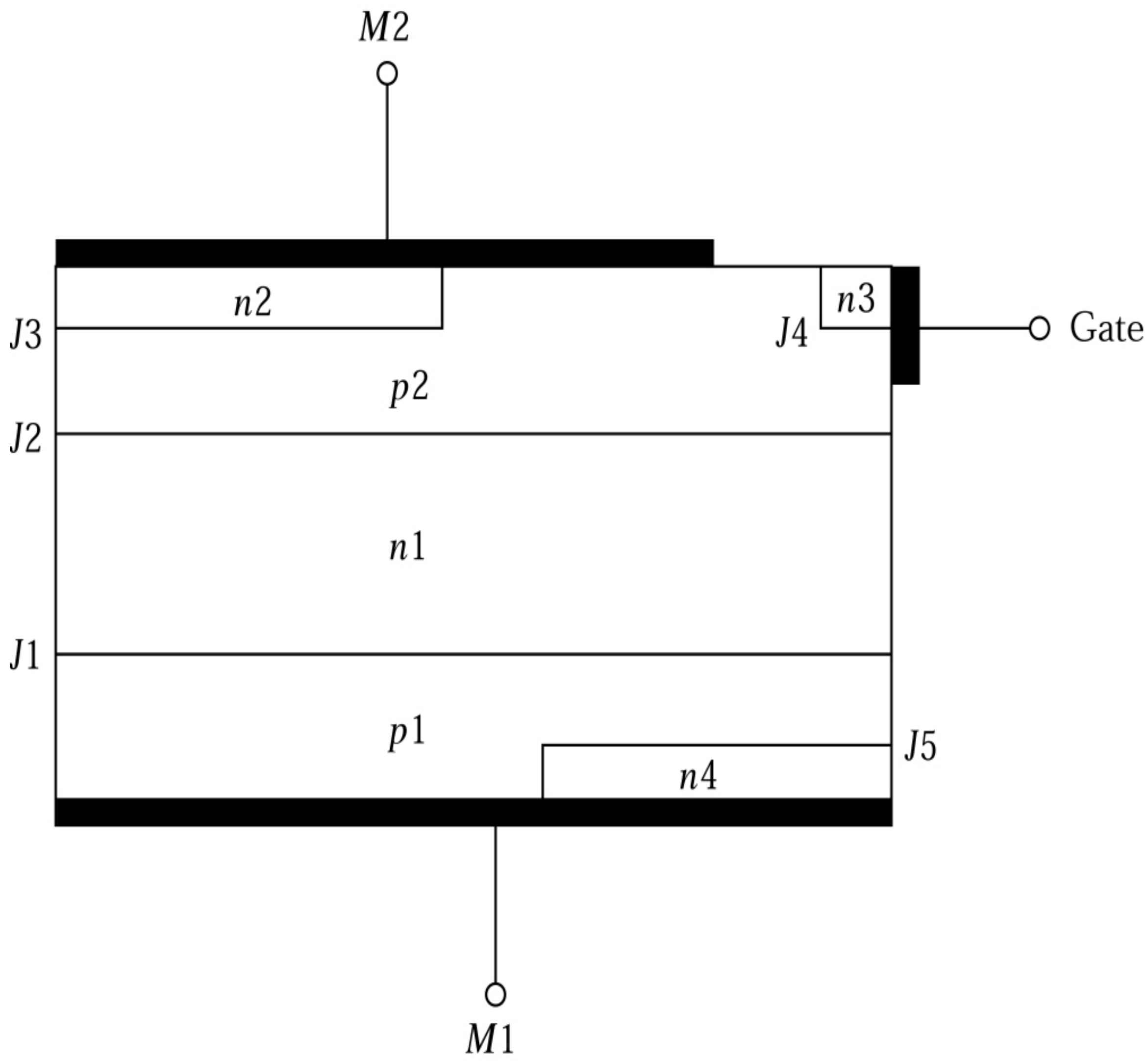
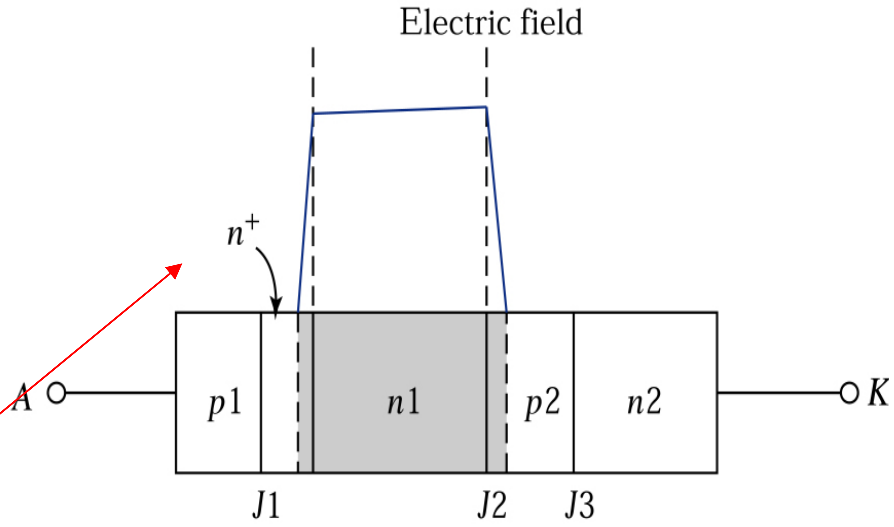
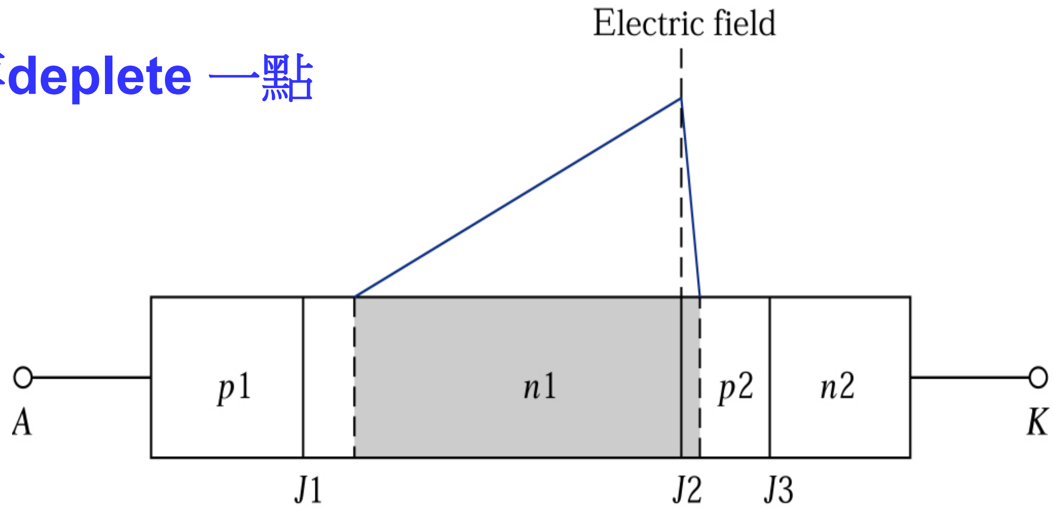


Figure
Comparison of the structure and electric field for the same forward-blocking voltage: (*a*) the asymmetric thyristor and (*b*) the conventional thyristor.





Asymmetric: 因為 **n+,** 只要**deplete** 一點
優點: n1 變薄,
Von ↓, t(on) ↓
T(off) ↓ (stored Q↓)

Figure
The gate **turn-off** thyristor with a negative voltage applied to the gate. The main applications of thyristors.[10]

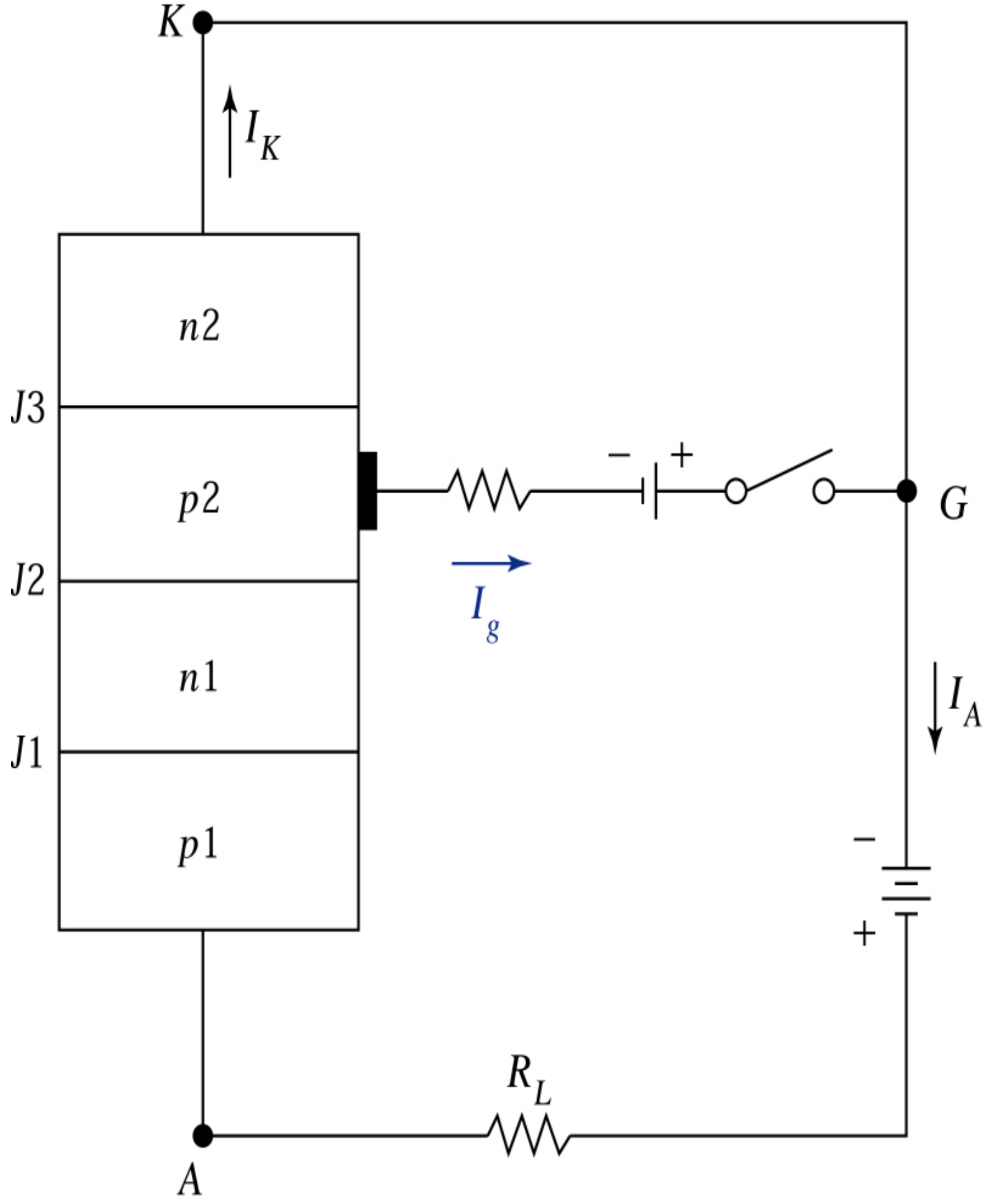


Figure
The main application of thyristors.[10]