Semiconductor Devices THIRD EDITION

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Chapter 3 *p*–*n* Junction

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(a) A bare *n*-type Si wafer. (b) An oxidized Si wafer by dry or wet oxidation.
(c) Application of resist.
(d) Resist exposure through the mask.



(a) The wafer after the development. (b) The wafer after SiO₂ removal. (c) The final result after a complete lithography process.
(d) A p-n junction is formed in the diffusion or implantation process.
(e) The wafer after metalization. (f) A p-n junction after the compete process.



(c)

Metal (f)



Figure 3.1 Current-voltage characteristics of a typical silicon *p-n* junction.



Figure 3.2. (*a*) Uniformly doped *p*-type and *n*-type semiconductors before the junction is formed. (*b*) The electric field in the depletion region and the energy band diagram of a *p*-*n* junction in thermal equilibrium.

$$V_{1} V_{2}$$

$$P_{p} p \frac{dV}{dx} = D_{p} \frac{dp}{dx}$$

$$-\mu_{p} p \frac{dV}{dx} = D_{p} \frac{dp}{dx}$$

$$dV = -\frac{D_{p}}{\mu_{p}} \times \frac{dp}{p}$$

$$V_{21} = \frac{kT}{q} \ln \frac{p_{1}}{p_{2}}$$

$$= q\mu_{p} p \left(\frac{1}{q} \frac{dE_{i}}{dx}\right) - kT\mu_{p} \frac{dp}{dx} = 0,$$
(1)

又由已知
$$p = n_i e^{(E_i - E_F)/kT}$$
 (2)
(2)
 $\frac{dp}{dx} = \frac{p}{kT} \left(\frac{dE_i}{dx} - \frac{dE_F}{dx} \right)$ (3)
(3)代八(1)

$$J_p = \mu_p p \frac{dE_F}{dx} = 0 \tag{4}$$

$$\frac{dE_F}{dx} = 0.$$
(5)
$$\begin{cases} (1) 魚 外 加 電 場 \\ (2) 熱 平 衡 \end{cases}$$

•注意 dEi/dx ≠ 0

•
$$\pm$$
 Poisson's eq. $\nabla^2 V = -\frac{\rho}{\varepsilon}$ $(\nabla \cdot D = \rho)$

中性區
$$\rightarrow \frac{d^2 \psi}{dx^2} = 0$$
 即無 ρ_s 無 E⁽⁸⁾
所以 $N_D - N_A + p - n = 0.$ (9)

$$\begin{aligned} & \begin{array}{l} p\text{-type} \\ & \psi_p \equiv -\frac{1}{q} \left(E_i - E_F \right) \Big|_{x \leq -x_p} = -\frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right). & \begin{array}{l} \text{(ND=n=0, $\rho=NA$)} \\ & \text{(10)} \\ \end{array} \\ & \begin{array}{l} & \psi_n \equiv -\frac{1}{q} \left(E_i - E_F \right) \Big|_{x \geq x_n} = -\frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right). & \begin{array}{l} & \text{(11)} \\ & \text{(NA=p=0, $\rho=ND$)} \\ & \text{n-type} \end{array} \end{aligned}$$



空乏區中, Poisson's eq. 為
$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_s} \left(N_A - N_D \right).$$
(13)

$$\frac{d^2\psi}{dx^2} \equiv -\frac{d\mathscr{E}}{dx} = -\frac{\rho_s}{\varepsilon_s} = -\frac{q}{\varepsilon_s} \left(N_D - N_A + p - n\right).$$
(7)







(c)



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Figure 3.4. Built-in potentials on the *p*-side and *n*-side of abrupt junctions in Si and GaAs as a function of impurity concentration.



Abrupt Junction

計算方便,亦大都屬於此種Junction



Figure 3.6.

(*a*) Space charge distribution in the depletion region at thermal equilibrium. (*b*) Electric-field distribution. The shaded area corresponds to the built-in potential.

D

n



$$\begin{cases} N_A x_p = N_D x_n. \quad (15) & 0 \\ W = x_p + x_n. \quad (16) & 0 \\ Depletion width \end{cases}$$

$$\begin{aligned}
\mathscr{E}(x) &= -\frac{d\psi}{dx} = -\frac{qN_A(x+x_p)}{\varepsilon_s} & \text{for } -x_p \leq x < 0 \\
& \vdots \frac{d^2\Psi}{dx^2} = \frac{qN}{\varepsilon_s} \\
\mathscr{E}(x) &= -\mathscr{E}_m + \frac{qN_Dx}{\varepsilon_x} = \frac{qN_D}{\varepsilon_s} (x-x_n) & \text{for } 0 < x \leq x_n,
\end{aligned}$$
(17a)

$$\mathscr{E}_{m} = \frac{qN_{D}x_{n}}{\varepsilon_{s}} = \frac{qN_{A}x_{p}}{\varepsilon_{s}}.$$
(18)

area

$$V_{bi} = -\int_{-x_p}^{x_n} \mathscr{E}(x) dx = -\int_{-x_p}^{0} \mathscr{E}(x) dx \Big|_{p\text{-side}} - \int_{0}^{x_n} \mathscr{E}(x) dx \Big|_{n\text{-side}}$$
$$= \frac{qN_A x_p^2}{2\varepsilon_s} + \frac{qN_D x_n^2}{2\varepsilon_s} = \frac{1}{2} \mathscr{E}_m W.$$
(19)

$$\pm (15)(19) \qquad W = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{N_A + N_D}{N_A N_D}\right) V_{bi}}.$$

(20)

Figure 3.7.

p+/n

(a) One-sided abrupt junction (with $N_A >> N_D$) in thermal equilibrium.

- (b) Space charge distribution.
- (c) Electric-field distribution.

(*d*) Potential distribution with distance, where V_{bi} is the built-in potential.



p+/n NA>>ND
$$\rightarrow \qquad W \cong x_n = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}}.$$

(21)

•實際p/n junction亦多為abrupt

$$\mathscr{E}_m = \frac{qN_BW}{\varepsilon_s}$$
(23)

$$\mathscr{E}(x) = \frac{qN_B}{\varepsilon_s} \left(-W + x\right) = -\mathscr{E}_m \left(1 - \frac{x}{W}\right), \qquad (24)$$
$$\psi(x) = \frac{V_{bi}x}{W} \left(2 - \frac{x}{W}\right). \qquad (x = W, \ \Psi(W) = Vbi) (26)$$

Figure 3.8.

Schematic representation of depletion layer width and energy band diagrams of a *p-n* junction under various biasing conditions.

a) Thermal-equilbrium condition. (*b*) Forward-bias condition. (*c*) Reverse-bias condition.



•若外加偏壓



☆ V:forward為正, reverse為負

(27)

Figure 3.9.

Linearly graded junction in thermal equilibrium.

- (a) Impurity distribution.
- (b) Electric-field distribution.
- (c) Potential distribution with distance.
- (d) Energy band diagram.



Slope= a









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• Linearly Graded Junction

$$\frac{d^{2}\psi}{dx^{2}} = \frac{-d\mathscr{E}}{dx} = \frac{-\rho_{s}}{\varepsilon_{s}} = \frac{-q}{\varepsilon_{s}}ax - \frac{W}{2} \le x \le \frac{W}{2}, \qquad (28)$$

$$\mathscr{E}(x) = -\frac{qa}{\varepsilon_{s}} \left[\frac{\left(W/2\right)^{2} - x^{2}}{2} \right]. \qquad (29)$$

$$\mathscr{E}_{m} = \frac{qaW^{2}}{8\varepsilon_{s}}. \qquad (29a)$$

$$W = \left(\frac{12\varepsilon_{s}V_{bi}}{qa}\right)^{1/3}. \qquad (31)$$



Figure 3.10. Built-in potential for a linearly graded junction in Si and GaAs as a function of impurity gradient.



Figure 3.11.

(a) *p-n* junction with an arbitrary impurity profile under reverse bias. (*b*) Change in space charge distribution due to change in applied bias. (*c*) Corresponding change in electric-field distribution.

$$C_{j} \equiv \frac{dQ}{dV} = \frac{dQ}{W\frac{dQ}{\varepsilon_{s}}} = \frac{\varepsilon_{s}}{W}$$
(32)



For a one-sided abrupt junction

$$C_{j} = \frac{\varepsilon_{s}}{W} = \sqrt{\frac{q\varepsilon_{s}N_{B}}{2(V_{bi} - V)}}$$
$$\frac{1}{C_{j}^{2}} = \frac{2(V_{bi} - V)}{q\varepsilon_{s}N_{B}}$$
$$* 1/Cj^{2} \text{ VS V 得到一直線}$$

1: 斜率可算 NB (bulk concentration)

2: 交點可算Vbi

△ 測量 doping profile 用 C-V 法

\bigcirc abrupt junction

Figure 3.12.

(a) p⁺-n junction with an arbitrary impurity distribution. (b)
Change in space charge distribution in the lightly doped side due to a change in applied bias. (c) Corresponding change in the electric-field distribution.



$$N(W) = \frac{2}{q\varepsilon_s} \left(\frac{1}{\frac{d(1/C_j^2)}{dV}}\right)$$



Figure 3.13. Impurity profiles for hyperabrupt, one-sided abrupt, and one-sided linearly graded junctions.



Excess carrier

$$n_{p} - n_{po} = n_{po} \left(e^{qV/kT} - 1 \right).$$

$$p_{n} - p_{no} = p_{no} \left(e^{qV/kT} - 1 \right)$$

$$\therefore n_{no} = n_{po} e^{qV_{bi}/kT}$$

$$n_{n} = n_{p} e^{q(V_{bi} - V)/kT}, \quad n_{n} \sim n_{no}$$

$$n_p = n_{po} e^{qV/kT}$$

Excess carrier

$$J_p(x_n) = -qD_p \frac{dp_n}{dx} \Big|_{x_n} = \frac{qD_p p_{no}}{L_p} \Big(e^{qV/kT} - 1\Big).$$

$$J_n(-x_p) = qD_n \frac{dn_p}{dx}\Big|_{-x_p} = \frac{qD_n n_{po}}{L_n} \Big(e^{qV/kT} - 1\Big)$$

$$\therefore \frac{a p_n}{dx^2} - \frac{p_n - p_{no}}{D_p \tau_p} = 0$$

$$p_n = p_{no} + p_{no} (e^{qV/kT} - 1)e^{-(x - x_n)/L_p}$$

Figure 3.15.

Injected minority carrier distribution and electron and hole currents. (*a*) Forward bias. (*b*) Reverse bias. The figure illustrates idealized currents. For practical devices, the currents are not constant across the space charge layer.



Ideal diode eq.(僅求diff. current)

$$J = J_p(x_n) + J_n(-x_p) = J_s(e^{qV/kT} - 1),$$
V為負時,可略.J=Js為定值

$$J_s = \frac{qD_pp_{no}}{L_p} + \frac{qD_nn_{po}}{L_n},$$
:sat. current density







V

Figure 3.16. Ideal current-voltage characteristics.

(b) Semilog plot.



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Generation-Recombination and high-injection Effect*

$$G = -U \approx \left[\frac{\sigma_p \sigma_n V_{th} N_t}{\sigma_n \exp[\frac{E_t - E_i}{kT}] + \sigma_p \exp[\frac{E_i - E_t}{kT}]} \right] = \frac{n_i}{\tau_g}$$

空乏區之產生電流 (因為G= ni / \taug)

Assume $\sigma n = \sigma p = \sigma 0$ $G \approx \frac{\sigma_0 V_{th} N_t n_i}{2 \cosh[\frac{E_t - E_i}{kT}]}$ G = Max at Et=Ei Generation-Recombination and high-injection Effect*

空乏區之產生電流

$$J_{gen} = \int_{0}^{W} qGdx \cong qGW = \frac{qn_{i}W}{\tau_{g}}$$
(因為G=ni/\taug)
For p+/n (NA>>ND) (55a) (Jdiff為VR \geq 3kT/q
下由(55)得到)
反向 $J_{R} \cong q \sqrt{\frac{D_{p}}{\tau_{p}}} \frac{n_{i}^{2}}{N_{D}} + \frac{qn_{i}W}{\tau_{g}}$.
Ge: ni大 · Jdiff dominate
Si : ni小 · Jgen dominate

Recombination Effect*

$$n_n p_n \cong n_{n0} p_{n0} e^{qV/kT} = n_i^2 e^{qV/kT}$$

Assume $\sigma n = \sigma p = \sigma 0$

$$U \approx \frac{\sigma_0 V_{th} N_t n_i^2 \left(e^{qV/kT} - 1\right)}{n_n + p_n + 2n_i \cosh \frac{E_i - E_t}{kT}}$$

at Et=Ei
$$U \approx \sigma_0 V_{th} N_t \frac{n_i^2 \left(e^{qV/kT} - 1\right)}{n_n + p_n + 2n_i}$$

Recombination Effect*

At $n_n + p_n = \min_{n \to \infty}$, U = Max. $n_{n}p_{n} = 常數$ $U \max \approx \sigma_0 V_{th} N_t \frac{n_i^2 \left(e^{qV/kT} - 1\right)}{2n_i \left(e^{qV/2kT} + 1\right)}$ $dn_n p_n + n_n dp_n = 0$ $-dn_n = \frac{n_n}{dp_n}dp_n$ p_n $d(p_n+n_n)=0$ $U \max \approx \frac{1}{2} \sigma_0 V_{th} N_t n_i e^{q V (2kT)}$ $dp_n = -dn_n = \frac{n_n}{-}dp_n$ p_n $p_n = n_n = n_i e^{q \sqrt{2kT}}$

Recombination Effect*







With increasing temp, increase of Idiff > Irecom due to Js Low temp, Jg dominate $\sim (V_R)^{1/2}$; high temp, Js dominate **(b)**

Trap analysis should be low temp

(a)

Figure 3.18. Temperature dependence of the current-voltage characteristics of a Si diode². (a) Forward bias. (b) Reverse bias.

Minority Carrier Storage excess ☆在Forward bias 會有 $Q_p = q \int_{x_n}^{\infty} \left(p_n - p_{no} \right) dx,$ $= q \int_{x_n}^{\infty} p_{no} \left(e^{qV/kT} - 1 \right) e^{-(x - x_n)/L_p} dx,$ $= qL_p p_{no} \Big(e^{qV/kT} - 1 \Big).$ $Q_p = \frac{L_p^2}{D_n} J_p(x_n) = \tau_p J_p(x_n)$ 雷流 Minority life time

Diffusion Capacitance

☆在 forward bias 下: *反向有Cj *順向有Cd

definition

$$C_{d} = AdQ_{p} / dV \quad dV 指 A.C.$$
$$C_{d} = \frac{Aq^{2}L_{p}p_{no}}{kT} e^{qV/kT}$$



Figure 3.19. Small-signal equivalent circuit of a *p-n* junction.



Figure 3.20. Transient behavior of a *p*-*n* junction (*a*) Basic switching circuit. (*b*) Transient response of the current switched from forward bias to reverse bias.





☆ For 快速switch,使 $\tau_{p\downarrow}$

☆ 在E_i增加 G-R center (doping Au 等)

Figure 3.21.

Normalized transient time versus the ratio of forward current to reverse current.³







Figure 3.22. Energy band diagrams under junction-breakdown conditions. (*a*) Tunneling effect (*b*) Avalanche multiplication.



Figure 3.23. Depletion region in a *p*-*n* junction with multiplication of an incident current.



Figure 3.24. Critical field at breakdown versus background doping for Si and GaAs one-sided abrupt junctions.⁵

Figure 3.25.

Avalanche breakdown voltage versus impurity concentration for one-sided abrupt junction and avalanche breakdown voltage versus impurity gradient for linearly graded junction in Si and GaAs. Dash-dot line indicates the onset of the tunneling mechanism.⁵



Figure 3.26. Breakdown voltage for diffused junctions. Inset shows the space charge distribution.⁶



 $N_B \downarrow$, $a \downarrow$, $V_B \uparrow$



Figure 3.27. Breakdown voltage for $p^+-\pi-n^+$ and $p^+-\nu-n^+$ junctions. *W* is the thickness of the **lightly doped** *p*-type (π) or the lightly doped *n*-type (ν) region.

Figure 3.28.

(a) Planar diffusion process that forms junction curvature near the edge of the diffusion mask, where r_i is the radius of curvature. (b) Cylindrical and spherical regions formed by diffusion through a rectangular mask.





Figure 3.29. Breakdown voltage versus impurity concentration for onesided abrupt doping profile with cylindrical and spherical junction geometries,⁷ where r_i is the radius of curvature indicated in Fig. 3.28..

Figure 3.30.

(a) Energy band diagram of two isolated semiconductors.
b) Energy band diagram of an ideal *n-p* heterojunction at thermal equilibrium.



Band offset: ΔEc , ΔEv Band alignment



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